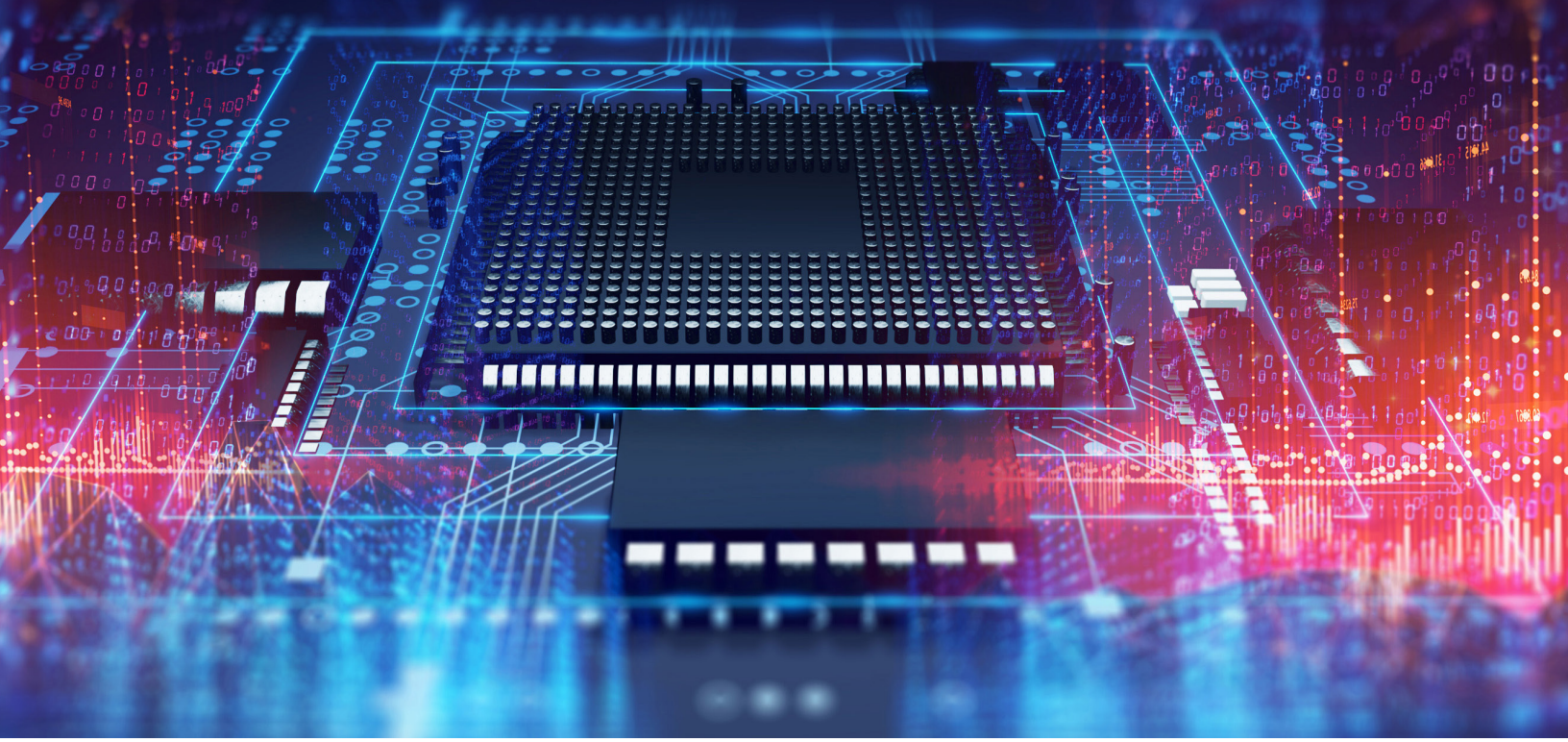


DIGITAL INDUSTRIES SOFTWARE

Tessent MemoryBIST

Memory self-test, repair and debug

Benefits

- Flexible and automated BIST IP integration, access network integration and pattern validation shorten time-to-market
- Resource sharing and flow integration with Tessent LogicBIST and Tessent TestKompress reduce overall DFT cost and increase defect coverage
- Design-time and field programmable algorithm specification allows complete control of test quality and test time trade-offs
- User controllable area and test time trade-off options enable product-specific test cost optimization
- On-chip global eFuse management and optional non-volatile memory test capability reduce overall manufacturing costs

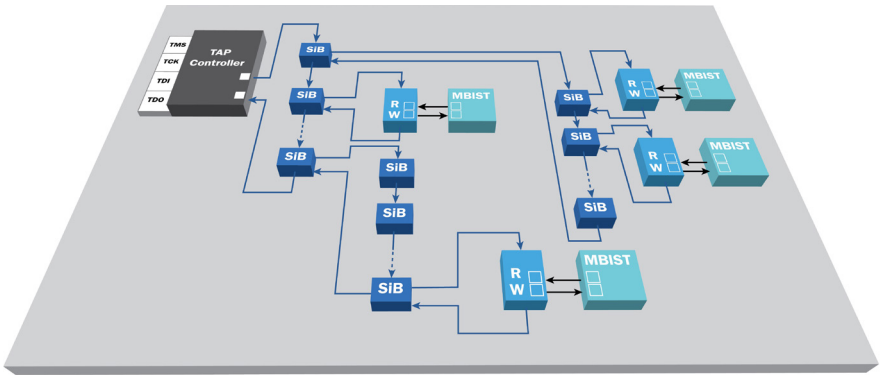
Industry-leading solution for Memory Built-in Self-Test

The Tessent™ MemoryBIST software and IP provide a complete solution for at-speed test, diagnosis, repair, debug and characterization of silicon memories. The solution's hierarchical architecture enables the addition of built-in self-test and self-repair capabilities at both the individual core level and the top level.

On-chip generated test patterns are delivered to the memories at application clock frequencies. The Tessent MemoryBIST controllers are configurable to support a variety of memory types, as well as a range of memory timing interfaces and port configurations. They are accessed and controlled through an IEEE 1687-2014 (IJTAG) network. This highly configurable network can access all Tessent IP and support any third-party IJTAG-compliant instruments. The controllers can be accessed throughout the life of the integrated circuit, including manufacturing test, silicon debug and in-system test.

Benefits *continued*

- Desktop-based test debug and characterization speed time-to-market
- Customizable pass/fail criteria provided by the ECC option enhances yield and reliability
- Works with ECC detection/correction capabilities to safeguard against aging defects



Hierarchical Tessent MemoryBIST infrastructure.

Features

- Hard and soft programmable algorithm support to balance quality and test time
- Comprehensive defect coverage for advanced technologies such as FinFET
- Power-aware test and repair for multiple power domains
- Fully autonomous hard and soft incremental repair solution for on-chip and off-chip analysis
- Advanced BIST Access Port (BAP) configurable interface for minimal latency in-system test and reduced ATE test time
- Simple ATE test flow using fast on-chip trim calibration for optimal read/write operations
- Flags low-quality memory devices and allows health monitoring to track failures over time
- External memory and 2.5/3D-IC support for multi-die and TSV interconnects
- Shared-bus interface and full interoperability with third-party memory IP
- Unified characterization and debug platform with Tessent SiliconInsight

Tessent MemoryBIST includes a comprehensive and flexible implementation flow built on the Tessent Platform. Automation is provided for design rule checking, test planning, BIST integration and verification either at the RTL or gate level. Tessent SiliconInsight™ manages the back-end flow for memory test (debug and characterization). This interactive, desktop-based debug environment can provide diagnosis data down to the chip-level XY coordinate of failing cells.

Advanced BIST access port

The advanced BAP provides a configurable interface to enable optimized in-system testing. This direct access interface supports a low-latency protocol for configuring the MemoryBIST controller, executing Go/NoGo tests and monitoring the pass/fail status. Eliminating shift cycles to configure the controllers in the IJTAG environment serially can significantly reduce test time.

Algorithm programmability

Memory test algorithms can be hard-coded into the Tessent MemoryBIST controller at design time. The algorithms can be chosen from a comprehensive library collection or customized by the user. These algorithms can then be applied to each memory through run-time control. This capability helps optimize test time by selecting shorter test algorithms as the manufacturing process matures.

Additionally, the Tessent MemoryBIST Field Programmable option enables any memory BIST controller to incorporate full run-time programmability. With this feature, any user-programmed memory test algorithm can be downloaded into the BIST controller while on the tester or in-system. This capability enables the handling of unforeseen defect mechanisms without requiring a design re-spin. Field algorithm programming facilitates yield learning because different diagnostic algorithms can be downloaded during yield ramp.

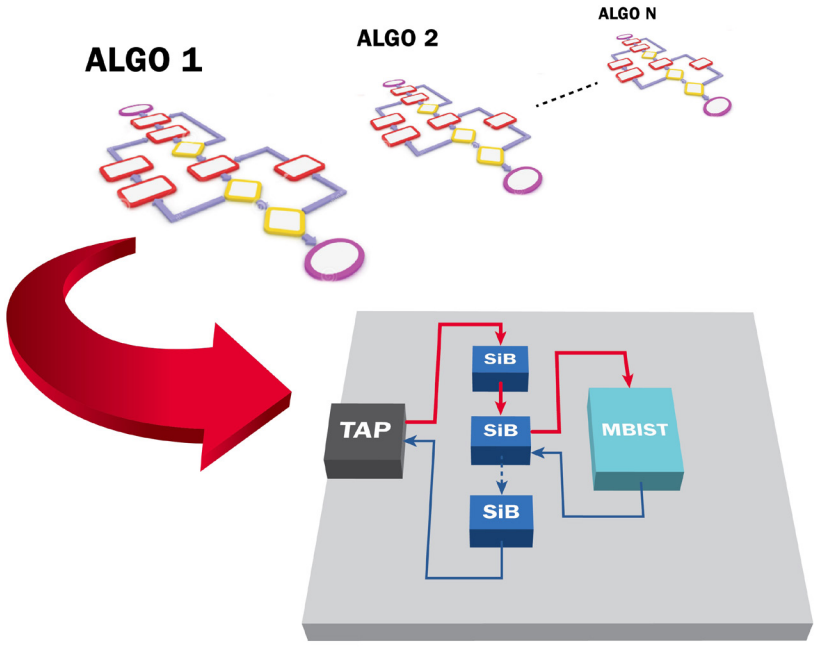
Power-aware on-chip self-repair

The Tessent MemoryBIST repair option eliminates the complexities and costs associated with external repair flows. It tests and permanently repairs all defective memories in a chip using virtually no external resources. The Tessent MemoryBIST built-in self-repair (BISR) architecture uses programmable fuses (eFuses) or a One-Time Programmable (OTP) device to store memory repair info. During memory test, built-in repair analysis engines within each BIST controller calculate the fuse information needed to repair each memory.

Repair information can be accumulated over different test conditions. The final data is stored in a local BISR register, part of a serial chain that belongs to a power domain. A fuse controller operates these serial chains to shift and compress repair data into a central eFuse array.

Hard incremental repair is also supported. The results of the additional repair analysis performed during subsequent manufacturing or in-system tests can be added to the stored fuse information.

Tessent MemoryBIST offers flexibility for eFuse management, enabling a balance between test time and routing congestion. With a central eFuse, using a single serial chain can minimize routing; having multiple chains and/or distributed eFuses across cores can minimize overall repair time by leveraging concurrent operation.



Tessent MemoryBIST field programmability.

Shared-bus interface support

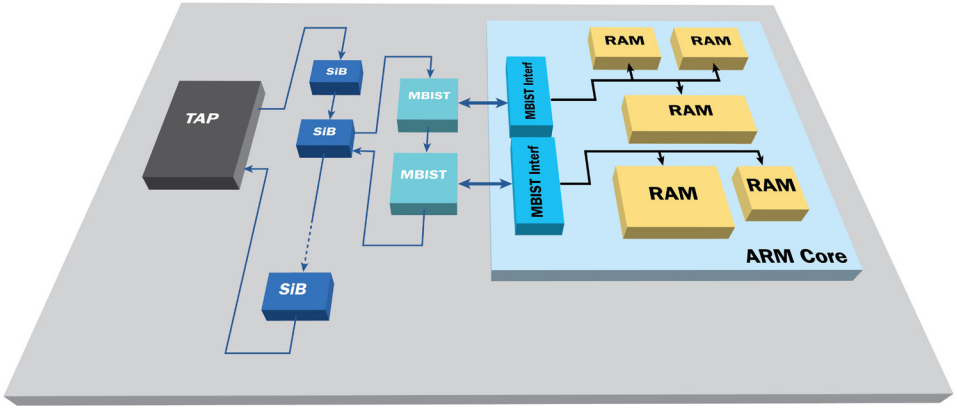
Processor cores from vendors such as Arm® can provide a shared-bus interface to the memories internal to the processor core IP. This interface provides a standard set of shared address, data and control ports to access all memories embedded within each processor core. The memory BIST controller no longer communicates directly with each memory; instead, it must now understand how to access each memory through the common interface signals. Additionally, it must account for the varying levels of pipelining to and from each memory.

Tessent MemoryBIST supports the integration of memory BIST and repair capabilities into a design that contains both stand-alone memories and memories embedded within an IP core that are only accessible through a shared-bus interface.

External memory and 3D IC support

Tessent MemoryBIST provides support for testing memories that are external to the device containing the BIST IP. Support is provided for both stand-alone memory packages at the board level and 2.5/3D packages consisting of one or more memory dies stacked on top of a separate logic die.

The memory BIST control logic is integrated into the logic chip, allowing at-speed testing of the memory bus logic and connections. Tessent MemoryBIST supports Wide IO and HBM interfaces and package configurations where multiple memory dies are stacked and connected to a single logic die via the same electrical interconnects. Both bond wire and through-silicon via (TSV)-based interconnects can be tested. The field programmability option supports changes in the memory die, or variant stacks that use different memory designs.



Testing through a shared bus interface.

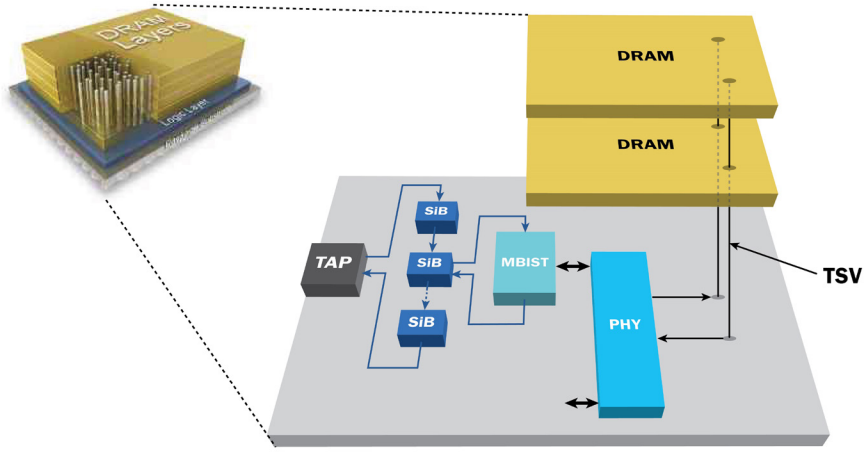
ECC-aware Memory BIST

The Tessent MemoryBIST ECC option complements memory repair to deliver the highest yield improvement for both production and post-silicon applications. This solution can indicate if ECC (Error-Correcting Code) should be used as the primary correction method or to supplement repair capabilities (when present). The tool is flexible enough to account for all standard usage possibilities because its threshold values are not hard-coded in RTL.

The ECC-aware option enables the optimal combination of memory redundancy and ECC to be utilized during manufacturing and in-system tests. It does this by allowing the selection of the number of ECC bits to be used during runtime. During manufacturing, when the ECC circuitry can be turned off, MBIST verifies the integrity of the entire memory, including the array portion where ECC check bits are typically stored. Redundant or spare resources can be allocated where they are needed the most, leveraging ECC's capabilities to detect and correct occasional errors. This solution includes a Failing Bit Counter (FBC) that provides health monitoring capabilities.

Non-volatile memory (NVM) support

The Tessent MemoryBIST NVM option extends silicon-proven MBIST test applications from SRAMs to MRAMs and other non-volatile memories (NVMs). It simplifies a DFT engineer's work by automating NVM tests on-chip, performing automatic trim search settings for both manufacturing and in-system purposes. It streamlines what is normally a complex ATE test sequence into a task that can be accomplished using a lower-cost tester.



Testing 3D stacked memory die.

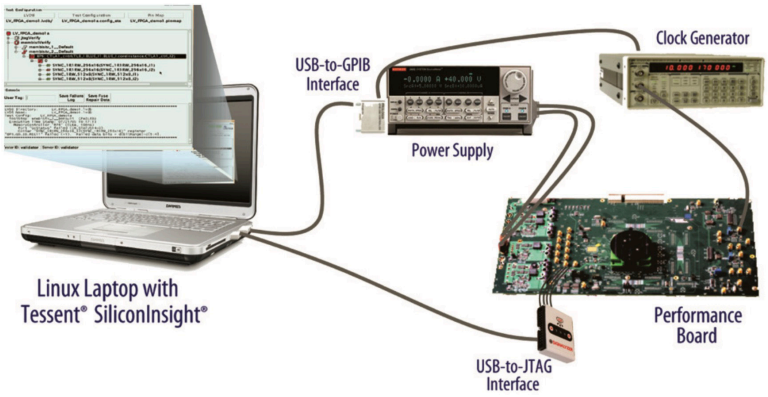
Test debug and characterization

Tessent SiliconInsight provides an automated environment for test bring-up, debug and silicon characterization. Designers can interactively execute tests, collect data and generate shmoo plots for any selection and order of BIST-tested blocks on the device, either in a lab environment or on the tester through ATE-Connect™. ATE-Connect enables direct communication between Tessent DFT software and ATE hardware.

Tessent SiliconInsight can significantly increase productivity during silicon validation and debug, speeding time-to-market.

Tessent Product Family

Tessent offers comprehensive solutions for integrated circuit (IC) testing and functional monitoring. These include top-tier tools designed for testing optimization, data analytics, security, debugging, and in-life monitoring. Our products ensure maximum test coverage, accelerate yield ramp-up and enhance quality and reliability throughout the silicon lifecycle.



Tessent SiliconInsight.

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