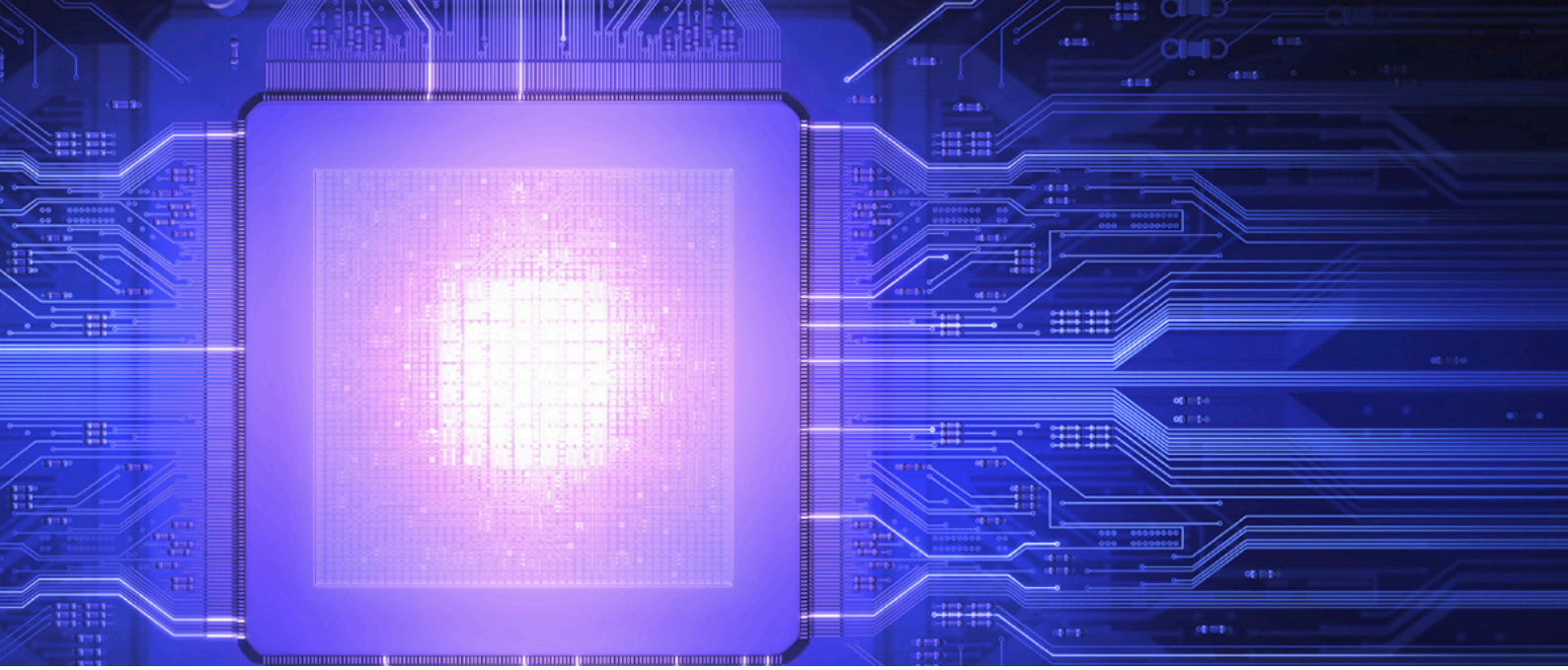

DIGITAL INDUSTRIES SOFTWARE

Tessent LogicBIST with Observation Scan Technology

Executive summary

To meet the ISO 26262 requirements for high quality and long-term reliability, it is important to implement on-chip safety mechanisms that can achieve an extremely high defect coverage of the logic. This paper describes a new logic BIST technology that allows the capturing of test responses from the circuit during scan shifting for the observe point flops. This Observation Scan Technology (OST) improves logic BIST (LBIST) test quality and reduces in-system test time. Empirical results gathered from industry designs show that LBIST-OST enables 90% test coverage with up to 10X fewer LBIST patterns when compared with previous industry-leading LBIST solutions.

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Introduction

Advanced safety features and the auto industry's push to automate the driving experience has caused rapid growth in the electronic content of automobiles. This electronic content has become both increasingly complex and tightly integrated into the automobile's safety systems. ISO 26262 was introduced to govern the functional safety requirements of these systems and has been broadly adopted by automotive manufacturers and suppliers worldwide.

To meet these requirements for high quality and long term reliability, it is important to implement safety mechanisms that can achieve an extremely high defect coverage of the logic. To achieve this, structural test techniques as used for manufacturing test provide an ideal mechanism to reach the highest coverage possible. The recommended target for these structural in-system tests is a stuck-at coverage of target of 90%.

The other targets to consider when implementing insystem test, as detailed in the ISO 26262 specification are:

• FTTI Fault Tolerant Time Interval – This defines the time-span in which a fault or faults can be present in a system before a hazardous event occurs

• FRTI Fault Reaction Time Interval – This is the time span from the detection of a fault to the system being put into a safe state

• DTI Diagnostics Time Interval - The time span from when a fault occurs to when it can be detected

The FTTI will be defined as part of the overall failure modes, effects, and diagnostic analysis (FMEDA) and defined for each safety goal (figure 1):

FTTI > Diagnostic Test Interval (DTI) + Fault Reaction Time Interval (FRTI)

As the complexity of automotive electronic devices continues to increase, using structural testing becomes more critical, however by nature of the designs the
overall testing of the structural test is becoming longer. This can cause the structural test time to exceed the DTI

and hence as there is often little control over the FRTI. This has a direct impact on the FTTI.

If an FTTI exceeds the safety goal, it then impacts the ability to achieve the required ISO 262626 certification level required for a given product. This paper describes a new logic BIST technology that can capture test responses from the circuit during scan shifting called Observation Scan Technology (OST). OST was developed to improve logic BIST (LBIST) test quality and reduce in-system test time. Empirical results gathered from industry designs show that LBIST-OST enables 90% test coverage with up to 10X fewer LBIST patterns when compared with previous industry-leading LBIST solutions.

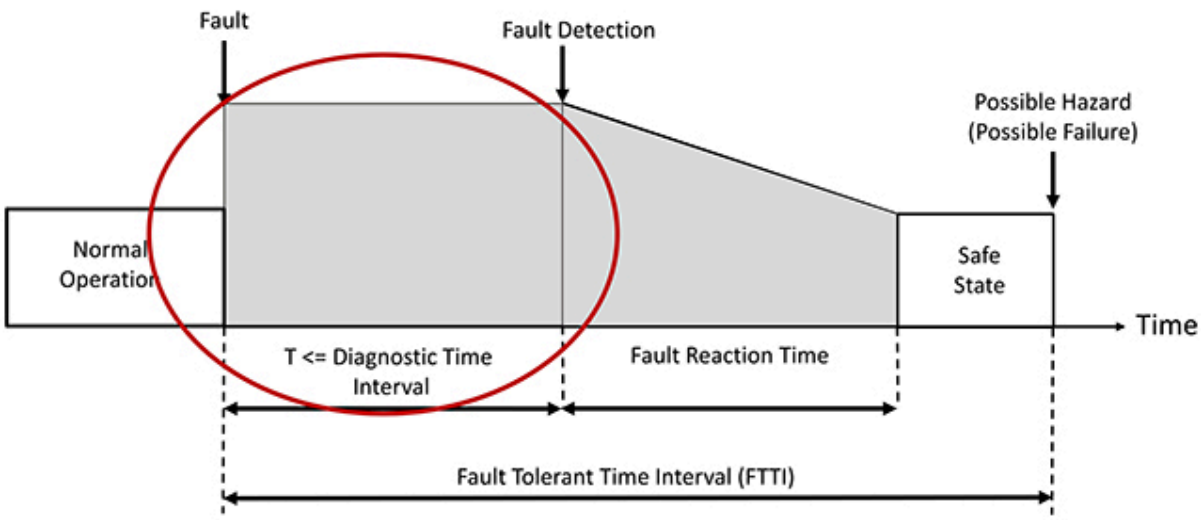

Figure 1: Fault reaction time and fault-tolerant time interval. FTTI > diagnostic test interval + fault reaction time interval.

Logic BIST for safety-critical devices

Logic BIST is an established technology for enabling in-system test of semiconductor devices that have to meet strict safety-critical requirements [1]. Tessent offers a hybrid TK/LBIST IP that shares many of the same logic structures, which reduces silicon area needed for test circuitry [2, 3]. This allows Tessent TestKompress (TK) and Tessent LogicBIST to work concurrently. There is a large body of experimental evidence that indicates that the TK/LBIST hybrid scheme results in the shortest

test time and high coverage, on par with the best hybrid implementations. This is because of common elements that LBIST and TestKompress contain.

With LBIST used as an in-system test solution, the challenge is to meet test coverage requirements for increasingly larger designs and do so within the allocated test time. This is becoming harder, as typically the number of LBIST patterns required is higher than ATPG, due to the randomness of the generated patterns.

The challenges of addressing the strict requirements of in-field and in-system test (IST) are seen extensively when using Tessent LogicBIST for an automotive application. LBIST must run periodic tests during the functional operations with a test time defined by the safety requirements as described above. A typical automotive application for a vehicle could see a required test time between 5 and 50 milliseconds, which is more due to the small time interval granted by the IST rather than the safety goal requirement. Other restrictions include power constraints, which could increase the LBIST pattern count and the ASIL-D latent fault metric requirement for logic BIST to achieve 90% stuck-at fault coverage.

Observation Scan Technology

The requirement of having a very short test time remains orthogonal to what the state-of-the-art logic BIST tests can achieve. Although, with a direct access to the IC's memory elements, scan makes it possible to generate high quality tests. Test time is nearly 100% spent on shifting as almost all memory elements for shift registers in a test mode.

To shorten the test time interval, Tessent LogicBIST with OST [4] adds observation points into the design that can capture faults every shift cycle. The LBIST-OST architecture is shown in figure 2. These fault effects can then be captured into dedicated observation scan-flops that form a dedicated observation scan chain. Silicon area used by LBIST-OST is kept to a minimum

by sharing the flip flops between a number of these observation test points.

To reduce external test data volume and pseudorandom pattern count, the observation scan chains are continuously shifted into the compactor, which drives the MISR signature generation. These observation scan chains are also shared with traditional LBIST scan chains, delivering responses once the entire test pattern has been shifted-in. It's worth noting that the selection of the optimal number of test points to elevate the random-pattern test coverage follows a procedure presented in [2].

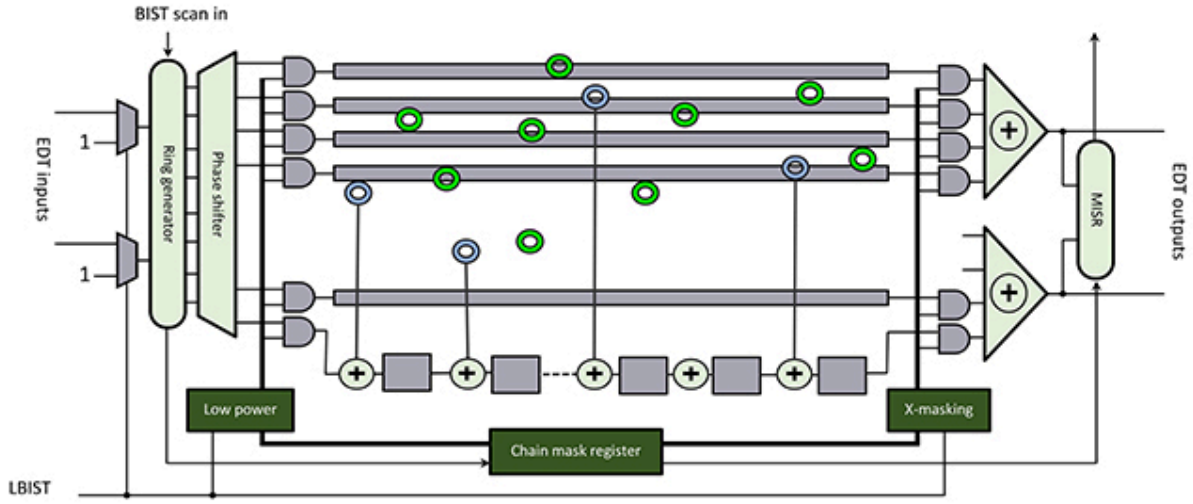

Figure 2: Hybrid TK/LBIST architecture with observation scan.

Modified scan cells serving as observation points are arranged into observation scan chains to accumulate test response using additional logic added to these dedicated scan cells. It allows an encapsulation of shift and capture functionality with a single clock cycle. A complete scan cell design is shown in figure 3.

It consists of a 4-input multiplexer that selects the data source for a D-type flip flop based on two control inputs; M1 and M2. It is worth noting that M1 behaves like a conventional scan-enable signal whereas M2 decides whether to accumulate responses during shift or capture.

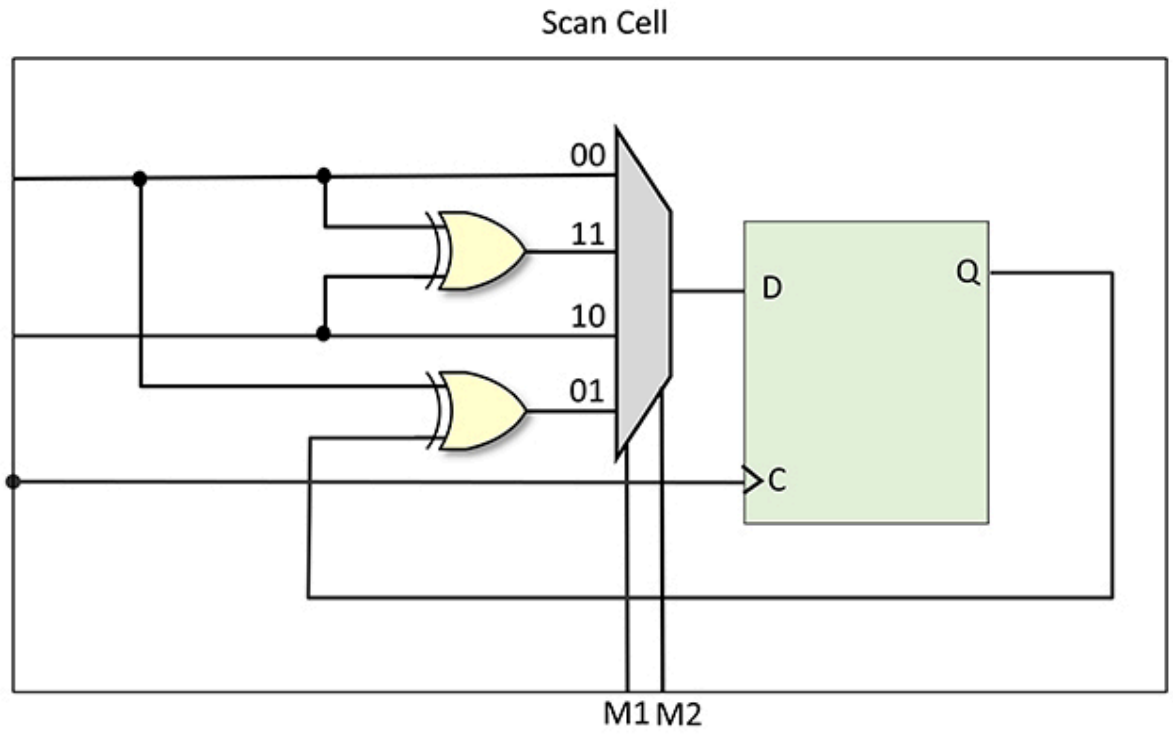

Figure 3: Observation scan cell design.

If M1 and M2 are set to 00, the scan cell enters the mission mode, i.e., it captures every clock cycle. Compaction mode is when both M1 and M2 are set to 11. When the M1=1 and M2=0, the flip-flop is connected to the previous scan cell. When M1=0 and M2=1, the scan cell is moved to the capture mode where the data from the test point is captured. During capture mode, the scan element not only captures the output of the test point, but it accumulates it with the existing state of the scan element. This is needed to ensure that the fault effects captured in the observe points during shift are not overridden during the capture cycles.

Modes	M1 (=SE)	M2	D	St	Q
Shift	1	0	d	s	s
Shift	1	1	d	s	d + s
Capture	0	0	d	s	d
Capture	0	1	d	s	d + q

LBIST-OST analysis and insertion flow

The design implementation flow with LBIST-OST is almost identical to that of traditional logic BIST. In the Tessent flow, when a DFT specification is used within Tessent Shell to create and insert the RTL-based test logic, a dedicated DFT signal is used to control the capture of responses during shift. This signal can be turned off dynamically as needed. Fault simulation considers the value of DFT signal prior to simulating shift cycles. Two new design rule checks validate the correct structure of the observation scan cells.

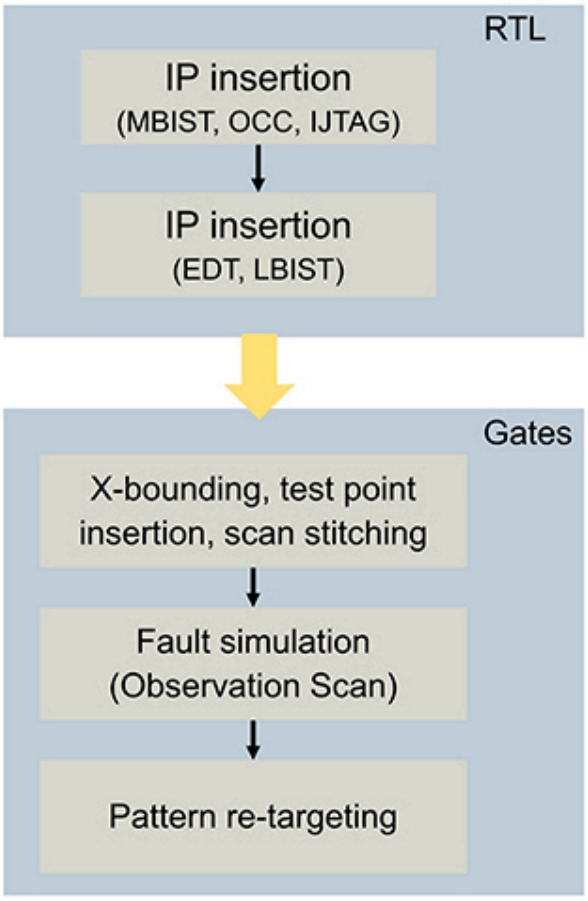

Figure 4: LBIST with Observation Scan Technology insertion flow.

Within Tessent Shell there is a unified context to perform test point insertion, x-bounding, and scan stitching in the same run, enabling a single-pass flow for the gate-level logic insertion (figure 5). During the insertion of the LBIST-OST logic, observation scan cells are stitched in separate chains, not mixed with regular scan cells, and observation points are not inserted in cross domain paths.

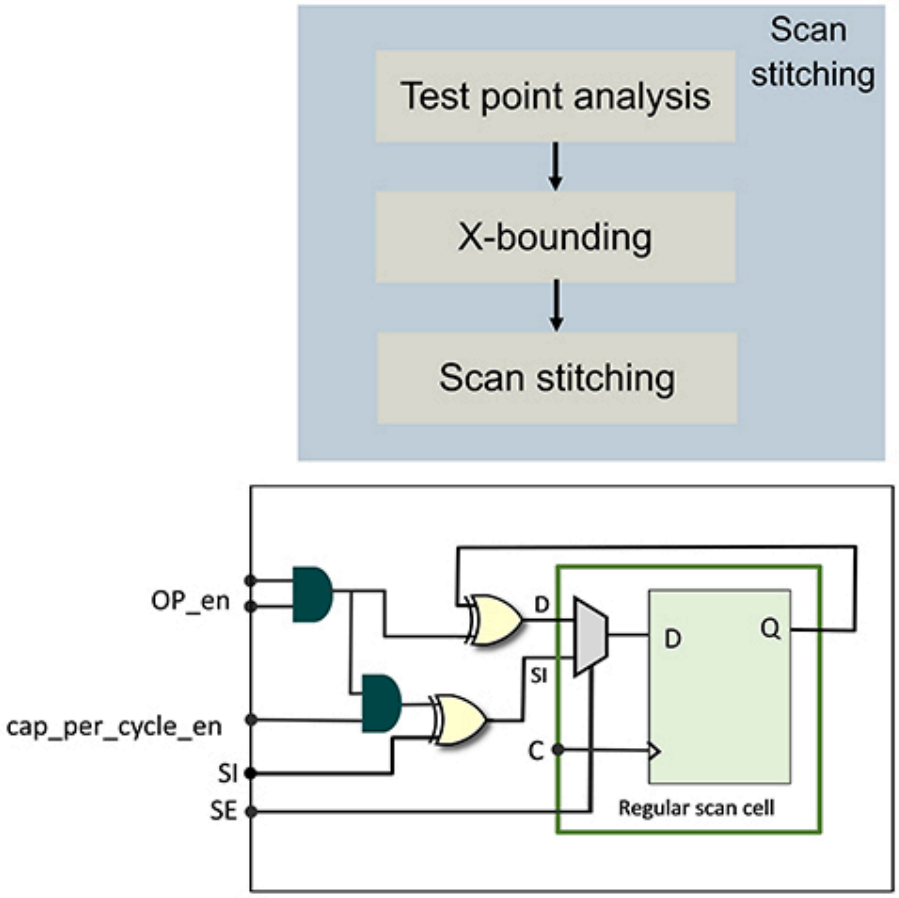

Figure 5: Unifed context for testpoint , x-bounding and scan stitching

During this unified singlepass insertion, the dedicated scan cells used for the capture-per-cycle function are added along with discrete cells to implement the correct behavior, so there is not a requirement for a custom observation scan cell model. Also these are not mixed with regular scan cells within the design.

Results

Tessent LBIST-OST test points have been inserted on a number of industrial

designs [3-5], producing the empirical data shown in the following tables. The key results are reductions in pattern count at 90% LBIST SAF coverage, based on adopted ISO 26262 requirements, and increases in test coverage for high-quality in-system test applications. This provides a viable solution for scenarios where a shorter test time is required, such as power-on-self-test and periodic testing, where a device may only be taken off line for a very short time during functional operation.

We performed experiments on 10 designs ranging in size from 1M to 14M gates, with 44K-900K scan cells, and 200 – 3,200 scan chains. The details of these designs are shown in table 1.

Table 2 is presented with three sections:

• The baseline test coverage without any test points.

• Coverage gain with the addition of traditional test points, both control and observe.

• Coverage gain with the addition of both traditional and observation test points.

As shown in table 2, test coverage (TC) improves significantly with the addition of LBIST-OST over what can be achieved with traditional LBIST, with counts of control points (CP) and observe points (OP). On average, we see a 14% coverage improvement when applying 16k patterns to our design data.

Table 1 – Experimental design parameters.

Design	Gates	Scan cells	Scan chains	Longest chain	Stuck-at faults
D1	1.2M	44K	196	231	2,049,104
D2	1.3M	86K	203	435	3,455,172
D3	956K	53K	279	190	2,495,198
D4	2.6M	194K	817	242	3,497,404
D5	6.6M	295K	1,236	242	11,834,546
D6	3.7M	207K	900	237	10,175,700
D7	14.2M	899K	3,163	291	37,265,306
D8	1.3M	77K	1,200	65	3,839,431
D9	1.3M	78K	1,200	66	3,885,239
D10	3.2M	145K	2,400	61	10,484927

Table 2 – Test Coverage improvements with 16k patterns.

Design	Baseline	Baseline + test points				Baseline + testpoints + Observation Scan			
	TC (%)	CPs	OPs	TC (%)	TC gain (%)	CPs	OPs	TC (%)	TC gain (%)
D1	**80.20**	347	603	88.87	**5.67**	443	507	90.74	**7.45**
D2	**71.81**	850	1,726	85.47	**13.66**	1,265	1,347	91.54	**19.73**
D3	**75.09**	1,340	1,430	89.04	**13.95**	1,483	1,287	90.30	**15.21**
D4	**85.08**	1,719	2,254	93.50	**8.42**	2,048	1,889	94.19	**9.11**
D5	**78.85**	3,133	2,799	92.08	**9.69**	3,393	2,539	92.42	**10.03**
D6	**78.85**	1,987	2,348	91.95	**13.10**	3,128	1,207	94.46	**15.61**
D7	**84.66**	9,163	9,710	95.61	**10.95**	12,052	6,821	96.62	**11.96**
D8	**77.85**	638	1,057	88.77	**11.19**	253	1,442	91.13	**13.55**
D9	**77.30**	547	1,180	88.24	**10.94**	258	1,469	90.93	**13.63**
D10	**64.63**	1,402	18,29	87.75	**23.13**	902	2,329	91.89	**27.26**

Table 3 shows results with emphasis on the pattern count required to achieve a target test coverage. With OST, the number of LBIST patterns needed to achieve the required 90% stuck-at test coverage was reduced by up to 16X.

Obviously the results vary based on the design, but the typical gain can be seen to be around a 10X reduction.

This study also emphasized another advantage of this technology: Comparing LBIST-OST to previous technology, the coverage and test time goals can be met with a smaller number of test points (0.5% rather than 2%), reducing the overall silicon overhead.

Table 3 – Pattern count reduction at 90% stuck-at test coverage.

Design	Total test points	Baseline + test points pattern count @ 90%TC	Baseline + TP + Observation Scan		Baseline + TP + Observation Scan (CP sharing)	
			PC @90% TC	PC reduction (x)	PC @90% TC	PC reduction (x)
D1	950	52,992	3,200	16.56	3,648	14.53
D2	2,612	65,536	3,456	18.96	34,56	18.96
D3	2,770	49,920	7,680	6.50	11,264	4.43
D4	3,973	1,920	448	4.29	448	4.29
D5	5,932	2,624	896	2.93	896	2.93
D6	4,335	5,568	1,600	3.48	1,600	3.48
D7	18,873	1,152	384	3.00	384	3.00
D8	1,659	67,072	5,760	11.64	6,,080	11.03
D9	1,727	92,352	6,848	13.49	6720	13.74
D10	3,231	38,784	5,376	7.21	5,504	7.05

Summary

Tessent LogicBIST with Observation Scan Technology represents the best in-system test solution for ICs targeting automotive applications, enabling a dramatic reduction of in-system test time. The amount of reduction in test data volume and increase in BIST coverage will depend on the number of observation points added to the circuit and on the design characteristics. It is generally accepted that ISO 26262 requires 90% coverage during in-system test. Empirical results have shown the need for up to 10X fewer patterns to reach 90% LBIST SAF coverage with LBIST-OST when compared to previous-generation LBIST test point technology.

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[1] L. Harrison, J. Wiltgen, “Using Built-In-Self-Test Hardware to Satisfy ISO 26262 Safety Requirements.”

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