DIGITAL INDUSTRIES SOFTWARE

Facing a new age of challenges in IC design

Executive Summary
Siemens is introducing three new platforms as RTL designers, software coders, and system-level engineers must collaborate to create today's electronic products and semiconductors. As the RTL design team create and verify the chip design, software teams develop and test driver, operating-system, middleware, and application code and integrate them with the chip design and board-level hardware. All proceed concurrently. One platform cannot optimally meet all three of these sets of needs. Each verification system must meet the stringent and unique requirements to support today's massive designs. Most importantly they must all share much of their DNA.

Introduction

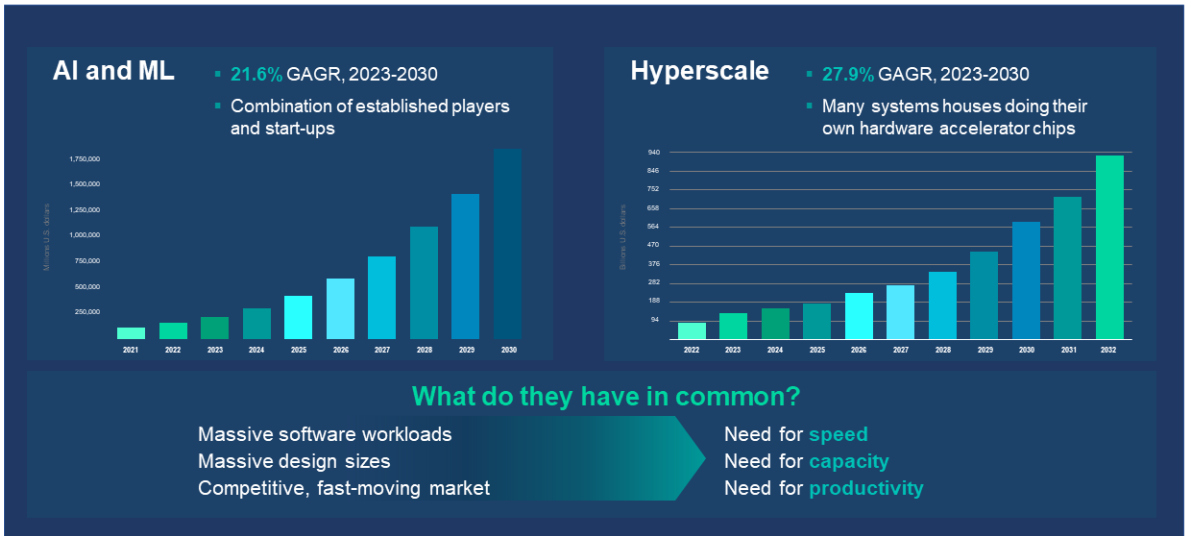
The scale of IC designs has increased enormously, driven by a leap in demands of a few key applications: datacenter CPUs and GPUs, and artificial-intelligence (AI) accelerators. In that latter case, exploding training demands for generative AI models and the beginnings of research into general AI shows an insatiable appetite for hardware.

The industry has been able to respond because of new IC manufacturing process generations—3nm and 2nm—promising enormous gate counts along with multi-die modules, some comprising dozens of dies. Design teams want to treat all the RTL for these dies as if they were single monolithic chips, pushing equivalent gate counts of new designs even beyond the reach of a single 2nm die. We are entering an era of chip designs encompassing the equivalent of tens of billions of gates.

Siemens simultaneously announced three closely related IC development platforms: an emulation system, Veloce Stratos CS; an enterprise-scale prototyping system, Veloce Primo CS; and an at-speed prototyping system, Veloce proFPGA CS. In an industry accustomed to incremental change, this raises a vital questions: why three platforms now?

A new landscape

All three categories have existed for years and are available from multiple sources, including Siemens. Four areas, all with major recent changes, dramatically improved value propositions: design scale and complexity, the significant role of software in defining hardware, the physical environment where chips are designed, and the technology that underlies the Veloce systems.



Software rising

At the same time, the size and complexity of software stacks have grown faster than the hardware, a result of the companies creating the most advanced IC designs.

Many advanced ICs today are designed by systems houses—cloud service providers, telecom giants, automotive manufacturers, aerospace companies—for a specific application. The IC is not the product. The system, including the full software stack, is the product that the design team must verify.

The two branches of development—RTL for hardware, and software for the system functionality and applications—must proceed in parallel. Early in the design, most of the effort is already going into software design and debug. At this point, two-way communications between the RTL and software teams is imperative and many new tools and methodologies are being development to simplify this somewhat difficult change. Difficult because in the past methodologies have not been intuitively connected.

Early two-way communication between RTL and software teams was part of the technology to build the Veloce CS system, a system that is significantly different than our previous generation of systems. The FPGAs in the Veloce Primo CS and Veloce proFPGA CS prototyping systems, and the purpose-built custom accelerator we designed for the Veloce Strato CS emulation system, have far higher capacity, greater speed, and lower power consumption than previous generation chips. We exploit 2.5D multi-die module technology and optical interconnect as well. Datacenters and high-performance computing platforms have driven these advances, and we applied them.

Three distinct challenges

Now is the time to introduce three new systems at once as RTL designers, software coders, and system-level engineers must collaborate to create today's electronic products and semiconductors. As the RTL design team create and verify the chip design, software teams develop and test driver, operating-system, middleware, and application code and integrate them with the chip design and board-level hardware. All proceed concurrently.

Each set of tasks has distinct needs. The RTL development team works with the IC logic design while it is most fluid, designing and verifying at the level of individual logic signals. At least initially, they make frequent changes to both the design itself and their testbenches, stressing compile and configuration times. In contrast, the software team barely cares about the RTL design except to determine whether the root cause of a bug lies in the hardware or software. They need a fast execution platform for their code—one that represents the current design of the full chip with enough speed to boot operating software and run meaningful portions of real applications—potentially hundreds of millions of instructions.

System designers need to examine a specific interaction between the chip, the software stack, and the external world looking for time-dependent bugs that can only be observed at or near real-time operation of the prototype. Typically, they inspect how a particular portion of the chip—say, one computing element or a DMA controller—interacts with a bus interface and with the peripherals on that bus when a particular portion of an application is running.

One platform cannot optimally meet all three of these sets of needs. Each verification system must meet the stringent and unique requirements to support today's massive designs. Most importantly they must all share much of their DNA.

Continuous communications

In practice, while the three teams are conducting different activities, information flows back and forth continually between them. The chip team must ensure the others are working with the most current version of the RTL model. The software team and system team must notify the chip team of suspected hardware bugs and change requests.

If the three platforms differ in their user interface, in the way the RTL model is represented, or in the way they collect and store data, interactions are inefficient, and perhaps counterproductive. One version of the RTL model must produce the same behavior on all three platforms. The greatest risk is that the models used by the three teams diverge—a catastrophe that may not become apparent until silicon bring-up.

One command language. One design model. One database. That is why we designed the Veloce CS system with its three platforms together, and why we are introducing all three at once.

Specific needs and answers for them

While Veloce Strato CS, Veloce Primo CS, and Veloce proFPGA CS are united by common user interface, RTL models, and database, each platform must meet the demands of its role in the verification process.

Capacity is a principal requirement imposed by today's advanced IC designs. Both the emulation and enterprise prototyping systems must be able to hold the entire compiled RTL model for the chip to observe real workload execution. Through advanced ASIC processes and advanced FPGAs for prototyping, use of high-speed interconnect, and a modular architecture, Veloce Strato CS and Veloce Primo CS have fine-grained, plug-in scalability from entry-level up to the equivalent of 40+billion gates.

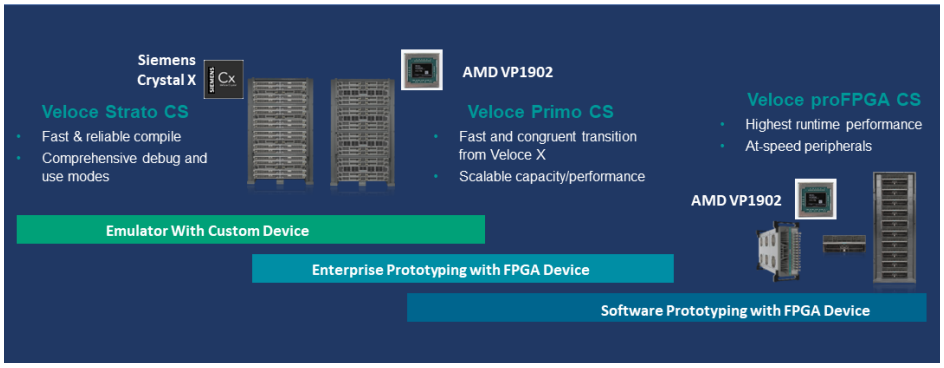
The twin of capacity is speed—performance to exercise an entire chip design and execute real workloads in minutes, not months. Veloce Strato CS exploits its new purpose-built custom accelerator chip and interconnect technologies to reach speeds significantly higher than those of alternative systems. Veloce Primo CS uses advanced FPGAs and interconnect to give it execution speed many times greater than even that of Veloce Strato CS.

Large models also require fast compilation. Developing our RTL model compilers in parallel with the internal architectures of Veloce Strato CS and Veloce Primo CS, we accelerated compilation times and avoided problems that can dramatically slow compilation. When the RTL model needs to change, recompilation is fast.

Observation and control

Another principal need is fast, understandable trace and trigger operation and it must be represented differently in the two platforms. Accordingly, Veloce Strato CS makes all signals in the model available to trace, trigger, or breakpoint commands. The FPGA-based Veloce Primo CS and Veloce proFPGA CS platforms require access to individual signals specified when the model is compiled. Software developers get the added speed of the FPGA-based architecture in exchange for less convenient means of changing their access to logic-level signals.

Processes for compiling the RTL model for Veloce Strato CS and Veloce Primo CS are nearly identical: a switch directs the compiler to one platform or the other, while the model stays the same. Veloce proFPGA CS uses the same RTL model, usually only a portion of the full model would be compiled for any experiment, an underlying concept we call congruence. An RTL model compiles to produce the same behavior in each platform, just at different execution speeds and levels of observability even though the compiled code is different for each platform. The same user command produces the same result on Veloce Strato CS and Veloce Primo CS, and on Veloce proFPGA CS when the context makes sense. This lets teams share a single RTL model, to work together or separately, and communicate efficiently for higher integrity of the design and schedule.



Making shareability work

We can relate many of the features of the Veloce CS system three platforms directly to the needs of verification teams working on leading-edge ICs. Their enterprises have needs too—first, shareability. It is fundamentally important that these platforms are sharable between members of the same project and across enterprises. Sharing must be natural and easy—not an added chore for design teams or a nightmare for IT managers. This ability to share—efficiently—systems on this scale has several design implications.

One important aspect of shareability is software configurability. Different teams are working on different RTL models of different sizes. This capability is a given for emulation platforms. For enterprise prototyping platforms, configurability via software comes at a cost. Speed of the links between FPGAs is critical to overall system

performance. Traditionally, the fastest links are hard-wired, or pluggable cables. Both inhibit flexibility. Allowing a design team days of access to an enterprise prototyping system in a remote datacenter to reconfigure cables is impractical for logistical and security reasons creating conflict between the need for interconnect flexibility with remote configuration capability, and system performance.

At Siemens, we cultivated several generations of high-performance software-configurable interconnect technology to address this problem, allowing Veloce Primo CS to offer full remote, closed-box reconfiguration on scaled-out systems while maintaining excellent performance.

Along with configurability comes granularity, an issue for energy and capital efficiency. Designers don't want to install and operate twice the capacity needed because the RTL model grew slightly larger. Accordingly, we designed all the Veloce CS systems to scale with the finest granularity in the industry from 40 million gates in a single blade to 40+ billion gates in a series of fully loaded racks.

Fitting in

Finally, shareability means that the shared Veloce Strato CS and Veloce Primo CS platforms drop seamlessly into modern enterprise datacenters. They comply with the footprint standards for datacenter racks, using standard cabling conventions for power and networking and limit power density for air cooling using the datacenter's lateral-flow air movement and standard hot-isle/cold-isle layout.

Veloce proFPGA CS, can be used in a datacenter or in a lab or benchtop orientation where it is wired into a prototype circuit board and peripheral devices.

The value of three

Siemens EDA recognized the discontinuity triggered by the convergence of new, AI-related hardware needs, new process technology, and the emergence of chiplet-based large systems. With the Veloce CS system, we responded—creating three new, economical, scalable platforms addressing the new needs of design teams.

Our Veloce CS system is instrumental in creating the next generation of advanced ICs and multi-die modules, bringing new levels of productivity to engineering teams, new levels of integrity to designs and to schedules, and a new value proposition to the enterprises—be they IC vendors, IP houses, or systems developers—transforming these advanced IC designs into earnings growth.

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