SIEMENS
Ingenuity for life

Tessent FastScan

Automatic test pattern generation

Benefits

- Highest test quality with a very low pattern count.
- Supports all common scan architectures and design styles.
- High throughput through high performance pattern generation and automated debugging.
- Award-winning customer support and consulting services.

Features

- Extensive fault model support, including stuck-at, transition, cellaware, N-detect, timing-aware, bridge, IDDQ, path-delay, and user-defined.
- On-chip PLL / OCC support ensures precise at-speed test.
- Support for any common scan implementation. Fully integrated with Tessent Scan / ScanPro.
- Multi-processor ATPG reduces runtime without impacting coverage or pattern count.
- Effective handling of false and multi-cycle paths.
- Comprehensive design rule checking and testability analysis.
- Powerful Tessent Shell scripting environment for automation, introspection, and integration.

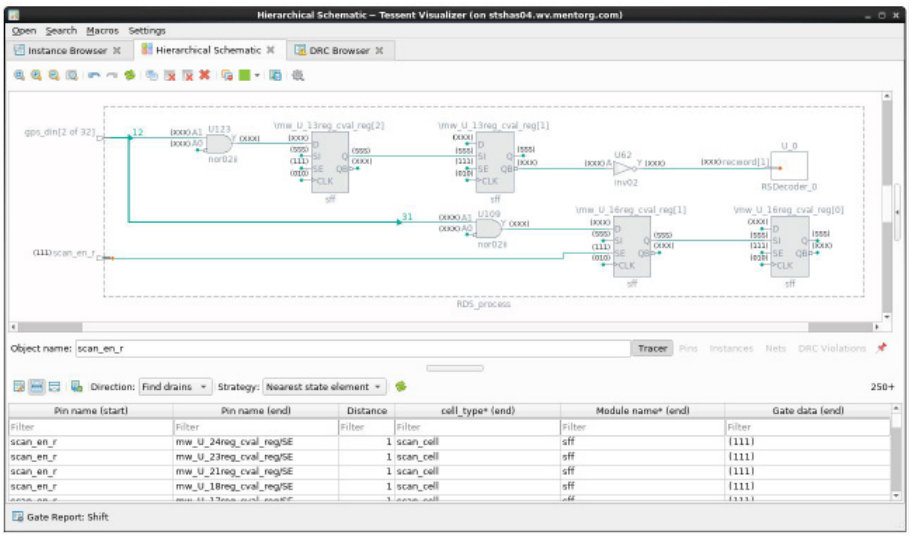
Industry leading ATPG solution

Advanced design techniques used in today's SoCs present significant challenges to achieving high-quality silicon test. Tessent™ FastScan™ is the gold standard in automatic test pattern generation (ATPG), with support for a wide range of fault models, comprehensive design rule checks, extensive clocking support, and innovative algorithms for performance-oriented pattern compaction. Its ability to be applied to any type of design makes it the most versatile ATPG solution available. Tessent FastScan is part of the Tessent Shell platform, which offers extensive capabilities for automation, customization, testability analysis, and debug.

High test quality

Tessent FastScan supports all traditional fault models used for uncovering both static and dynamically activated defects. Timing-aware test uses SDF to ensure that the long paths in the design are tested.

Support for user-defined fault models (UDFM) also allows virtually any defect mechanism to be modeled and targeted. While traditional fault models only consider faults on cell inputs and outputs and on interconnect lines between these, Tessent FastScan's cell-aware test targets defects inside the standard cells.



Tessent FastScan combines the industry's most effective ATPG engine with the powerful debug and analysis capabilities of Tessent Visualizer.

Tessent FastScan

Features *continued*

- ATPG Expert analyzes your design to optimize test coverage and pattern count with shortest runtime.
- Automatic simulation mismatch debug reduces test validation time.
- Links to Tessent Diagnosis and Tessent YieldInsight for defect and yield analysis.

Cell-aware test leverages a unique fault model that is created using a process that extracts shorts, opens, and transistor defects based on the Spice model of the cell. The optional Automotive-grade ATPG targets critical-area based fault models for bridge and open interconnect as well as cell-neighborhood (intercell) faults to detect bridge defects between cells.

High test quality is more than just fault models, it is also about minimizing the impact of unknown states in the design. False and multi-cycle paths are analyzed effectively to minimize the impact on test coverage.

Flexibility

Tessent FastScan supports any design flow and any common structured scan architecture. Unlike other tools that require a specific set of homogenous EDA tools for operation, Tessent FastScan is designed to work in all design environments using any combination of synthesis, place-and-route, and verification tools. When the scan structures are created using Tessent Scan or Tessent ScanPro, setup information for Tessent FastScan is automatically imported for the desired scan mode. Tessent FastScan also recognizes scan setup information from other scan insertion tools in industry standard IEEE 1450 STIL format.

To ensure reliable at-speed test, Tessent FastScan supports on-chip PLLs and OCC, whether inserted by Tessent ScanPro or other tools.

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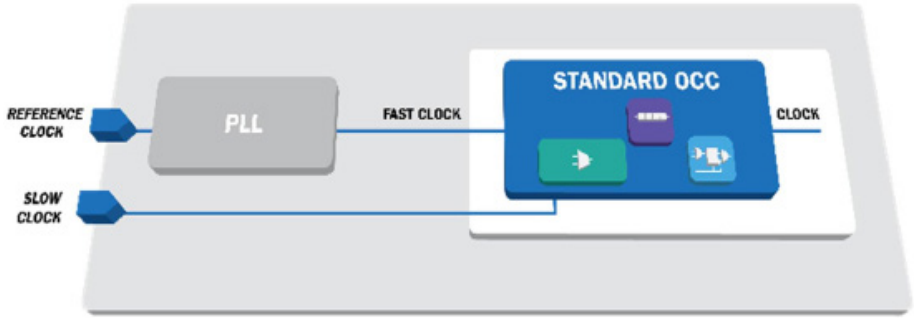
Productivity

Tessent FastScan is built on the Tessent Shell platform, which offers powerful TCL-based scripting, automation, and introspection.

Tessent Visualizer is the common debug environment integrated within Tessent products, including Tessent FastScan, for fast root cause analysis of DRCs and addressing testability problems. The intuitive user interface of Tessent Visualizer is designed to address key challenges of the most time-consuming DFT debug tasks.

Tessent Visualizer's ATPG statistics analysis and powerful tabular reporting pinpoint test coverage loss issues to specific design areas and characteristics in order to accelerate troubleshooting.

The innovative interface for finding and tracing to objects in large cones of logic results in significantly faster tracing and contributes to increased productivity. Tessent Visualizer is designed to handle billion-gate designs for quick search and display of design in various views such as schematics, tabular data, library cells, and DRCs to facilitate automated troubleshooting.



Tessent FastScan can leverage on-chip PLL and on-chip clock control for reliable at-speed test.

Tessent FastScan

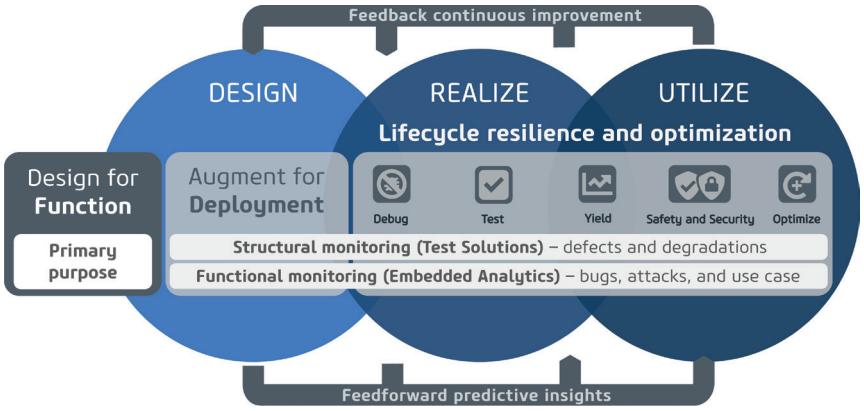
Test Pattern Compaction

Tessent FastScan is known for delivering high-coverage, compact test sets. The integrated ATPG Expert automatically optimizes coverage and pattern count with shortest run time. It monitors progress, learns, and adjusts during your ATPG run.

With the growing need to improve test quality with at-speed and cell-aware patterns, the amount of test data can still be an issue. In these situations, Tessent TestKompress™ with embedded deterministic test (EDT) technology can be used to provide the most compact pattern set. Both tools use the same efficient ATPG engine.

Tessent silicon lifecycle solutions

Design augmentation and linked applications that detect, mitigate and eliminate risks throughout the IC lifecycle, helping customers address their debug, test, yield, safety, security, and optimization requirements for today's most complex SoCs.



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