

The background of the slide is a landscape featuring a town, green fields, and wind turbines under a sunset sky. Overlaid on this are several digital elements: a line graph, a complex circuit board layout, and a schematic diagram with various symbols like 'G', 'P', and 'M'. A blue rectangular box is positioned in the lower right of the landscape, containing the main title. The Siemens logo and tagline are in the top left corner.

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Validating rule-based parasitic extraction against a field solver solution

Executive summary

Foundries and EDA vendors must ensure that their PEX rule decks provide accurate extraction. Design companies must ensure the accuracy of their rule-based PEX tool. Correlating rule-based PEX results against a field solver extraction provides reference numbers they can trust, as long as they set up the runs properly to ensure an “apples to apples” comparison.

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Introduction

Rule-based parasitic extraction (PEX) engines use tables or equations that are calibrated from field solver calculations. However, both circuit designers and foundry modeling engineers encounter situations where they need to compare and validate their rule-based PEX results against a proven “golden reference.” Designs can include many structures that the rule-based PEX engine fractures into pieces that correspond to the models on which it was trained, then measures the actual sizes and uses extrapolation and interpolation to calculate the corresponding parasitic resistance and capacitance. Engineers must be able to validate these results against a field solver solution to ensure the results are accurate in production.

For example, during the qualification of a foundry rule deck, foundry modeling engineers use correlation to ensure the extraction rule decks they deliver will work correctly with electronic design automation (EDA) tools. Design companies often run a PEX correlation in new technologies before creating real designs, by creating simple designs (such as a voltagecontrolled oscillator or ring oscillator), running rule-based extraction, then comparing the results to the field solver results.

Actual silicon measurements are always the ideal golden reference. Foundries often use fabricated integrated circuits (ICs) that include many shapes, while design houses may actually fabricate a special test structures die just for this purpose. However, physical measurements are not always easy to come by, due either to a lack of measurement data, or because the structures under test are difficult to measure. Even foundries, who have better access to silicon measurements, don't always have that option.

In such cases, correlating rule-based PEX results against a field solver extraction is a good option that engineers can rely on to provide reference numbers they can trust. However, there are a number of common issues that they may experience while performing the comparison, and they don't have anything to do with the accuracy of the rule-based extraction engine. By being aware of these issues, engineers and designers can modify the setup and use of both PEX processes to ensure the results can be fairly and accurately compared.

Field solver parasitic extraction

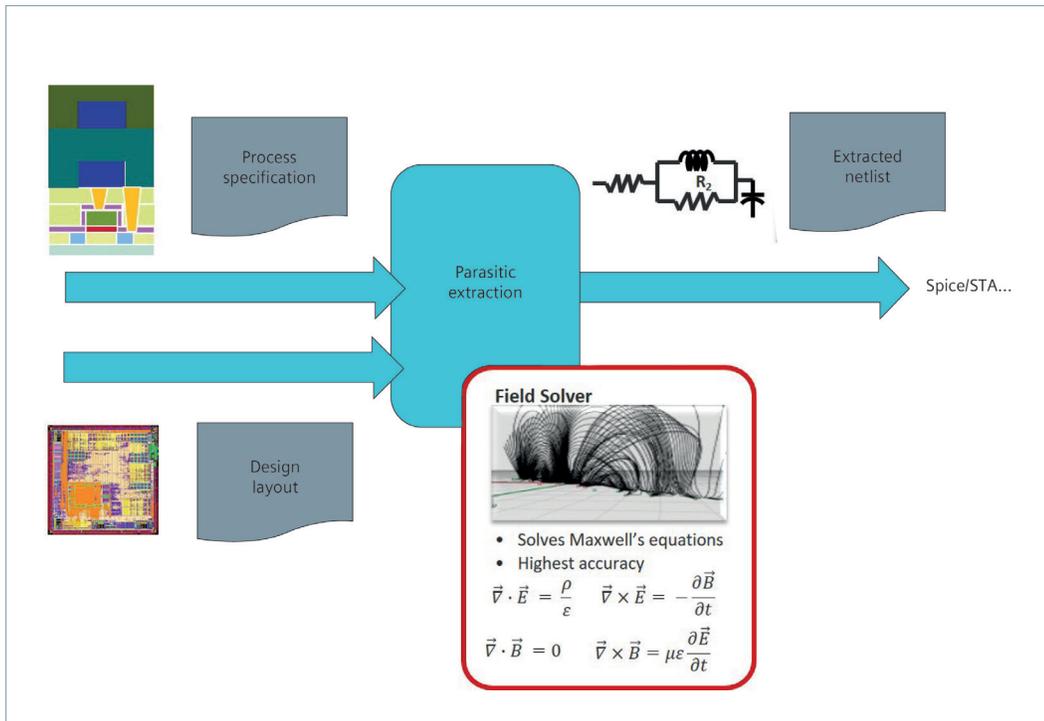


Figure 1: Field solver PEX flow.

Field solver-based PEX tools provide a precise and complete mathematical solution for parasitic extraction by solving Maxwell's equations. Because field solvers can handle complicated three-dimensional geometries, they generate highly-accurate extracted netlists (figure 1) that are typically used to generate the golden reference results needed to validate the accuracy of rule-based tools. Field solvers are not restricted to a pre-defined model of the parasitic effects that may or may not arise in any given design, and they don't require a model calibration step, because they work directly with the design layout.

Field solver PEX is used sparingly in real designs because it requires significant runtimes. In addition, field solvers can be difficult to set up for accurate construction of a three-dimensional description of the design layout containing all the physical parameters for each layer. While some EDA tools enable designers to run a field solver using the two-dimensional description of the design layout in the standard GDSII format, most design companies still use rule-based PEX for the majority of their extraction needs because it is faster and easier.

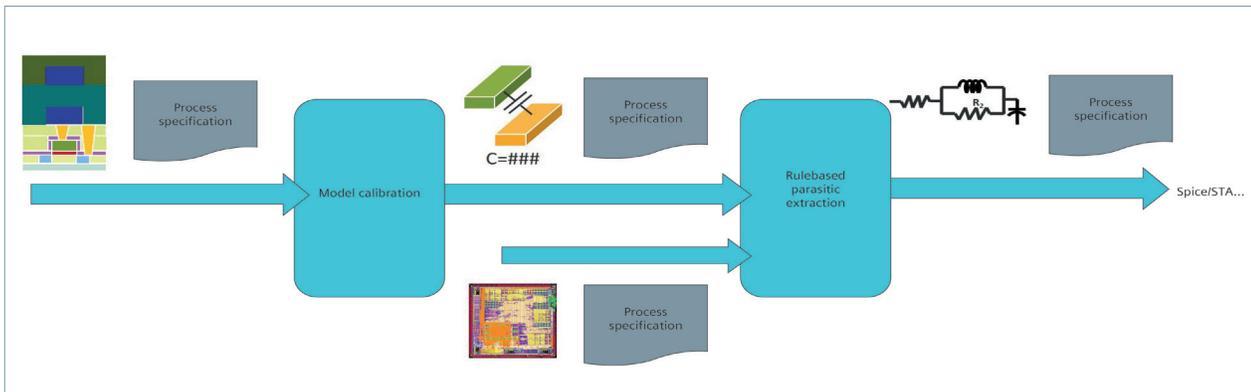


Figure 2: Rule-based PEX calibration and usage flow.

Rule-based PEX

A rule-based PEX tool reads a design layout using a two-dimensional description of the design's physical shapes (e.g., GDSII). It then identifies patterns in the layout that match a predefined set of models in the PEX rules, performs the calculations by substituting in the actual design dimensions, and writes an extracted netlist that includes the design circuit and its extracted parasitic components. This extracted netlist is used by SPICE circuit simulators and static timing analysis (STA) tools, and those results, in turn, are used to adjust or modify the design to obtain the desired performance and/or eliminate any operational issues.

Rule-based PEX calibration

The pre-defined set of structures in rule-based PEX engines are modeled by equations or tables. EDA companies select this superset to include the structures they believe will be used in actual designs. This selection is usually performed by modeling teams with extensive experience in both design and modeling techniques. However, before these rule-based PEX engines are delivered to users, they must be calibrated against a golden reference to ensure their accuracy for a given foundry technology node.

Development of a rule-based PEX flow begins with a process specification that describes what the set of layers (stack) in a given process technology looks like. For example, a stack specification starts by defining the height and properties of metal1, then the height and properties for metal2, and so on.

The syntax format used for this stack specification file differs from one electronic design automation (EDA) tool supplier to another, but they all must contain the necessary geometrical and electrical parameters for each layer in the stack. A combination of these layers with specific widths and spaces is then used to construct each pre-defined structure. The processstack is fed into a calibration engine, which generates the structures, runs a field solver against them, calibrates the pre-defined model equations for this stack against the field solver results, and generates the model equations in the form of extraction rules that can be understood by rule-based PEX tools (figure 2).

Rule-based PEX vs. Field solver correlation

When designers want to ensure the rule-based parasitic extraction for a specific design is accurate, they may choose to validate the extracted netlist obtained using rule-based PEX to the extracted netlist created by a field solver. However, to ensure the results are being fairly compared, the designer must ensure an "apples to apples" comparison. Certain design and setup conditions may skew the results, making a fair comparison impossible. To prevent this from happening, there are certain adjustments and modifications designers may need to make to ensure that the setup conditions of both engines are properly aligned if they want the correlation to be equivalent. In general, there are five issues that may affect the compatibility of the two sets of results.

DRC compliance

The design must be compliant with all design rule checks (DRC). Rule-based PEX tools rely on equations that are based upon some assumptions, giving them a limited range of validity. One of these fundamental assumptions is that the design is DRC-clean.

For instance, extracting a design that contains dimensions smaller than the technology minimum features creates inaccuracy in the rule-based engine results. Although this limitation does not apply to field solvers, which solve Maxwell's equations for whatever shapes are defined in the design, having a DRC-clean design during correlation is necessary to obtain an accurate comparison of results.

Capacitance ignore

Some capacitance components are already accounted for in the SPICE models during simulation, and should be ignored during extraction to avoid double-counting. To avoid extracting these parasitics, most rule-based PEX tools can be set up to "ignore" specific parasitic components. Because the rule-based engine uses a separate equation for different capacitance components (like fringe, plate, near body intrinsic/coupling capacitance components), designating a capacitance ignore allows you to easily drop one of those components while keeping the others (figure 3).

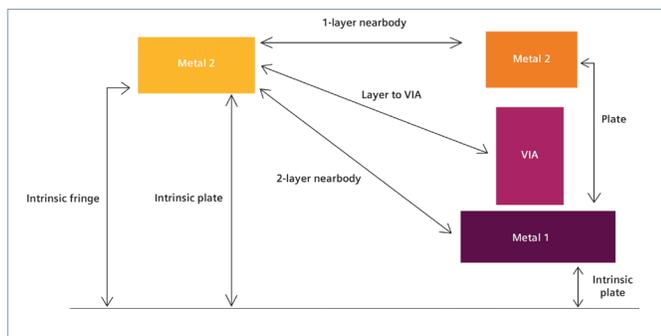


Figure 3: Typical capacitance components that can be removed individually from rule-based extraction using capacitance ignores.

While some field solvers can account for some of these capacitance ignores, ignoring a specific capacitance effect in a field solver is not as straightforward, because it calculates the capacitance as a lumped effect that can't be easily broken down into such components. To accurately correlate results, designers must either choose to remove all capacitance ignores from the rule-based PEX, or use de-embedding techniques to manually remove those components from the field solver PEX results.

In-die variation

Foundries usually use in-die variation data for interconnects to model post-fabrication variations in the process parameters, such as metal width, thickness, and resistivity. These variations depend on stack layer, layer width, spacing, and density. Foundry-qualified rule decks for rule-based PEX engines take this variation into account. However, not all field solvers can account for this kind of variation, so you may need to turn off in-die variation and/or layout magnification options in your rule-based PEX tool to ensure accurate comparisons. Alternatively, you can ensure the field solver input shapes use the actual post-fabrication layout dimensions in place of the drawn dimensions (figure 4).

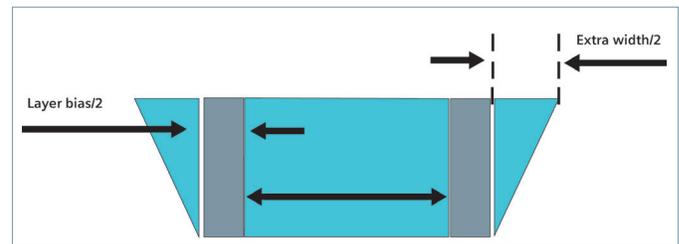


Figure 4: In-die variation accounts for differences between the drawn width of a shape and the actual size of the shape as manufactured.

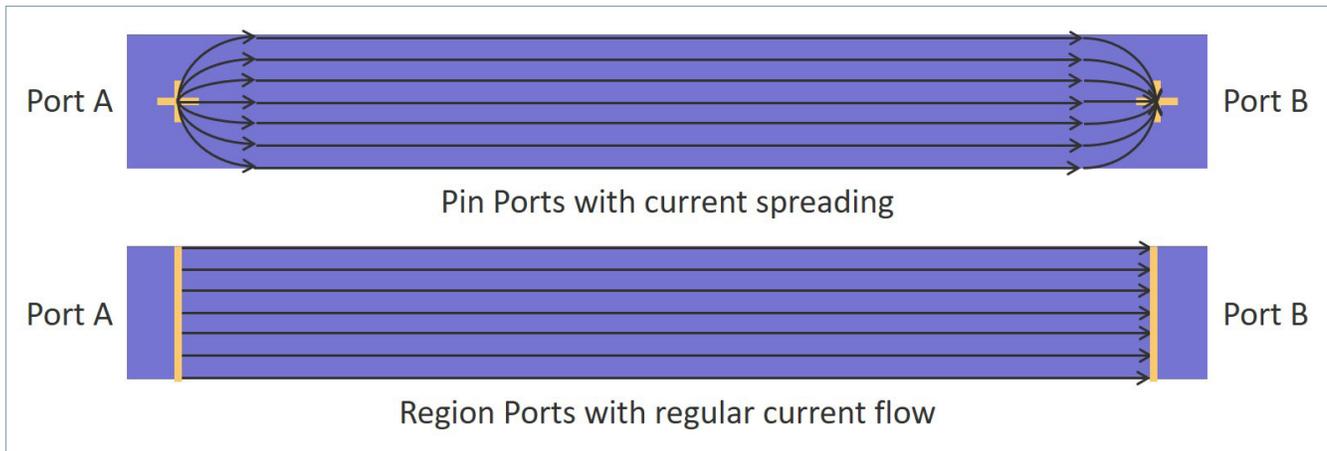


Figure 5: Pin ports must be replaced by region ports in field solver PEX to ensure accurate comparisons of port-to-port resistance.

PORT-TO-PORT RESISTANCE

Most rule-based engines model interconnect resistance in a single dimension. This approach enables port-to-port resistance calculation even when the port is defined by specific (x, y) coordinates in the layout, without having to worry about a current-spreading effect around these specific (x, y) coordinates on the interconnect. However, resistance calculations in field solvers are very much affected by current spreading, so when performing field solver PEX, regular ports must be replaced by region-based ports that are considered as infinite sources of charges regularly distributed along the interconnect width (figure 5).

MULTIPLE LAYERS

Multiple layers in the same physical location can cause inconsistency between rule-based and field solver PEX results. Rule-based engines usually calculate capacitance and resistance using pre-defined equations, even when they correspond to the same physical layer. If multiple layers correspond to the same physical layer, and none of them are ignored, this can cause double counting for rule-based results. A field solver can natively identify such duplicate geometries and treat them as one shape. Because this inconsistency can be caused by an incorrect setup for the rule-based PEX, it is essential to check the rule-based setup to ensure this double counting is eliminated.

Conclusion

Correlating a rule-based PEX engine against field solver PEX results is an important and critical process. Foundries and EDA vendors must ensure that the PEX rule decks they deliver will provide accurate extraction results when used in verification flows. Design companies need to ensure that moving to a new process node has not affected the accuracy of their rule-based PEX tool. When correlating your rule-based and field solver PEX results, it may take multiple iterations to ensure the two extraction flows are performing extraction in a compatible manner. However, this validation process is essential if you want an accurate comparison of results.

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