

DIGITAL INDUSTRIES SOFTWARE

Solido Design Environment

Comprehensive AI-powered design environment for nominal and variation-aware verification of custom IC circuitry

Benefits

Brute force-accurate signoff variation analysis, 1000X+ faster

- Orders of magnitude faster than brute-force simulation
- Full coverage verification across PVTs and Monte Carlo
- Brute-force Monte Carlo and SPICE accurate high-sigma verification
- Variation-aware design sensitivity, debugging and optimization

Comprehensive design environment

- Boosts engineering efficiency, producing more results for less effort
- Significantly reduces documentation time and effort

Introduction

Siemens Digital Industries Software is the leader in variation-aware design software for memory, standard cell, and analog/RF custom IC design. Solido Design Environment (Solido DE) is a comprehensive AI-powered design environment for all SPICE-level design and verification, and is a single unified solution for nominal and variation analysis. Solido DE is production proven and has already been used by thousands of designers to produce the most competitive products in high-performance computing, artificial intelligence (AI), internet of things (IoT), automotive and mobile application spaces. The solution helps meet aggressive low-power demands and adapts to the challenges of smaller, more advanced technology nodes without compromising product quality, yield or performance.

Using Solido DE, engineering teams can set up SPICE-level simulations for circuit measurements and regressions, as well as analyze waveforms and statistical results, all in a single cockpit that handles nominal and variation-aware analysis. The solution integrates AI technology seamlessly to perform production-accurate statistical yield analysis at a fraction of runtime compared to brute-force

Design Environment	PVT & Monte Carlo	High-Sigma	Design Optimization
<p>Nominal Simulation Comprehensive simulation setup</p> <p>Sweeps Powerful variable sweep management</p> <p>Corner Groups Fully configurable corner handling</p>	<p>PVTMC Verifier Fast and accurate verification coverage</p> <p>Fast PVT 2-50x faster verification across corners</p> <p>Monte Carlo 3σ verification & corner extraction</p>	<p>High-Sigma Verifier Next-gen high-sigma verification</p> <p>Hierarchical Monte Carlo Full-chip memory statistical variation</p> <p>High-Sigma Monte Carlo MC & SPICE accurate high-sigma verification</p>	<p>DesignSense Variation-aware design sensitivity</p> <p>Cell Optimizer Automated variation-aware cell-level optimization</p>

Benefits continued

- Automated trimming and calibration capability without the need for side scripts or VerilogA code

- Identifies design weaknesses undetectable by other methods

Easy to use and deploy

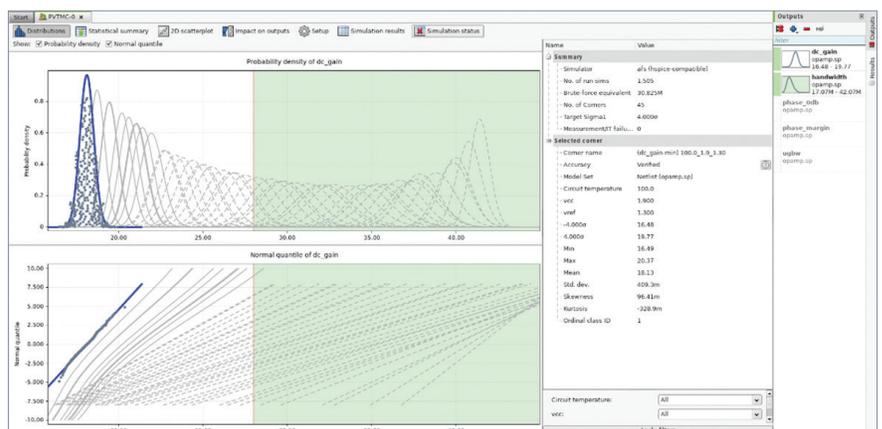
- Intuitive GUI for interactive design and analysis
- GUI or batch mode
- Works with all process technologies
- Integrated with leading design environments
- Supports most commercial and in-house SPICE simulators

Production proven and trusted by top semiconductor companies and foundries

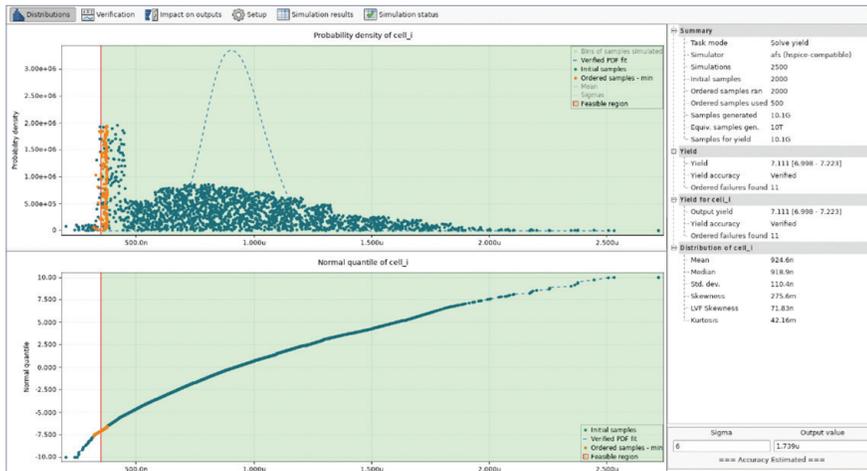
methods, and to assist the user identify optimization paths to improve circuit power, performance, and area. Solido DE can be used throughout the design process from initial device sizing to advanced 6+ sigma variation analysis.

Key technologies in Solido Design Environment include:

- Design Environment:** A comprehensive simulation setup for all the test-benches, including a powerful variable sweep management and a fully configurable corner handling, which allows a seamless transition between nominal and variation while optimizing engineering teams' performance through a streamlined workflow.
- PVTMC Verifier:** Full sign-off level verification coverage across process, voltage, temperature (PVT) and Monte Carlo (MC) variation that is 10-1,000,000x faster than brute force simulation. It identifies the worst-case corner for any target sigma and finds design sensitivities to variation.



FPVTMC Verifier: full coverage of PVT and Monte Carlo at 3-sigma and high-sigma.



High-Sigma Verifier: intelligent, fast, accurate, and verifiable high-sigma results.

- **High-Sigma Verifier:** Quickly verifies any circuit to high-sigma intelligently in a single pass with perfect Monte Carlo and SPICE accuracy. It automatically detects and solves complex binary and multi-modal outputs, and it is fast at any sigma. Its advanced automation makes it easy to deploy to a wide user base in interactive mode, and it is robust for use in large-scale, automated batch flows.
- **Hierarchical Monte Carlo:** Full-chip memory verification. It uses hierarchical, structurally-correct Monte Carlo samples to achieve full-chip simulation accuracy from a simplified memory slice.
- **Fast PVT:** 2-50X faster than brute force simulation across PVT and other operating conditions (such as load, bias and operating mode) with the same accuracy. It identifies design sensitivity to these operating conditions.
- **DesignSense:** Variation-aware sensitivity analysis. It enables rapid and precise variation debugging by sweeping device sizing at worst-case PVT and statistical corners. The tool visualizes trade-offs and opportunities to improve the design.
- **Cell Optimizer:** Automated variation-aware optimization. It efficiently optimizes designs across worst-case PVT and statistical corners, improving yield while delivering the best possible performance, power, and area.

Solido Design Environment specifications

Foundry support

- Supports all leading foundries
- Works with all process technologies

Simulator support

- Supports all commercial and in-house SPICE simulators

Design flow integration

- Integrated with leading design environments
- Standalone command line flow

Cloud readiness

- Cloud-ready and optimized
- Works with major cloud platforms

Grid computing support

- Supports leading computing cluster management platforms

Operating platform support

- Arm
- x86

Operating systems

- Linux®

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Asia-Pacific
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For additional numbers, click [here](#).