



DIGITAL INDUSTRIES SOFTWARE

Transforming analog verification with AI-accelerated circuit simulators for the next era of intelligent design

Executive summary

Semiconductor chip design is undergoing a rapid evolution, driven by the relentless demand for faster, more efficient, and highly integrated electronic systems. However, this progress comes with its own set of challenges, particularly in the realm of simulation and verification. Siemens Digital Industries Software's **Solido™ Simulation Suite** emerges as a cutting-edge solution, offering a unified platform to address the complex needs of analog, mixed-signal, custom-digital and SoC verification in today's semiconductor landscape. This white paper delves into the intricacies of semiconductor design challenges and how Solido Simulation Suite revolutionizes the simulation space with its advanced capabilities.

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The need for faster circuit simulation engines

In the sophisticated field of semiconductor design, the demand for faster SPICE simulation engines has never been more pressing. Modern trends in chip designs, propelled by advancements such as advanced-node adoptions and “More than Moore” designs, have significantly increased design complexity. As analog and custom IC designers strive to meet these demands, they encounter formidable obstacles in the form of slow and lengthy simulations that often fail to adequately cover all aspects of verification.

Increasing post-layout parasitics: Advanced process node adoptions have led to larger designs with escalating post-layout parasitics^{1,2}. This shift necessitates a move from mere schematic simulations to post-layout simulations for accurate verification. Also, larger cross-sections need to be extracted and simulated to validate macro-level functionality. The inclusion of advanced-node transistors introduces numerous parasitic elements, exacerbating simulation complexities. For example, SerDes designs face significant challenges due to the intricate interplay of parasitics in PLL circuits and clock/data recovery circuits, affecting the Bit-Error-Rate (BER).

Transistor model complexity at lower technology nodes: The adoption of complex transistor models at lower technology nodes, such as 3nm and below, has led to slower simulations. Gate-All-Around (GAA) transistor has emerged as the successor to FinFET (figure 1) for significantly scaled process nodes. It provides significant



Figure 1. Evolution of transistor model and complexity (source: Samsung)

capacitive coupling between the gate and the channel. GAA technology is seen as the next evolutionary step to replace FinFET. However, GAA transistors introduce additional complexities due to their unique structure, and although they improve certain parameters, they also bring new challenges related to parasitic capacitances³. Accurate modeling of these capacitances is crucial for analog simulations. Simulations with GAA transistors tend to take longer due to their increased complexity and additional capacitances, prolonging overall runtimes.

Variability: Verifying designs at all corners necessitates thousands of simulations, adding to the simulation burden⁴. Without faster SPICE simulators, meeting tape-out deadlines and time-to-market goals becomes increasingly challenging.

Impact of More than Moore: The emergence of highly integrated designs entails new architectures, such as multi-die systems on chips and 3D IC architectures. These architectures introduce thermal and electromagnetic challenges that require accurate transistor and multi-physics simulations for reliable performance⁵.

Introducing Solido Simulation Suite

Solido Simulation Suite (Solido™ Sim) is the newest addition to Siemens’ intelligent custom IC verification platform (figure 2). It is an integrated suite of AI-accelerated SPICE, fast SPICE and mixed-signal simulators for IC design and verification, empowering IC design teams to meet their demanding analog, RF, mixed-signal, memory, library IP, SoC and 3D IC verification requirements. Built on the foundation of Siemens’ industry-proven, foundry-certified Analog FastSPICE (AFS) platform, Solido Sim incorporates three innovative new simulators: Solido™ SPICE, Solido™ FastSPICE, and Solido™ LibSPICE, and also includes Siemens’ market-proven AFS, Eldo and Symphony solutions. Solido Sim is engineered to help IC design teams meet increasingly stringent specifications, verification coverage metrics and time-to-market requirements. It delivers comprehensive application coverage with best-in-class circuit and SoC verification capabilities. Solido Simulation Suite is integrated natively within Siemens AI-powered Solido Design Environment, offering customers superior performance with optimal accuracy, improved productivity, and

scalability across cloud infrastructure. Further, Solido Simulation Suite works closely with Siemens’ industry leading Calibre® Design solutions IC sign-off flow and Tessent™ Silicon Lifecycle solutions flow as well as Siemens’ Electronic Board System solutions, providing full-flow verification solutions across applications.

The AI advantage

Powering all three of these new solvers is Solido™ Sim AI – the latest version of Siemens’ groundbreaking, AI-accelerated simulation technology. With a legacy tracing back to Solido™ Design Automation, acquired by Siemens in 2017, Solido Sim AI is the newest iteration of the AI technology that Solido Design Automation used to pioneer the design and deployment of AI for EDA purposes 15 years ago. With Solido Sim AI, circuit simulation is advanced to the next level with algorithms that are self-verifying and tuned to SPICE accuracy, providing orders-of-magnitude improved acceleration. All of this is accomplished by using existing foundry-certified device models without alteration.



Figure 2. Siemens’ Solido Intelligent Custom IC Verification Platform.

The new simulators

The three new simulators offer distinguished benefits to IC designers:

Solido SPICE is the next-generation, feature-rich, high-capacity and SPICE-accurate simulation technology, providing 2-30X speedup (Figure 3) for analog, mixed-signal, RF, memory, custom digital, and Library IP applications, with foundry certified accuracy. With newer convergence, cache efficient algorithms and high multi-core scalability, Solido SPICE provides a significant performance boost for large pre- or post-layout designs. RF IC developers can directly benefit from Solido SPICE's new RF verification capabilities, while 2.5D, 3D and memory interface developers can now experience an efficient capability for full channel transceiver verification that includes equalization, drastically reducing interface assumptions and accelerating verification.

Solido FastSPICE is Siemens' cutting-edge fast SPICE simulation technology, providing an order-of-magnitude speedup (Figure 4) for SoC, memory and analog functional verification. It provides a dynamic use model for SPICE-to-fast SPICE scaling, providing a scalable interface to achieve speed goals with predictable accuracy. Solido FastSPICE includes multi-resolution technology for differentiated performance and SPICE-accurate waveforms during critical path analysis for memory and analog characterization.

Solido LibSPICE is Siemens' purpose-built batch solver technology for small designs, providing optimized runtimes (Figure 6) for Library IP applications. Solido LibSPICE is uniquely integrated into Siemens' popular Solido Design Environment and Solido Characterization Suite offerings for performance acceleration, enabling a full-flow solution for seamless and robust verification of standard cells and memory bit-cells.

Solido Simulation Suite benefits

Performance

Solido SPICE is powered by an advanced high-performance solver, bringing significant improvements to circuit simulation. With a strong emphasis on accuracy and efficiency, Solido SPICE enables smooth single-pass simulations for all complex analog designs. Solido SPICE now supports advanced RF envelope analyses and seamless in-die, multi-die and multi-chip interfacing of high-speed link verification including equalization effects.

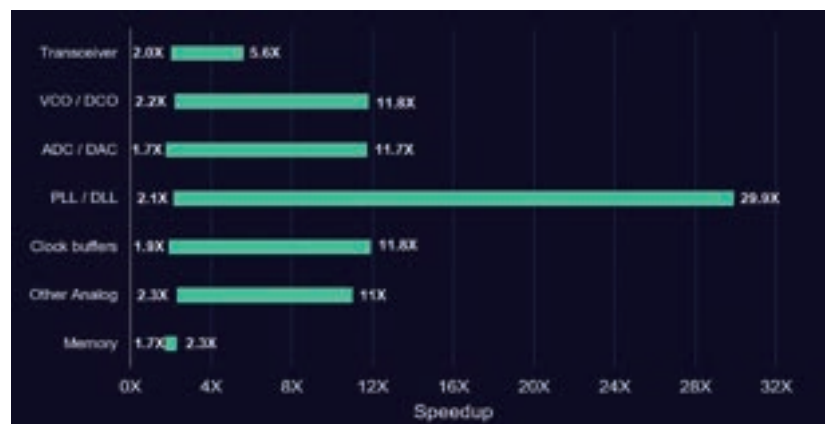


Figure 3. Solido SPICE speedup compared to competition.

- **Strong foundation:** Built on the foundation of industry proven Analog FastSPICE
- **Foundry certified:** Deploys foundry certified models
- **Advanced algorithms:** Utilizes efficient convergence and parasitic reduction algorithms for robust handling of large designs
- **Impressive scalability:** Achieved through cache-efficient memory access and highly parallel scalability on multi-cores

Solido FastSPICE takes the simulation performance to the next level, offering scalable accuracy for both analog and mixed-signal transistor-level functional verification, as well as memory/analog characterization. It incorporates a host of features designed to streamline the simulation speed with minimal accuracy impact.

- **Tunable partitioning:** Offers flexibility in circuit partitioning strategies, enabling efficient simulation of large circuits.
- **Topology/circuit-based detection:** Utilizes advanced detection methods based on circuit topology, enhancing simulation efficiency.
- **Multi-rate simulation:** Multi-rate simulation optimizes efficiency by allowing faster simulation

of components operating at higher speeds, while accurately capturing slower components' behavior, particularly beneficial for mixed-signal, custom analog, or heterogeneous systems.

- **Table-based device modeling:** Facilitates efficient modeling of device characteristics, crucial for fast simulation outcomes without significantly altering accuracy.
- **Advanced parasitic reduction modes:** Implements sophisticated parasitic reduction techniques to minimize computational overhead and maximize performance.

Fast SPICE technology transforms the simulation experience for circuit designers, providing a unified interface that delivers results with remarkable speed and predictable accuracy. Compared to traditional SPICE simulation, Solido FastSPICE offers simulation speeds enhanced by a factor of 10 to 100, without compromising on precision.

Both Solido SPICE and FastSPICE supports industry-standard netlist formats, ensuring compatibility and ease of adoption. Moreover, they seamlessly integrate with Symphony™ mixed-signal simulation platform, empowering comprehensive verification of full-chip and System-on-Chip (SoC) designs.

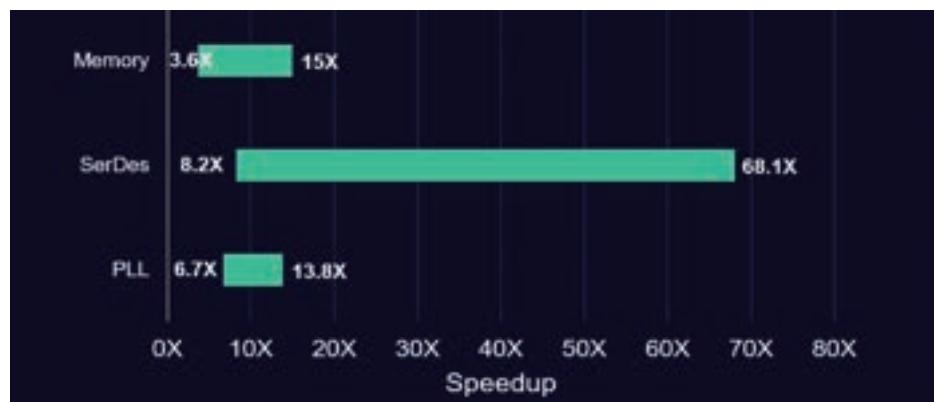


Figure 4. Solido FastSPICE speedup compared to competition.

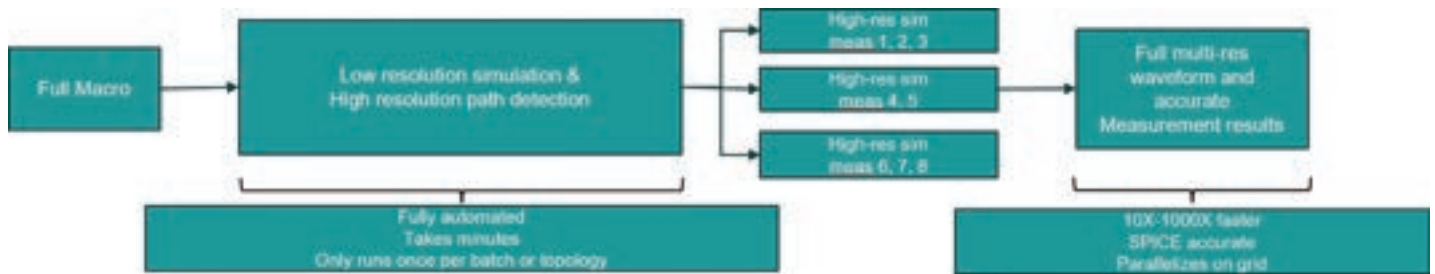


Figure 5. Solido FastSPICE multi-resolution technology.

Multi-resolution technology

Solido FastSPICE offers unique “Multi-resolution” technology that is instrumental for SerDes and SRAM characterization. Multi-resolution technology (figure 5) performs a fast low-resolution measurement-aware simulation, accurately detecting critical high-resolution paths, ensuring thorough circuit analysis and then provides full waveforms for debugging with higher resolution along the critical paths.

- **Speed:** World’s fastest batch fast SPICE simulator
 - >5X speedup for SRAM characterization simulations
 - >2X speedup for SRAM functional verification with 1000s of measures

- **Accuracy:** Within 2%/2ps of Solido™ SPICE
- **Scaling:** Linearly to high CPU counts

Multi-resolution technology combines speed and accuracy, making it an invaluable tool for efficient full macro and large cell characterization, which could otherwise consume days or weeks of simulation time.

Solido LibSPICE is uniquely constructed for handling small designs and is optimized for batch simulation flows including statistical, alters and sweeps. It provides accelerated transient performance for standard cell and memory bit-cell workflows.



Figure 6. Solido LibSPICE speedup compared to competition.

Ease of Use

The Solido Simulation Suite offers streamlined installation, invocation executable, and unified integration with industry simulation environments, reflecting a user-friendly approach that prioritizes simplicity and practicality. The installation process is straightforward and efficient, requiring just one setup to access the entire suite of Solido Simulation products. This eliminates the hassle of multiple installations and ensures a smooth user experience from the outset. The suite seamlessly integrates into

popular simulation environments, enhancing compatibility and ease of use. Its command line interface (CLI) streamlines operations by offering a unified platform for executing various simulation engines, effortlessly toggling between AFS, Solido SPICE, FastSPICE or LibSPICE with straightforward switches. This cohesive framework of switching the simulation engine ensures consistency and ease of use across simulation tasks. Further, with `solidosim -h` command, users now have an easy way to access help on all commands, analyses, options, etc.

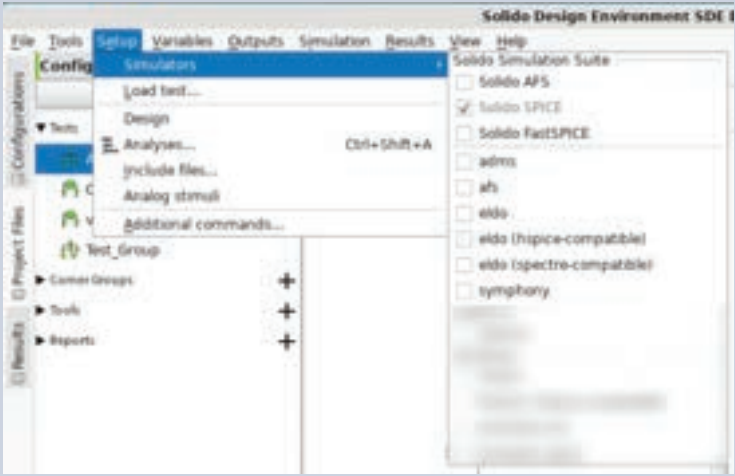
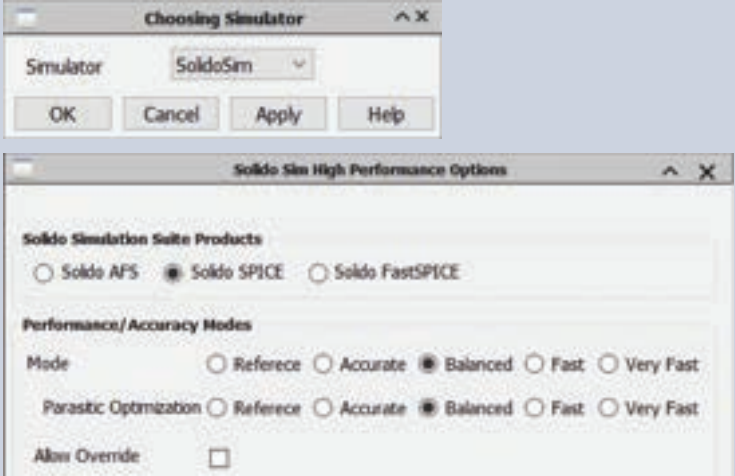
Simulation Environment Invocation	Command line invocation
<p>Solido Design Environment</p> 	<p><code>solidosim -afs</code></p> <p><code>solidosim -spice</code></p> <p><code>solidosim -libspice</code></p> <p><code>solidosim -fastspice</code></p> <p>The current <code>afs</code> executable will exist for backward compatibility.</p>
<p>Other simulation environment</p> 	

Table 1. Solido Simulation Suite Use Model.

Advanced RF analysis capabilities

Solido Sim provides a comprehensive set of RF analyses for pre- and post-layout RFIC design. A crucial capability for verifying advanced digital RF communication systems is RF envelope analysis. Envelope analysis is a technique that efficiently simulates RF circuits operating with complex I/Q limited-bandwidth waveforms, commonly found in digital modulation schemes used in wireless communication systems. Solido Sim offers support for various wireless modulation standards, such as 802.11ax, through “wsource” elements. This enables the simulation of critical measurements like constellation diagrams, error vector magnitude (EVM), and power spectral density (PSD) using accompanying “wprobe” elements. Additionally, users can define their own complex I/Q modulation schemes. These simulation capabilities are crucial for predicting nonlinear distortion effects in circuits like power amplifiers (PAs) used in Wi-Fi applications, which must adhere to stringent specifications for adjacent channel power ratio (ACPR) and EVM. Envelope analysis provides accurate predictions for these metrics based on envelope PSD and constellation results. Furthermore, the inclusion of fast-envelope analysis is particularly beneficial for PA applications. Overall, Solido Sim’s envelope analysis empowers engineers to perform comprehensive design and verification of modern digital RF communication systems.

Advanced high-speed link verification

Verification of high-speed memory and SERDES channels requires combined SPICE-level, S-parameter, and algorithmic IBIS and IBIS-AMI modeling of equalization components to capture chip, package, and board level effects for accurate signal integrity analysis. The IBIS-AMI modeling standard allows silicon IC vendors to share details of their I/O buffer behavior with customers without

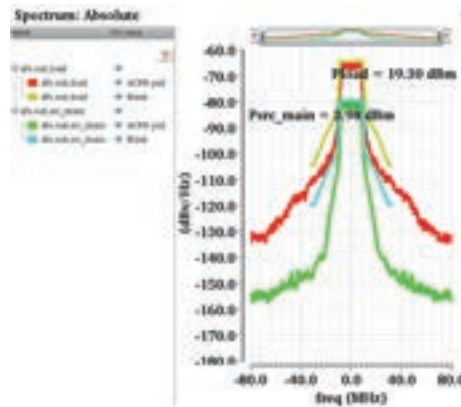


Figure 7(A). Envelope spectrum.

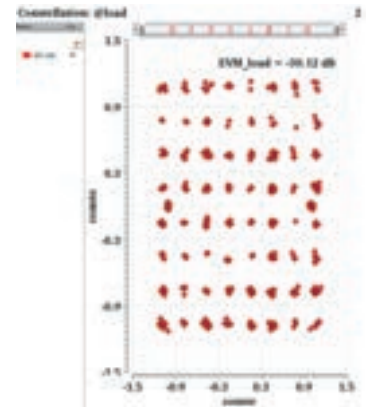


Figure 7(B). Constellation.

disclosing implementation details. These models can capture advanced algorithmic behavior as is needed for channel equalization schemes as well as clock and data recovery approaches. IBIS-AMI is seeing widespread use since its adoption for modeling SERDES interfaces and DDR memory designs. Solido Sim supports the use of IBIS-AMI models in combination with its advanced SPICE verification solution. This makes possible high-accuracy time-domain waveform processing that captures I/O channel losses and circuit nonlinearities, combined with algorithmic modeling that predicts how equalization can mitigate those effects. The result is an ideal combination of speed and accuracy for SERDES and DDR applications.

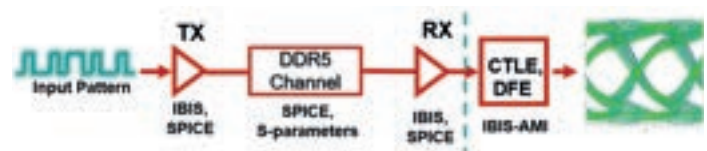


Figure 8(A). Example for DDR interface.



Figure 8(B). Die & Package Cross section.

Integration with other Siemens EDA products

Solido Simulation Suite is tightly integrated with Siemens EDA’s suite of custom IC flows and solutions (figure 9). Within the Design Environment, it interfaces with the AI-powered Solido DE and Tanner schematic and layout capture tool, facilitating streamlined design workflows. Symphony mixed-signal verification is an integral part of Solido Simulation Suite, ensuring comprehensive verification of analog and mixed-signal designs. Additionally, for library characterization, Solido Simulation Suite leverages the powerful Solido characterizer. For EM/IR analysis and Electrical Rule

checks, Solido Simulation Suite collaborates effectively with Calibre technologies mPower and PERC, respectively, ensuring rigorous design rule compliance. Solido SPICE’s engine is integrated with HyperLynx’s engine for IBIS-AMI verification of high-speed links. Lastly, Solido Simulation Suite seamlessly integrates with Tessent’s design-for-test requirements, encompassing analog fault simulation and scan-based test diagnosis, thus providing a comprehensive solution for design verification and testing needs.

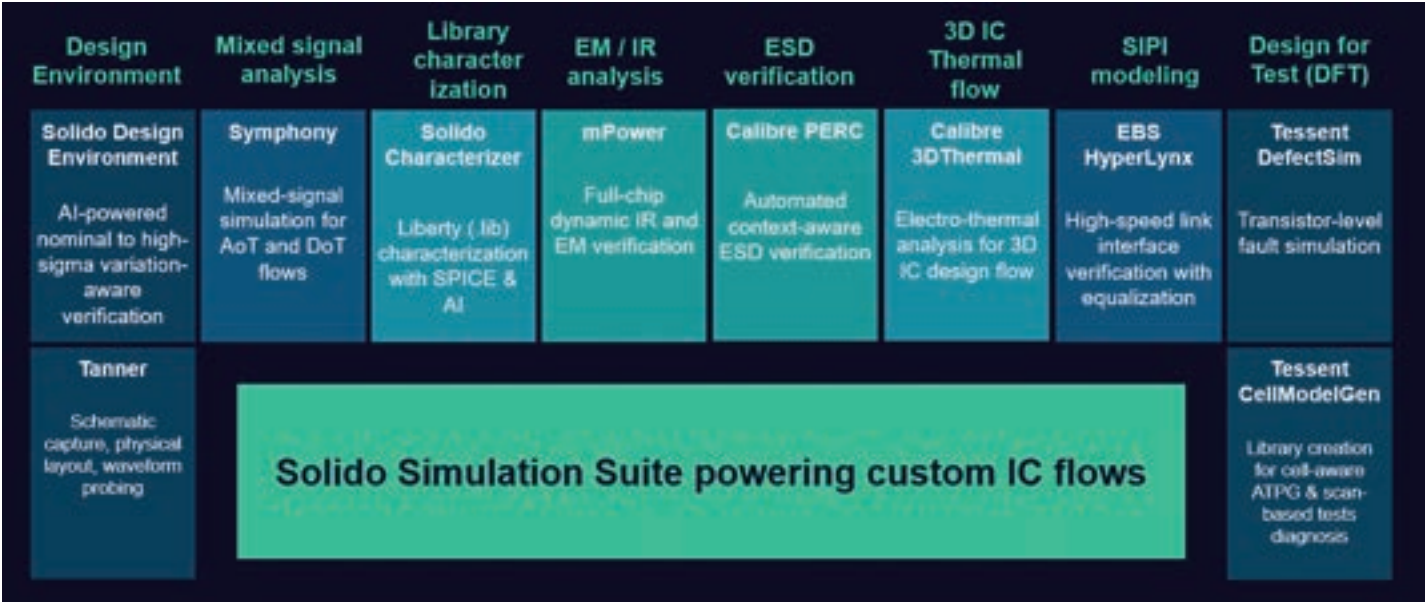


Figure 9. Solido Simulation Suite integration with other Siemens EDA products.

Conclusion

The introduction of Siemens' Solido Simulation Suite marks a significant advancement in semiconductor chip design. This suite offers a one-stop solution to the complex challenges faced by analog, mixed-signal, custom digital and SoC verification engineers in today's semiconductor industry. By employing advanced AI-accelerated simulators, Solido Simulation Suite addresses the pressing need for faster and more accurate analog simulations. It tackles the increasing complexities arising from advanced-node adoptions and multi-die designs,

providing designers with the tools needed to navigate these challenges effectively. With its suite of simulators – Solido SPICE, Solido FastSPICE, and Solido LibSPICE – Siemens enables IC design teams to enhance their productivity and confidence in verifying analog designs. Through integration with Siemens' AI-powered Solido Design Environment, Solido Simulation Suite promises superior performance and scalability, ushering in a new era of intelligent semiconductor chip development.

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