



DIGITAL INDUSTRIES SOFTWARE

# Symphony mixed-signal platform

Industry's fastest and most versatile mixed-signal platform

## Features and benefits

- Fastest accurate mixed-signal simulation
  - Fully leverages AFS advantages
  - Foundry certified nm SPICE accuracy
  - > 5-10x faster than traditional SPICE solvers
  - > 2x faster than parallel SPICE solvers
  - Extremely efficient mixed-signal integration
- Fully configurable architecture
  - Fit-to-Purpose architecture and design-aware technologies
  - Supports industry-leading digital solvers

Today's ICs increasingly rely on complex mixed-signal functionality with stringent performance and low power requirements for applications in segments including IoT, Automotive, Communications, and Industrials. Verification of these complex mixed-signal ICs is challenging due to the need to ensure that they meet demanding specifications with correct connectivity, functionality, and adequate system performance across analog/digital (A/D) interfaces on the chip. To address these challenges verification teams need to run an increasing number of mixed-signal simulations at the top level as well as at the sub-system level. These mixed-signal simulation solutions need to be fast, accurate, easy to use, and seamlessly integrate into existing analog and digital verification flows.

The Symphony™ Mixed-Signal Platform is the industry's fastest and most configurable mixed-signal solution to accurately verify design functionality, connectivity, and performance across A/D interfaces at all levels of the design hierarchy and for all IC applications. Symphony's modular architecture leverages Siemens' Analog FastSPICE™ (AFS) circuit simulator to provide the fastest mixed-signal

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**Features and benefits** *continued*

- Extensible to all Siemens analog solvers
- Provides maximum reuse of verification infrastructure
- Integrated into leading schematic capture flows
- Provides comprehensive language support
- Plug and play setup and use model
  - Support for analog/digital-centric flows
  - Simple & intuitive configuration file format
  - Ability to reuse A/D command line arguments
  - Powerful A/D boundary element support
  - Efficient waveform viewing with Siemens' EZwave viewer
  - Save/Restore capability for enhanced productivity
- Advanced verification and debug
  - Comprehensive visual debug with Visualizer Mixed-Signal (Symphony Pro)
  - Mixed-signal Hi-Z detection
  - Solido Variation Designer integration
  - BE Browser with cross-probing for visual context-based debugging
  - Tcl interactive mode for runtime debugging



simulation performance with nanometer (nm) SPICE accuracy and capacity of 20M SPICE elements. With certified accuracy by the world's leading foundries, AFS delivers 5–10x faster performance than traditional SPICE and > 2x faster performance than parallel SPICE simulators. Symphony has been proven on a wide range of ICs and IC subsystems including ADCs, transceivers, PMICs, multi-GHz PLLs/DLLs, and sensors.

Symphony's unique, fully configurable design-aware technologies and fit-to-purpose architecture provide verification teams the ability to integrate and optimize their mixed-signal flow for any application. Symphony works with all leading digital solvers, including Siemens' Questa®, allowing users to maximize reuse of their existing verification infrastructure, including testbenches, stimuli, scripts, post processing, encrypted IP blocks, and digital/analog netlists. The digital blocks can be described in Verilog, SystemVerilog, VHDL, or encrypted IP and the analog blocks can be described at the transistor level in industry standard SPICE formats or in Verilog-A HDL. Symphony also integrates into the leading schematic capture flows and supports both analog/digital-centric methodologies.

Symphony delivers the industry's most intuitive use model with a simple configuration file format and command structure. The command line structure allows complete reuse of existing digital/analog solver command line arguments. Symphony offers extensive A/D boundary element (BE) support covering all signal types and multiple power domains including those with dynamic supplies. It is integrated with EZwave™ waveform viewer providing a seamless user experience with capabilities such as unified display of A/D waveforms and color coding of waveforms based on design abstraction level.

Symphony's state of the art debugging capabilities improve efficiency of design error tracing across A/D interfaces. It offers a powerful debugging cockpit called the BE Browser to give designers the visual BE context needed to trace back design errors to their sources. Symphony's interactive Tcl mode allows users to interact dynamically with a running simulation to effectively debug their designs. It leverages interoperability of debug features across the schematic capture tool, waveform viewer, and the simulation kernel to provide a seamless user experience. Symphony's Save/Restart functionality increases user productivity for specific applications by avoiding simulation reruns.

Symphony offers a powerful set of features designed to increase the verification scope beyond the pure functional realm into verifying performance aspects of the IC. Symphony's Hi-Z checking capability allows users to detect when a mixed-signal net goes into a 'Z' state enabling the testbench and the digital control logic to respond correctly to the 'Z' state. Symphony is integrated into Solido™ Variation Designer, the world's most advanced variation-aware design solution that enables full design coverage in orders-of magnitude fewer simulations, but with the accuracy of brute force techniques. Symphony Variation Designer is the industry's only variation aware solution that supports mixed-signal capabilities. Symphony supports Analog Access functions to allow testbenches to monitor analog signal behavior deep in the design hierarchy without having to modify the pin interfaces of the intervening modules and preserve the verification intent of the original digital testbench.

Symphony Pro, the advance tier of Symphony, is built on the proven performance of

Symphony and Questa Visualizer™ platform to extend the rapid deployment of industry-standard Universal Verification Methodology (UVM), Real Number Modeling (RNM) and UPF-driven low-power techniques into the mixed signal domain by offering exceptionally fast simulation performance in a unified environment for unprecedented throughput and capacity. Symphony Pro's Visualizer mixed-signal environment offers a seamless debug experience across the entire mixed-signal design hierarchy with comprehensive analysis, automation, and ease-of-use for unmatched productivity.

In summary, Symphony's best-in-class performance, accuracy, and usability enable a broad range of verification checks including:

- Connectivity and functionality checking at the top level across A/D subsystems
- Ensure that higher-order analog behavior does not disrupt system functionality due to A/D feedback
- Characterize analog IP blocks with their digital control included

### **Symphony mixed-signal platform specifications**

- Nanometer SPICE accuracy
  - > 150 dB transient dynamic range
- 1K – 20M element capacity
- Up to 16 cores with multi-threading support
- Transient analysis
- Leading SPICE netlist formats
- Digital HDL support
  - SystemVerilog
  - Verilog
  - VHDL
  - Real number modeling constructs
  - Encrypted digital IP

- Verilog-A and Verilog-AMS HDL support
- Leading digital solver support including Questa
- Design configuration commands
- Sandwich configuration support
- Output formats
  - Analog: wdb, PSF, tr0, nutmeg, FSDB
  - Digital: qdb, FSDB, VCD
- Design flow integration
  - Industry-leading EDA design environment
  - Command line use model
- Built-in A/D Boundary Elements (BE)
  - Bi-directional support
  - Support for logic, electrical & real types
  - Multiple power-supply and supply-sensitive BEs
  - Scoping: net, port, subckt/model, instance
- EZwave Viewer support with unified A/D display
- Advanced features
  - BE Browser
  - Save/Restart
  - Hi-Z checking analysis
  - Analog Access functions for hierarchical references
  - Tcl Interactive Mode
  - Solido Variation Designer integration
  - System-level simulations with MathWorks Simulink
- Hardware requirements
  - Minimum memory recommendation
    - 2 GB of disk space
    - 256 MB of physical memory
    - 512 MB of swap space (virtual memory)
- Operating systems
  - Linux®
  - Redhat®/CentOS 6.5 or higher

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Industries Software  
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Americas  
1 800 498 5351

Europe  
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