

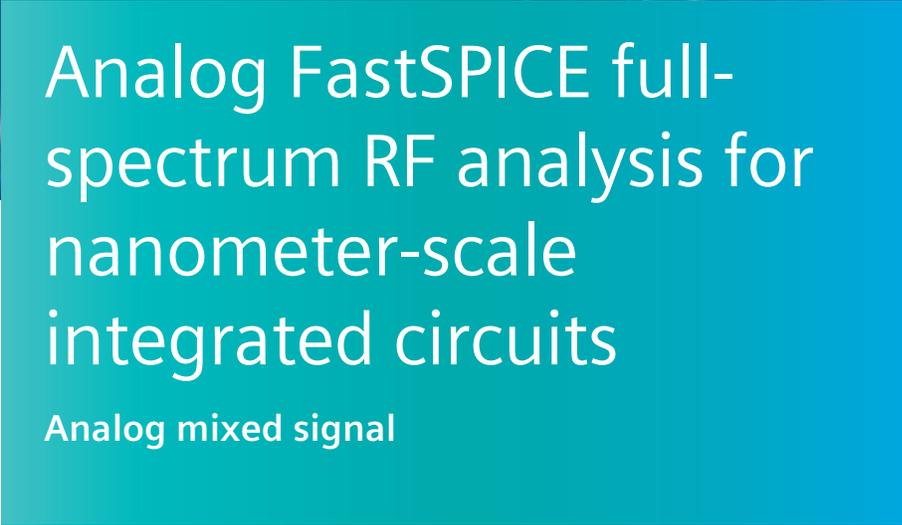


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Analog FastSPICE full-spectrum RF analysis for nanometer-scale integrated circuits

Analog mixed signal

Executive summary

This paper describes Analog FastSPICE RF analyses (AFS RF). AFS RF is a suite of RF analyses within the Analog FastSPICE unified verification platform (AFS Platform) that natively leverages the platform's capabilities.

Introduction

Today's consumer, communication and computer electronic devices have clocks, communication interfaces and high-speed signal-conditioning circuits that operate at radio frequencies (RF). Providing price-competitive products often requires monolithic integration of these circuits in low-power nanometer-scale bulk CMOS silicon. This is a worst-case scenario for RF designers, who must battle a dramatic growth in the number of low-voltage and increasingly nonlinear devices that are subject to nanometer-scale physical effects. There is mounting evidence that these physical effects – most notably device noise, parasitics and crosstalk – fundamentally limit RF circuit performance at 65nm and below.

RF simulation tools have not kept pace with these changing design requirements. Traditional RF simulators have severely limited capacity, have inherently limited accuracy and trade off accuracy for performance. Although these tools are adequate for circuits down to perhaps 0.18 micron or 0.13 micron, they simply cannot provide accurate analysis at the nanometer scale. Lacking dramatically better tool capabilities, designers must rely on approximations that inevitably lead to silicon respins or overdesign (excessive area or power) – both of which are prohibitively expensive.

This paper describes Analog FastSPICE RF analyses (AFS RF). AFS RF is a suite of RF analyses within the Analog FastSPICE unified verification platform (AFS Platform) that natively leverages the platform's capabilities. AFS RF provides the industry's first and only full-spectrum, single-tone RF analyses with true SPICE accuracy and exceptionally fast run times on >100,000-element circuits. Using AFS RF, design teams get silicon-accurate results for highly complex circuits including parasitic and device noise effects.

After a brief overview of nanometer-scale RF circuit design challenges and accuracy requirements, this paper describes how the AFS Platform with AFS RF provides superior "basic" RF circuit verification through transient, harmonic balance and time-based periodic analyses. Next, it describes how the AFS Platform enables RF designers to get true silicon-accurate results by including device noise effects (such as white noise and flicker noise) and parasitic effects for individual blocks as well as complex-blocks (e.g., full PLLs or transmitter transmit/receive paths). Finally, it briefly demonstrates how the AFS Platform enables rapid, rigorous characterization.

Nanometer-scale RF circuit design challenges

Designers of high-performance analog and RF circuits in nanometer-scale CMOS face a number of qualitative and quantitative challenges that did not exist just a few years ago. Driven by requirements for increasing functionality and performance at decreasing cost and power, designers have rapidly moved to highly-integrated, low-voltage, bulk CMOS implementations – an environment that is fundamentally “hostile” to RF circuits. Low voltages mean dramatically less signal headroom and reduced linearity. At the same time, increasing signal bit resolution reduces quantization noise and unmask thermal and flicker device noise effects. Device noise effects are growing significantly as a percentage of overall signal levels and fundamentally limit overall circuit performance at 45nm and below.¹

Designers are fighting signal-to-noise challenges by using more sophisticated circuit architectures, which inevitably increases overall complexity. In the case of mixed-signal interfaces, this includes using circuits such as charge pumps, switched-capacitor filters, phase frequency detectors and dividers that produce sharp signal transitions. Interface blocks operating at multi-gigahertz frequencies are increasingly plagued by parasitics, which often outnumber pre-layout devices by 10x

to 100x at nanometer technologies. Behaving as noise sources and attenuators, these parasitics introduce extremely complex and often unpredictable signal effects that cannot be adequately estimated. Moreover, at these frequencies and signal levels, design teams can no longer rely on simple package models.

In addition to parasitic and package issues, the increasing variability in nanometer-scale processes impacts circuit performance characteristics and must be taken into consideration during block optimization. The increasing variation in circuit performance relative to specified operating ranges and tight implementation constraints (such as device mismatch) requires ever more intensive characterization through extensive corners and Monte Carlo analysis. However, these computationally intensive analyses are often impractical with traditional RF tools.

To illustrate these design challenges, consider a transceiver application. The block diagram in figure 1 shows the verification requirements for a transceiver at the block, complex-block and full-circuit levels. At the block level, the XO and VCO require true SPICE accurate oscillator noise analysis that includes phase noise and amplitude noise contributions. The blocks that are non-linear or have sharp transitions such as the charge pumps,

switched-cap filters and dividers require true SPICE accurate periodic noise analysis. After the block-level analyses are completed, transient noise is required to accurately perform complex-block and full-circuit verification with device noise effects. As is highlighted in gray, all high-frequency blocks should be analyzed with detailed parasitics. The remainder of this paper addresses each of these requirements and analyses.

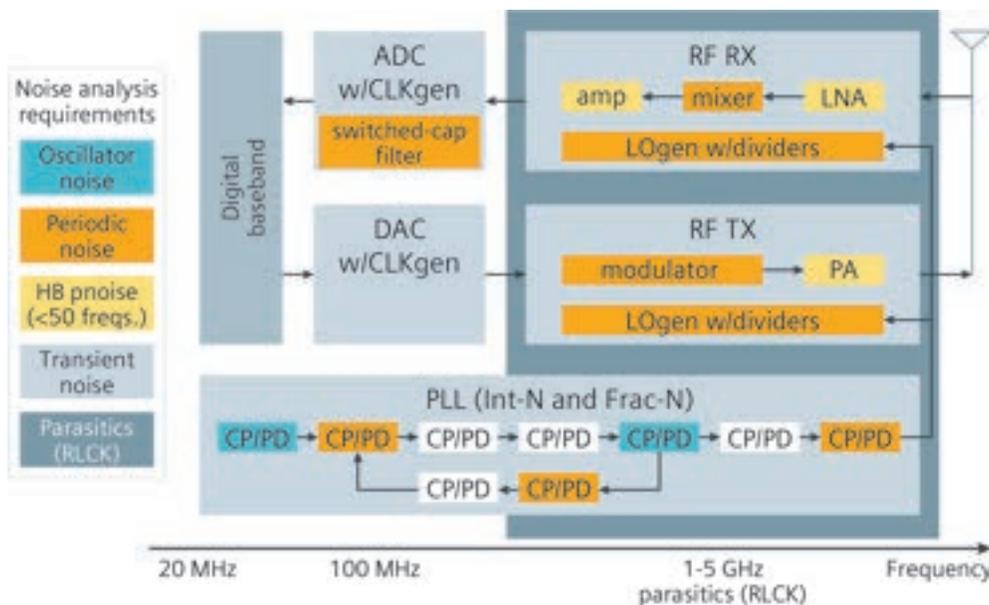


Figure 1: Transceiver noise analysis requirements.

Silicon-accurate analysis

Given the rigorous demands of nanometer-scale GHz CMOS RF circuits, it is imperative that design teams have access to simulation tools that deliver silicon-accurate analysis. Device models are the most obvious accuracy limitation and set the floor for overall analysis accuracy. All tool inaccuracies strictly add to this accuracy floor, thereby directly increasing design margin or the risk of silicon iterations. There are direct and indirect simulator inaccuracies.

Direct simulator inaccuracy includes the simulator noise floor and analysis-specific simplifications. Traditional SPICE transient provides a clear accuracy benchmark for time-domain analyses. Although often overlooked, indirect inaccuracies due to simulator capacity and performance limitations are even more critical. Increasingly designers cannot run sufficient analyses – or perhaps run

a desired analysis at all – without using a divide-and-conquer approach, simplifying their circuit, modeling portions behaviorally, ignoring physical effects, or using a combination of these techniques. The only way to compensate for traditional RF simulator capacity and performance shortcomings is, again, through additional design margin or potential silicon iterations.

The next two sections explain how the AFS Platform with AFS RF addresses issues associated with basic signal analysis, i.e., traditional analysis of pre-layout circuits with manually estimated parasitics, without device noise, without detailed post-layout parasitics, and without process, voltage or temperature (PVT) variations. Subsequent sections progressively add each of these nanometer CMOS silicon realities.

Transient signal analysis

When transient simulation techniques are applied to the analysis of RF circuits, it is usually necessary to transform the simulation results into the frequency domain in order to directly compare them with the circuit specifications. Such transformations can expose minute differences in time-domain waveforms. Thus it is important to ensure any transforms are robust and sufficiently accurate. It is also important to ensure a sufficiently low transient noise floor, because the default SPICE tolerances (~0.1 percent) are often inadequate.

Figure 2 shows the AFS noise floors for different values of reltol based on running a 480 MHz low noise amplifier (LNA) and examining the output spectrum.

The post-processing in the example in figure 2 is such that every other harmonic should ideally be zero at frequencies far away from the signal. The actual

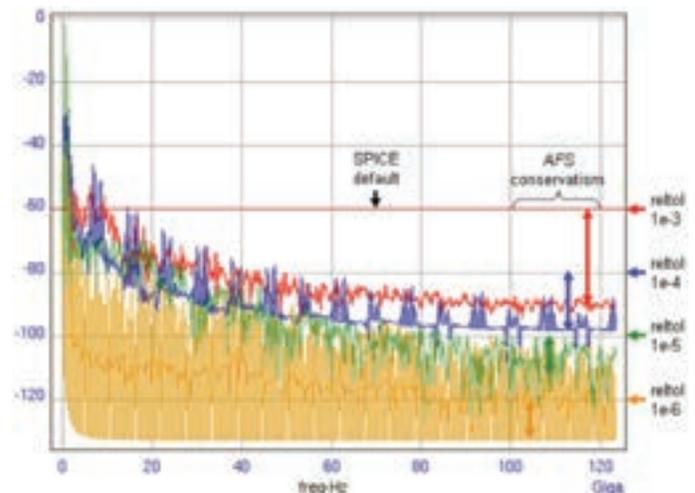


Figure 2: AFS transient noise floor.

simulated values represent the simulator's numerical noise floor. The SPICE default of $1e-3$ implies -60dB noise floor. AFS transient correlates overall accuracy to reltol, conservatively providing more than 20 dB dynamic range per order of magnitude. Reducing reltol by one order of magnitude adds 20dB dynamic range. As the results demonstrate, the AFS noise floor is conservative for each of the reltol settings and reliable to beyond 120dB of dynamic range.

The AFS Platform delivers foundry-certified true SPICE accuracy that is consistently 5x-10x faster than traditional circuit simulation on a single core, and even

faster on multi-core systems. The AFS Platform also provides reliable DC convergence for circuits with >10M elements – 10x to 100x higher than traditional SPICE simulators. AFS reads standard HSPICE® and Spectre® netlists and models as-is, solves the original device equations and solves the complete matrix and device equations at every simulation time step to ensure the highest possible accuracy. As figure 2 demonstrates, AFS transient simulation reliably deliver >120 dB of dynamic range, providing RF designers with world-class accuracy and dramatically higher performance and capacity compared to any other transient simulator.

Periodic signal analysis

For periodic signal analysis, the most appropriate method depends upon circuit non-linearity and behavior. Frequency domain techniques, most notably harmonic balance (HB), provide superior accuracy (dynamic range) and performance for near-linear circuits that do not have sharp transitions. However, nanometer-scale circuits increasingly are moderately to highly nonlinear, exhibit sharp transitions, or both. Analyzing such circuits requires time-domain-based techniques such as Shooting-Newton (SN). The characteristics of nanometer-scale circuits, however, are straining traditional implementations of both approaches, making them increasingly inaccurate or impractical.

Traditional iterative harmonic balance engines that use Krylov-based solvers are excellent for small near-linear RF blocks that require few harmonics. However, periodic steady state (PSS) convergence for these solvers is highly sensitive to circuit complexity, nonlinearities and the number of harmonics. When traditional HB tools cannot reliably converge, designers must analyze smaller blocks, simplify the circuit, or reduce the number of harmonics. All of these approaches sacrifice accuracy. Marginal convergence at this stage simply delays the problem to later in the design cycle when it is desirable to include parasitics, device noise effects, or characterize the circuit across corners or process variations. In addition to a traditional Krylov-based solver, Analog FastSPICE RF includes the industry's first HB

direct solver. The HB direct solver provides significantly more robust convergence and 2x to 10x higher performance on moderately nonlinear circuits.²

Traditional RF simulation tools rely on limited-spectrum approaches that only consider a specified number of harmonics or sidebands around the circuit frequency for the noise computations. In contrast, AFS provides the industry's only full-spectrum periodic noise analysis (pnoise). It is named full-spectrum because it includes device noise effects from all sidebands or harmonics. Figure 3 demonstrates the impact of limited-spectrum

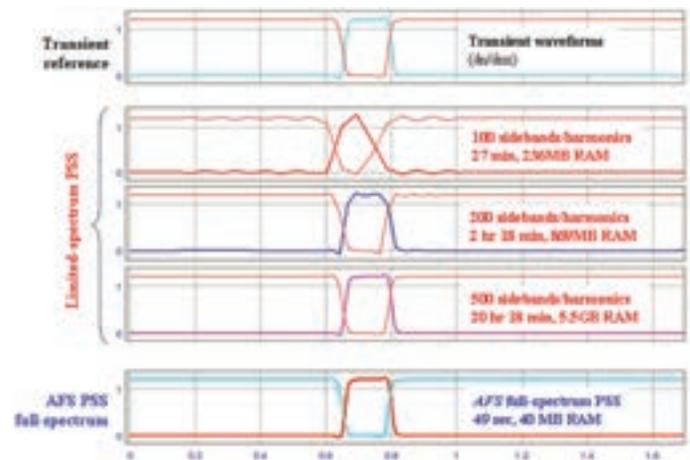


Figure 3: Phase frequency detector PSS results.

techniques in PSS accuracy – and by implication, on noise accuracy. These results apply to HB and limited spectrum noise.

The top plot in figure 3 shows the transient waveforms for a single period of a phase frequency detector. This circuit demonstrates the challenges associated with analyzing circuits with sharp transitions. The middle three plots show results for limited-spectrum runs with an increasing number of harmonics or sidebands. Note the increase in runtime and memory as the PSS results start to approach the transient waveforms. At the 500-sideband level, limited-spectrum PSS took 20hrs and the results approximate transient but still do not match within even default SPICE tolerances. As the bottom plot demonstrates, AFS full-spectrum noise delivers results that are identical to transient in a single 49 second run with very low memory requirements.

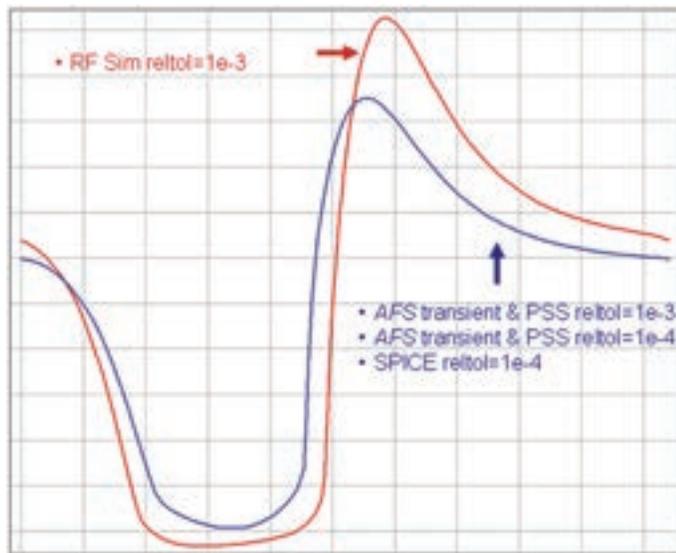


Figure 4: AFS PSS accuracy example.

Traditional RF simulators have also run into severe limitations in PSS convergence. With a practical limit of a few thousand elements, these simulators increasingly cannot handle today's pre-layout RF blocks. To make matters worse, traditional RF simulators often produce incorrect PSS results. PSS should yield a result that is within the SPICE tolerance of a SPICE transient simulation that has run long enough to reach the circuit's periodic steady state. Unfortunately this is not always the case in traditional RF simulators. Figure 4 demonstrates such a case in which the RF simulator reported a PSS that was markedly different from a traditional SPICE simulator, AFS transient and AFS RF PSS – all of which agreed to within the SPICE tolerances. The result was that the traditional RF simulator reported grossly inaccurate noise results.

In addition to PSS accuracy issues, traditional RF simulators have severe PSS convergence capacity limitations. With a practical limit of a few thousand elements, these simulators increasingly cannot handle today's pre-layout RF blocks. Designers often conclude that traditional RF simulators are essentially unusable for post-layout PSS analysis of all but the simplest blocks.

AFS RF uses the AFS transient engine to deliver PSS results with true SPICE accuracy. Coupled with next-generation PSS algorithms, the result is robust, accurate convergence on circuits with >100K elements – typically 10x to 20x larger than traditional RF simulators. In fact, AFS RF has successfully converged on post-layout RF circuits with 400K elements. This capacity lets designers run pre-layout and post-layout analyses on complex RF blocks without making any simplifications that reduce accuracy.

Periodic device noise analysis

Device noise has become a first-order physical effect for nanometer-scale CMOS circuits, and is the primary performance limiter for many high-performance analog and RF circuits at 45nm and below. Traditional RF simulation tools employ limited-spectrum approaches to estimate device noise impact based on computing each device's noise contribution from a specified number of harmonics or sidebands around the circuit frequency. This approach is sufficient for circuits in 0.18 micron or larger technologies, and for circuits without sharp transitions. However, it is increasingly inadequate at decreasing process nodes and for circuits with sharp transitions such as charge pumps, switch capacitor filters, phase frequency detectors and dividers. Such cases numerically require many hundreds or thousands of harmonics or sidebands that leads to convergence problems and extremely long runtimes.

AFS RF provides traditional harmonics-based device noise computation for circuits that require only a few sidebands. However, for circuits with sharp transitions, AFS RF provides full-spectrum periodic analysis (AFS RF pnoise) that performs device noise computations directly in the time domain and then translates the results to the frequency domain. Using a unique computational approach, AFS RF provides the equivalent of an infinite number of harmonics or sidebands on every run. The result is true SPICE accuracy in device noise analysis regardless of the circuit type. For circuits with sharp transitions, AFS RF pnoise produces silicon-accurate results in a single run, often over 10x faster than the best approximations from traditional RF tools. By combining the superior PSS convergence and pnoise performance of AFS RF, designers can easily analyze circuits that are >10x more complex than is otherwise possible at this level of accuracy.

Figure 5 illustrates the requirement for full-spectrum pnoise for circuits with sharp transitions using a switched-cap filter example. As is shown, increasing the number of sidebands in the traditional RF simulator ("RF Sim") dramatically changes the results which monotonically approach those of the AFS full-spectrum pnoise analysis. Moreover the runtime differences between the two approaches were dramatic. The most accurate run that actually converged in the traditional RF simulator took

over 2 days. By contrast, the first and only AFS RF run delivered true SPICE accurate results in just 1.5 minutes.

AFS RF also provides the industry's only full-spectrum oscillator device noise analysis (oscnoise). Oscillators are unique in that they effectively have two noise effect regions: phase noise dominates for low- to mid-offset frequencies, and amplitude noise dominates at high-offset frequencies. Phase noise is a large-signal effect, while amplitude noise is a small-signal effect. Traditional RF simulators use modified forms of limited-spectrum periodic noise analysis to approximate oscillator device noise effects in both regions. This approach often yields particularly poor estimates at low- and high-offset frequencies.

AFS RF uses a proprietary non-approximate stochastic nonlinear engine for transistor-level phase noise analysis and full-spectrum pnoise analysis for amplitude analysis.³ Numerous design teams have independently proven that the results are silicon accurate across the full frequency spectrum. As a by-product of this unique computational approach, for every noise source AFS RF oscnoise analysis provides profiles of the noise intensity, oscillator output phase noise sensitivity to the noise intensity (the impulse sensitivity function – ISF) and the product of these two profiles mapped across a period.^{4,5} This information lets oscillator designers rapidly pinpoint issues and opportunities for oscillator noise optimization, both in circuit topology and device design.

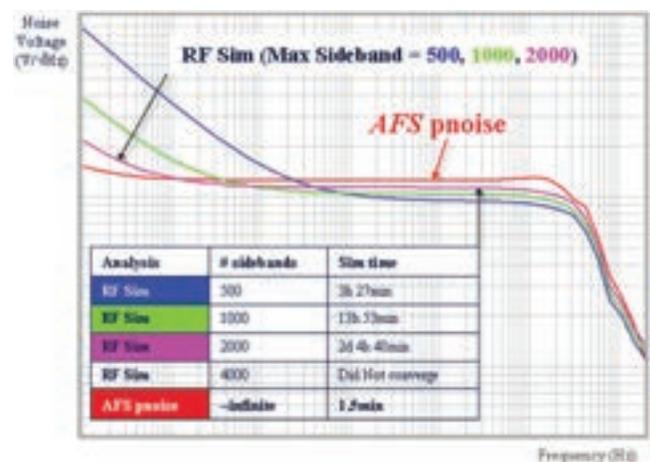


Figure 5: AFS pnoise accuracy example.

Transient device noise analysis

Virtually all periodic blocks are integrated into higher-level complex-blocks such as PLLs, receive chains, transmit chains, I/O channels and frequency synthesizers. Such blocks exhibit complex nonlinear behavior relative to their sub-blocks. Without a tool that can run transistor-level device noise analysis at the complex-block level, design teams must create behavioral models that translate the sub-block effects to the complex-block specification level, e.g., PLL jitter or phase noise metrics.

The AFS Platform includes transient noise analysis (AFS TN) that provides proven true SPICE accuracy for any type of circuit: non-periodic, periodic driven and periodic autonomous circuits (oscillators). Transient noise analysis injects representative white and flicker noise samples for every noise source at every time step, based on the instantaneous device bias condition and the device noise information in the model files. AFS TN is built on the AFS transient engine with its true SPICE accuracy, 5x-10x performance over traditional SPICE, and >10M-element capacity. The AFS TN implementation is very efficient, with runtimes that are within 2x of an AFS transient-only simulation. AFS TN is proven to consistently produce results that are within 1dB to 2dB of measured silicon for integer-N PLLs, fractional-N PLLs, DACs and ADCs.

Figure 6 shows the AFS transient noise analysis results and silicon measurements for an integer-N PLL operating at 800 MHz. As highlighted in the phase noise plot, the AFS TN results and measurements agree within 0.5 dB at the specified offset frequencies.

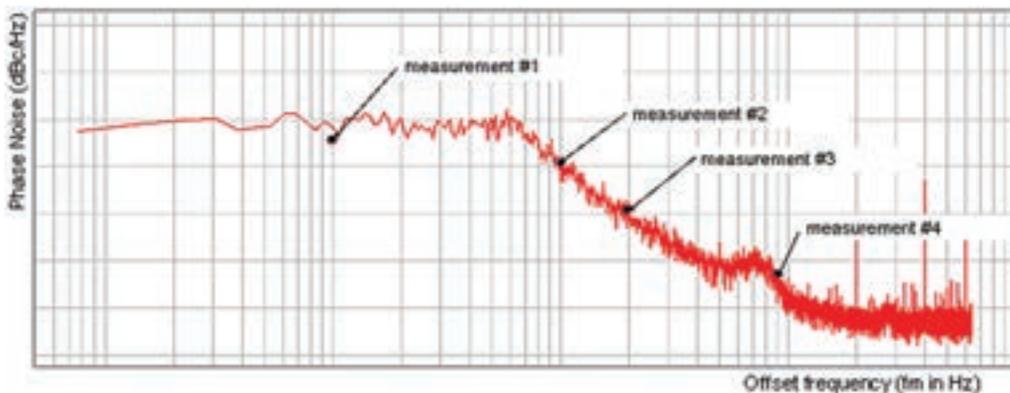


Figure 6: Integer-N PLL -AFS transient noise vs. silicon measurement.

Similarly, figure 7 demonstrates the accuracy of AFS TN on a sigma-delta ADC. As is shown, the transient noise analysis results are in excellent agreement with silicon, both of which dramatically differ from transient only simulation. This example illustrates the need to include device noise effects early in the design cycle, and thereafter.⁶

AFS TN also serves as a golden reference for device noise analysis. It is straightforward to directly compare the results of AFS TN to AFS RF pnoise and AFS RF oscnoise, for example, which enables designers to validate analyses with independent techniques. This triangulation is an effective way to resolve any discrepancies with traditional RF simulator results and gain better insight into device noise sources and their effects.

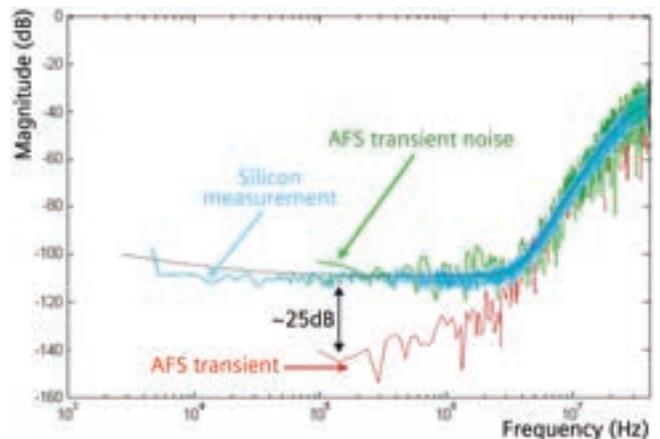


Figure 7: Sigma-delta ADC - AFS transient noise vs. silicon measurement.

Parasitics

Designers know that parasitics can profoundly affect circuit performance, especially at high frequencies. Unfortunately, traditional RF simulators do not have the capacity or performance to include detailed parasitics unless the block size is very small. Assuming a 10x to 100x increase in total element count and a practical capacity limit of a few thousand elements for traditional RF simulators, designers are limited to blocks that are at most a few hundred elements for reliable RF analysis. Instead designers manually estimate and include elements for what believe will be the most important parasitics. For larger blocks, designers often estimate or

model how various blocks will interact, or build in enough design margin to compensate for the parasitics that they cannot actually simulate.

AFS RF provides >100K-element capacity and superior performance, so it can directly run RF analyses and include detailed parasitics without estimations, models, or over-engineering. This holds true in harmonic balance and time-based analyses, including PSS and noise. Moreover, AFS TN lets designers simulate circuits of almost any size with true SPICE accuracy.

Characterization

Due to the narrow operating range and increasing process variability in nanometer-scale CMOS, thorough characterization of RF circuits has never been more important. This is especially true when the RF circuitry is integrated on a complex mixed-signal IC, where the direct and opportunity costs of silicon iterations to meet specifications or improve yield can be extremely high.

Characterization enables design teams understand the silicon performance implications of operating under temperature, voltage and process variations. A corners-based methodology considers specific extreme conditions, whereas a Monte Carlo-based approach stochastically models realistic process distributions. Variants of each approach, such as intelligent corner selection and Monte Carlo Latin Hypercube Sampling, may produce higher quality results with fewer iterations. However, the number of necessary iterations remains large, and is increasing, even when designers use the most efficient methodologies. RF designers know that they should do considerably more characterization, and would like to

do so, but they face practical limitations: correlation of results to silicon, simulation time and simulator license and hardware limitations.

Silicon correlation in particular is a fundamental limitation, without which the other limitations are much less relevant. As described above, device noise and parasitics are first-order physical effects in nanometer-scale circuits. Due to the limitations of traditional RF simulators, it has been impractical to get true SPICE accurate results while including these effects. Unfortunately, characterization that fails to include these effects provides limited benefits (i.e. basic performance sensitivity analysis), because the results will not correlate with silicon.

AFS RF elegantly and practically addresses all of today's RF characterization limitations. Its true SPICE accuracy, which incorporates device noise and parasitic effects, ensures results that correlate very well with measured silicon. The superior performance and convergence of AFS RF enables the fastest and most robust analysis across a wide range of variations. AFS RF can also utilize the AFS Platform

multi-core parallel (MCP) operating mode to run characterization iterations for sweeps or Monte Carlo on different cores of a shared-memory system.

The AFS Platform MCP automatically handles assigning the runs and aggregating the results. The speedup is typically 2.5x-4x for four cores and 4x-6x on eight cores, with no change in the use model or the accuracy of the results. Combining the effects of a 5x-10x faster single iteration runtime with MCP, designers can realize >25x overall faster turnaround; hence a 24-hour characterization job is done in less than one hour on a single machine. Moreover, the AFS Platform MCP capability is very license-efficient, yielding a ~33 percent cost/run savings on four-core runs and a ~50 percent cost/run savings on eight-core runs.

Table 1 shows AFS Platform MCP benchmark results for several RF circuits and demonstrates the speedup of the AFS MCP versus single-core AFS.

TABLE 1. MCP benchmarks

AFS Multi-Core Parallel			Speedup vs. 1-Core AFS		
Circuit	Analysis	Elements	MOS	4-Core AFS	8-Core AFS
Ring VCO	RF	101	80	3.8x	5.2x
DSM IP3	RF	1.4K	135	3.5x	4.5x
ADC	transient	17K	15.4K	3.6x	5.7x
VCO	transient	1.5K	1.2K	3.3x	5.0x
DLL	transient	127K	4.3K	4.0x	7.8x

Conclusion

In the past decade, RF designers have moved from designing dedicated analog or RF circuits in specialized silicon to designing 10x more complex, 10x higher frequency mixed-signal circuits in nanometer-scale CMOS – circuitry which is often monolithically integrated with a massive amount of digital logic. Traditional RF simulation tools have simply not kept pace. The AFS Platform with AFS RF provides silicon-proven accuracy in the face of nanometer-scale physical effects – and does so with 5x-10x higher performance and >10x higher capacity than traditional RF tools. The AFS Platform greatly improves the productivity of RF design teams, letting them quickly deliver lower-cost, lower-power silicon that consistently meets the most challenging IC specifications.

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