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Advancing silicon photonics physical verification through innovation

Executive summary

The growing market for silicon photonic integrated circuits has led to the need for reliable, automated physical and manufacturing verification process flows that address the unique physical characteristics of silicon photonics designs. By expanding and adapting the use of established physical verification and optimization functionality, EDA companies have enabled their tools to accommodate the new components and design concepts of silicon photonics designs, and provided photonics designers with an automated and standardized path to tapeout.

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Introduction

Historically, integrated circuit (IC) design processes, particularly at older nodes, assume that what is drawn is what will be delivered (design to mask to silicon). And, historically, foundries have been able to deliver on that assumption, with a little help from the electronic design automation (EDA) industry. Design houses use design rule checking (DRC) and layout vs. schematic (LVS) verification to ensure a physical layout correctly implements the intended circuitry, and complies with the foundry's physical manufacturing requirements for the process node. However, even when layouts comply with all design rules, performance and yield issues can arise during manufacturing, due primarily to slight and unavoidable variations that occur during the various processes. To mitigate the effects of these manufacturing processes on the final silicon, most design houses apply an additional set of design for manufacturing (DFM) checks that help predict how a given design will react to a manufacturing process. For instance, engineers use lithography-friendly design (LFD) simulation to discover any areas in the layout that may cause resolution issues during the lithography process. They can then employ techniques such as optical proximity correction (OPC) to modify the layout before manufacturing to ensure the printed IC will accurately represent the intended layout.

Of course, trying to perform all this verification manually would be impossible. One of the primary developments that ensured the success of the electronic IC (EIC) market was the origination of a solid and stable automated verification platform. Verification strategies implemented in EDA tools help guarantee the manufacturability of ICs, as well as standardizing and optimizing IC design across the industry, making it the booming market it is today. EDA tools and technology, combined with the foundry process design kit (PDK), which is the embodiment of the rules and requirements for manufacturing at a given process node, were core components in the origin of the "fabless" design house. The emergence of independent foundries was the underlying factor that enabled the EDA industry to rise to prominence; in turn, EDA allowed the rapid development of the CMOS market and was a key contributor to its success. Along the way, design tools also evolved, speeding the process through different levels of abstraction while helping to ensure correct design and layout implementation. Design tools and methodologies such as place and route (P&R), as well as design components (like pcells for custom designs) are now used to move design flows towards efficient and successful implementation.

Silicon photonics is an emerging technology that shows great promise in overcoming some of the limitations that currently exist in the communication and data transfer domain in terms of speed, power, and accuracy. To deliver on that promise, and make photonics ICs (PICs) a worthy competitor to existing EIC technologies, it only makes sense to try to duplicate the same success of the EIC world by reusing the CMOS platform, particularly the verification EDA toolset. However, the nature of photonic devices creates limitations that prevent the direct use of the same EDA toolset used for EICs. These limitations are driving the development of innovative workarounds by EDA companies to enable design companies to use their existing tools' functionalities in a new way to successfully verify PICs, rather than spending that time, effort, and money to create an entirely new and separate toolset.

While PDKs and the automated design and verification flows that use them have been perfected for the EIC industry, they are still in the development phase for the PICs industry. Foundries, EDA providers, and design houses are all working in conjunction to create a successful automated design and verification environment for silicon photonics designs

Photonics verification challenges

The main blocks of the EIC verification platform are the DRC and LVS processes. DRC ensures the manufacturing feasibility of an EIC layout (physical design implementation) by validating its geometrical integrity and compliance with the foundry's physical requirements, while LVS is responsible for ensuring correct circuit functionality by ensuring the layout matches and correctly implements the design intent, as provided in the schematic. LVS verification includes checking the type and count of devices, comparing their geometrical parameters to the source, and checking the connectivity between devices.

The secondary (but no less important) function of EDA tools is design optimization. Design for manufacturing (DFM) analysis enables design teams to adjust their DRC- and LVS-clean designs to further improve their manufacturability. One DFM technique is the insertion of fill—metal shapes or devices that serve no electrical purpose, and are not typically connected to any power source. During manufacturing, after a layer is created, that layer is polished using chemical-mechanical

polishing (CMP) to remove excess materials and ensure a flat, uniform surface. If, for example, there are large open areas next to densely-populated areas of metal, CMP can create peaks and valleys. Fill is added to these open areas in the layout to provide a more uniform distribution of metal across the layout, which in turn provides a more consistent response to the CMP process. Designers use CMP simulation in conjunction with automated fill functionality to determine optimum fill insertion.

The goals of DRC, LVS, and DFM remain the same for PICs as they are for EICs. However, the reuse of the EIC verification platform is not a simple or straightforward process, owing to the disparities between EICs and PICs. EDA companies must find ways to adapt their tools to account for the differences between PICs and EICs, while still ensuring fast, accurate verification of PIC designs.

Another relevant factor is that the design to silicon process for PICs is also still quite embryonic . PICs were initially designed using in-house scripting technologies. Designers determined the required optical behavior, converted these requirements to desired curvatures, connected the necessary components, then converted this design to a tapeout database format such as GDSII or OASIS. Not only is this approach time-consuming and extremely risky, due to the ever-present possibility of human error in scripting or calculations, but it also poses significant challenges when trying to fix any manufacturing-related errors found in a generated layout.e. While moving from a scripted approach to an automated flow more analogous to a custom EIC flow can help increase the scaling limits of PIC design, and provide more flexibility to implement manual changes, PIC design still requires a significant amount of manual effort.

Photonics DRC

The geometrical integrity of an EIC design is measured by DRC, which determines if the design's physical layout complies with the manufacturing requirements (design rules) set by the foundry. Because traditional EIC designs consist of Manhattan shapes placed on a rectangular grid, the measurement of various geometrical parameters is straightforward, and accuracy can be quite precise.

However, in PICs, devices are characterized by their curvilinear features. Placing curvilinear structures on a rectangular grid presents a challenge for EIC verification tools and processes. Precise measurement is problematic due to edge and vertex snapping, which can occur when the vertices of the curved shapes must adapt to the limited precision of piecewise linear approximation (figure 1). This effect must be compensated for during the geometrical parameter measurements.

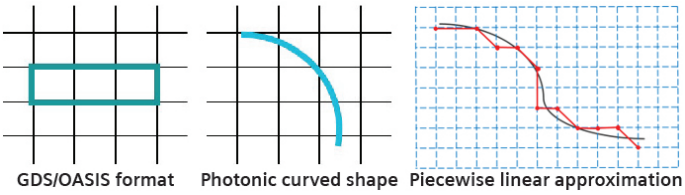

Figure 1. Electronic IC layout vs. photonics IC layout verification.

Different PIC verification techniques can achieve the required degree of accuracy with modest modifications to existing EIC toolsets. In the Calibre nmPlatform, equation-based DRC can be used to apply complex conditional DRC with the necessary tolerance to eliminate the false errors in the curved segments. This use of the Calibre eqDRC tool does requires modification of the foundry rule deck to add the eqDRC operations for each PIC spacing check that detects curved edges, and the required tolerance to be used when measuring spacing between these edges (Figure 2).

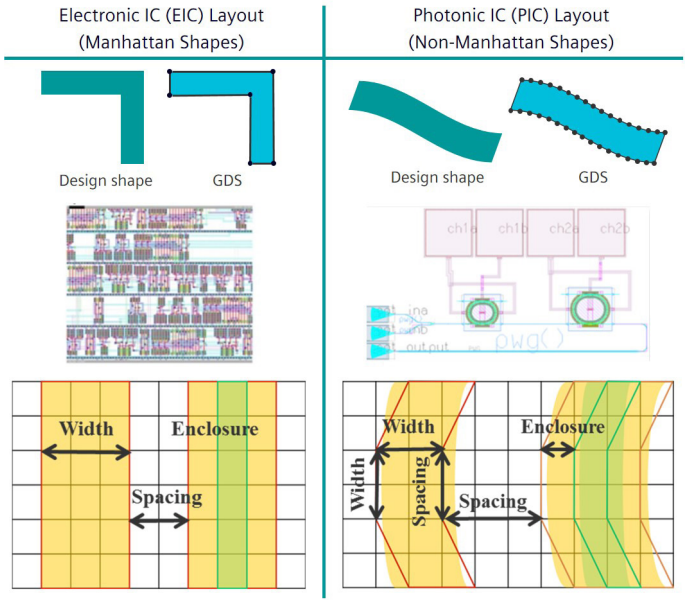

Figure 2. Physical verification challenges of curvilinear structures can be addressed with equation-based DRC.

However, because design houses generally prefer to avoid any modification of a foundry rule deck, Siemens introduced an alternative approach that leverages the Calibre Auto-Waivers infrastructure as a post-processing step to automatically filter out these spacing check false violations, so that only real violations are reported in the DRC results database file. This approach differs from the traditional EIC Calibre Auto-Waivers functionality, in which designers first run Calibre nmDRC, analyze the violations, identify the false results, and generate waivers for them. These waivers are then used to waive any false violations in future DRC runs. In the post-processing flow for silicon photonics, designers just need to perform one Calibre nmDRC run.

Invoking this option simply requires engineers to run the Calibre nmDRC tool in waiver mode (figure 3). The Calibre Auto-Waivers technology automatically identifies the original PIC curved layer. Any violations reported over its skew edges have an extra calculated tolerance added to the measured spacing value to compensate for the skew edge grid-snapping before the actual spacing is compared to the original spacing constraint specified in the rule deck. Spacings that still violate the constraint are reported as real violations, while the others are filtered out as "false" violations, to be stored and reported in a separate results database file for review, if needed. This flow runs seamlessly, so engineers do not need to be aware of the underlying details when invoking waiver mode.

The main advantage of this technique is that it is fully automated—it saves the foundries from the time and effort of implementing and supporting special DRC code for silicon photonics verification. Such implementations are usually quite time-consuming, as the special Calibre eqDRC operations must be added for each check in every DRC deck. The proposed flow enables foundries to use their existing DRC decks for spacing checks in silicon photonics layouts. Accountability is maintained because all filtered-out false violations are saved in a separate results database file.

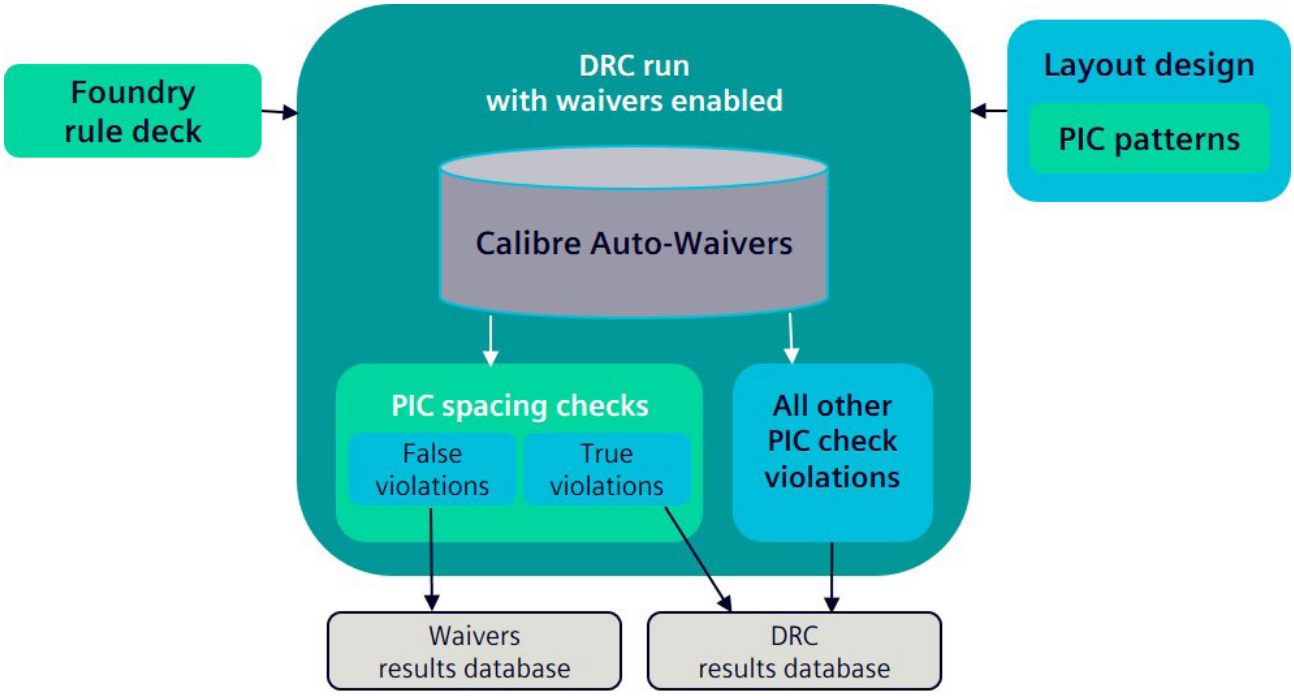

Figure 3. The Calibre Auto-Waivers tool automatically filters out PIC false violations during post-processing.

Photonics circuit verification

The challenge for circuit verification of silicon photonics designs is that silicon photonics design is still very immature compared to the EIC world. This immaturity makes the basic phases of traditional LVS, such as extracting devices from the layout, characterizing these devices with their most distinguishing geometrical parameters, and comparing them with the devices in the source schematic, much harder to perform. The primary difficulty is that unlike an EIC, where its basic components are treated as built-in devices by the existing EDA tools, PIC components are not yet natively supported as built-in devices. Consequently, photonic devices must be treated as custom devices, and new techniques must be adopted to extract them from the layout. The other difficulty is that most of today's photonic designs are layout-centric, meaning there is no schematic against which the layout can be compared. These differences make circuit verification of PICs a much harder task.

When verifying connectivity in an EIC, interconnects are treated as ideal wires, with no dimensions or parameters to be extracted and validated. Simply ensuring there are no unintended shorts or opens and that all devices are properly connected to one another is sufficient to verify correct connectivity and behavior. However, in a PIC, this approach is inadequate to ensure proper optical connectivity and behavior. For example, waveguides may seem to be analogous to wires, but they must be treated as devices, not interconnect, because their geometrical parameters affect the propagation of light, which has a significant impact on determining proper circuit operation (figure 4).

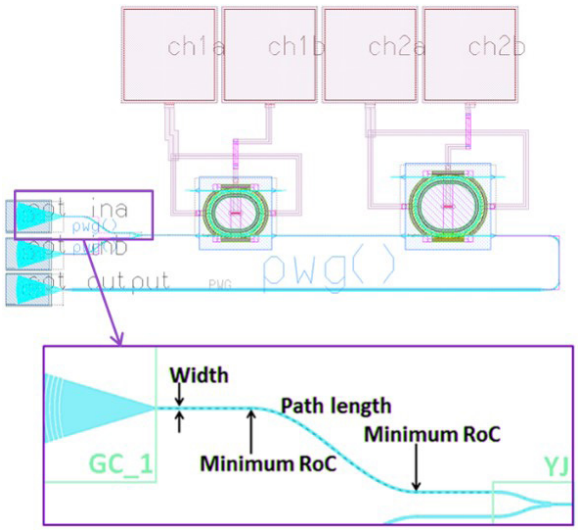

Figure 4. Waveguides parameter extraction.

Another key difference between a photonic and an electronic circuit is the definition of shorts and opens. Unlike wires in an EIC that cannot cross, it is not unusual for two waveguides to overlap in a PIC to create a crossing. These overlapping devices become a four-port network, without resulting in a short. Likewise, a terminator device does not constitute an open in a photonics circuit; it simply prevents the light from progressing forward.

Another important aspect to consider is the correct validation of the behavior of each device in a PIC design. In EIC LVS, validation calculates certain parameters for each device and compares those parameters to the source. These parameters are measured based on Manhattan-like geometries, like transistor length. In a PIC layout, where the devices are curvilinear, traditional LVS tools struggle to extract such parameters and validate correct device functionality, keeping in mind that any deviations from the intended shapes means the photonic circuit won't behave as expected or designed.

Considering all these points, the first step is to recognize and define the components required for PIC validation that are missing from the traditional LVS flow. There have been multiple attempts to develop a complete generic solution to the photonic LVS problem. Some solutions depend on ignoring the cell contents completely by performing a simple device black box-style LVS verification to ensure no shorts or opens exist in the generated layout, that is, using a correct-by-construction technique to verify the connectivity. This approach is limited in that it does not fully ensure proper matching between source and layout devices. Other solutions use a methodology that relies on substantial coding efforts to create a process that extracts the photonic devices, measures their parameters, and compares them to the source, all while overcoming the snapping issues. These solutions are certainly more accurate, but they require significant time and resources to create and maintain the code, as well as potentially requiring a large number of iterations to achieve a final deck that returns correct LVS results with no false violations. A hybrid approach that uses labels or markers can reduce the coding effort needed for the extraction of devices and their parameters, as well as maintain circuit integrity by not ignoring the cell content altogether, but it is time-consuming and subject to human error, and still returns an incomplete solution in those cases where devices overlap, resulting in merged markers.

One approach that provides adequate device verification is simply to re-render the intentional shape to the placement in context. If no changes are found, then designers know the placed device matches the intended source device. There are several techniques that can be used for this comparison, ranging from complex pattern matching to regenerating devices based on optical equations.

Photonics fill solution

PIC fill requirements vary from EIC fill requirements in one important aspect—the shape of the fill. When traditional EIC square fill shapes are used in a PIC layout, they cause hybrid modes in nearby waveguides. These hybrid modes add noise to the signal in the waveguide, and cause the power to disperse across various modes. To solve this issue, PIC fill shapes must have a circular profile. However, fill shape is only one contributing factor to dispersion of the optical signal. In PIC layouts, fill proximity is not just a factor in the manufacturing resolution, but also the source of possible electromagnetic (EM) coupling with waveguides. Using an EDA fill tool like the Calibre YieldEnhancer with SmartFill tool with advanced fill optimization capabilities enables designers to automatically and optimally insert circular fill around the waveguides in a PIC layout.

Photonics design implementation

With the advances in PIC physical and circuit verification in place, the focus can shift to design creation. In the EIC domain, millions of electrical devices can be quickly integrated into a large circuit while optimizing for parameters such as performance, power, area and more. To make that leap for PIC design, a similar automated design flow is needed for PIC assembly and generation. Innovative tools like the LightSuite Photonic Compiler tool provide PIC designers the ability to connect thousands of optical components and their associated electrical routing. Because the LightSuite Photonic Compiler tool also simultaneously validates Calibre signoff DRC rules while preserving the intended design connectivity, the number of verification and correction iterations required to achieve tapeout is greatly reduced, enabling PIC design teams to deliver designs on schedule, with confidence.

Conclusion

The growing market for silicon photonics circuits has led to the need for reliable, automated physical and manufacturing verification process flows that address the unique physical characteristics of silicon photonics designs. Fortunately, EDA companies have recognized that there is no need to invent new tools, or even reinvent the tools and processes already in place for EIC verification. By expanding and adapting the use of established functionality, like equation-based DRC, automated waiver processing, and smart fill optimization, EDA companies have enabled their tools (at least initially) to accommodate the new components and design concepts of silicon photonics designs, and provided PIC designers with an automated and standardized path to tapeout.

While there are still more challenges to overcome before a complete solution is devised for PIC design and verification, these initial solutions serve to illustrate that there are still many untapped ideas for reusing existing EDA tools for new purposes, providing room for even more innovative solutions moving forward.

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