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Physical verification for silicon photonics:

Challenges and solutions

Executive summary

The growing market for silicon photonics circuits has led to the need for reliable, automated physical verification and manufacturing verification process flows that address the unique physical characteristics of silicon photonics designs. Expanding the use of established functionality like equation-based DRC, shape-matching LVS, and litho-friendly design enables designers to accommodate the new components and design concepts of silicon photonics

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Introduction

In the early days of optical circuit research, there were visions of a silicon-based optoelectronic integrated circuit (IC), containing a variety of optical components that would perform light generation, modulation, manipulation, detection, and amplification. This research concentrated on III-V compound semiconductors, such as gallium arsenide (GaAS) and indium phosphide (InP).

While the investigation into such materials was (and is) interesting, there is no doubt that silicon is the dominant semiconductor material in electronics applications, due to its highly desirable physical attributes and ready availability (inexpensive, well understood, high-quality oxide, etc.). These circumstances redirected optical circuit research towards monolithic superchips, in which optical and electrical components could be integrated on the same chip (figure 1), leading to the evolution of the field of silicon photonics in the 1980s.

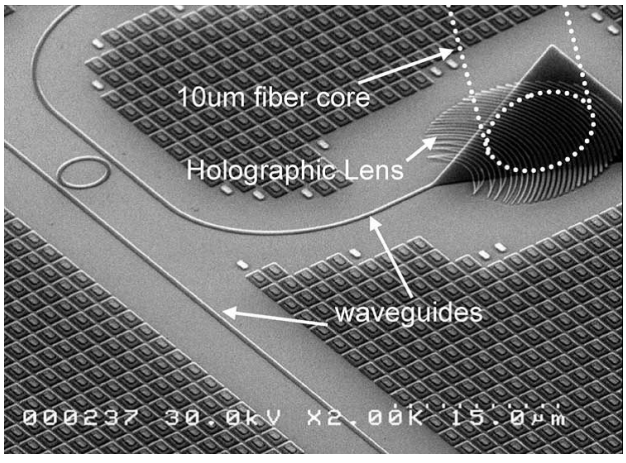

Figure 1: Microscope photograph of SOI integrated photonic test network, including mirroring filter and fiber-to-waveguide coupler (reprinted courtesy Dr. C.Gunn)[1].

During the 2000s, silicon photonics witnessed a ramp-up of investment in research and development, and the launch of multiple initiatives (AIM Photonics, COSMICC, PETRA, etc.) to support these efforts. The global silicon photonics market is now expected to grow at a rapid growth rate of 20.34% over the forecast period 2017-2022[2]. The factors driving the growth of this market include price, capability, and size. As the price of silicon photonics technology continues to fall, demand is significantly increasing across multiple vertical industries, including healthcare, telecommunication, and defense.

This growing market for silicon photonics chips increases the need for a solid, stable physical verification platform for silicon photonics designs. In turn, that need exposes the disparity between the IC manufacturing world, with its long-established and proven environment of processes and tools that support traditional silicon design verification, and the new silicon photonics technology, which introduces novel and challenging verification requirements. This divergence opens up opportunities for electronic design automation (EDA) companies to use their tools' functionality in new ways to achieve a verification flow that can assess the electric and optical behavior of photonics designs, similar to the existing verification flows for electronic ICs. A step further would be the integration of electronic and optical layout implementation tools.

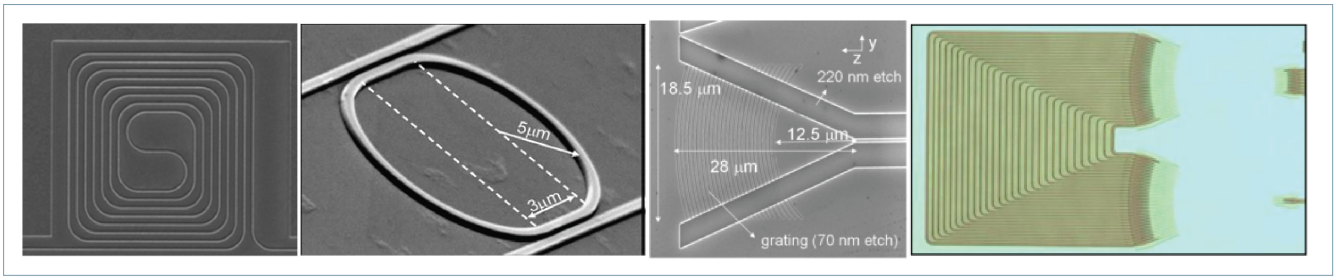

Figure 2: Images of silicon photonics components.

Silicon photonics design

Silicon photonics designs are different from electronic IC designs in one very critical element— the geometrical construction of basic components. Electronic ICs use a Manhattan geometry; circuits are designed in an orthogonal fashion, on a rectangular grid that only allows for 0°, 45°, and 90° angles. In contrast, silicon photonics designs include a wide variety of curvilinear structures, such as delay lines, ring resonators, waveguides, grating couplers, etc. (figure 2).

Another disparity between electronic ICs and silicon photonics designs is the lack of a circuit schematic. Silicon photonics designs do not use traditional design schematics, which makes the concept of classic layout vs. schematic (LVS) verification a foreign notion to photonics designers. However, it is still critical to ensure that photonics circuit ports are properly connected to electronic circuit nodes, and to enable device and device parameter recognition.

Physical verification challenges

The geometrical integrity of an electronic IC design is measured by design rule checking (DRC), which determines if the design's physical layout complies with the manufacturing requirements (design rules) set by the foundry. Because traditional electronic IC designs consist of Manhattan shapes placed on a rectangular grid, the measurement of various geometrical parameters is fairly straightforward, and accuracy can be quite precise.

In photonics ICs (PICs), placing curvilinear structures on a rectangular grid presents a challenge for existing electronic IC verification tools and processes (figure 3). Precise measurement is problematic due to edge and vertex snapping, which can occur when the vertices of the curved shapes must adapt to the precision of piecewise linear approximation.

This effect must be compensated for during the geometrical parameter measurements. Extraction and careful validation of those non-traditional shapes requires new parameters, such as bend curvature andcurvilinear path length. Reconstructing or reinventing an entire PIC toolset and verification flow to fit such structures is unrealistic, given the time and resources that would be required. Alternatively, the EDA industry has developed new PIC verification techniques that can achieve the required degree of accuracy with modest modifications to existing electronic IC toolsets.

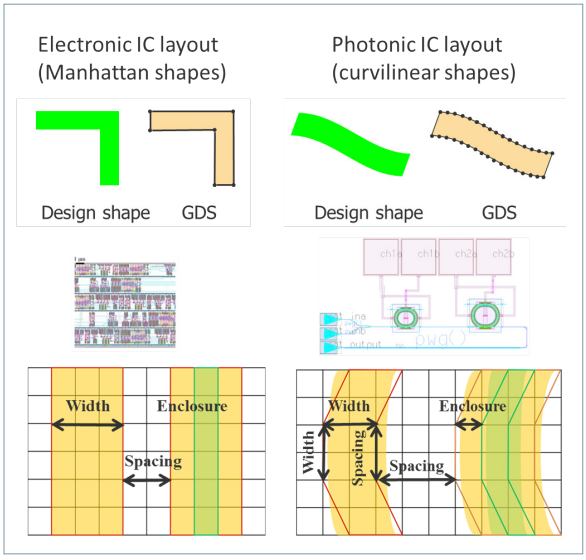

Figure 3: Physical verification challenges over curvilinear structures.

A useful addition to the PIC verification toolset is equation-based DRC, which can apply complex conditional DRC with multi-dimensional tolerance values in place of traditional DRC arithmetic calculations. Without the use of equation-based DRC, PIC physical verification generates many false errors, due primarily to edge snapping or rounding errors during measurements (figure 4).

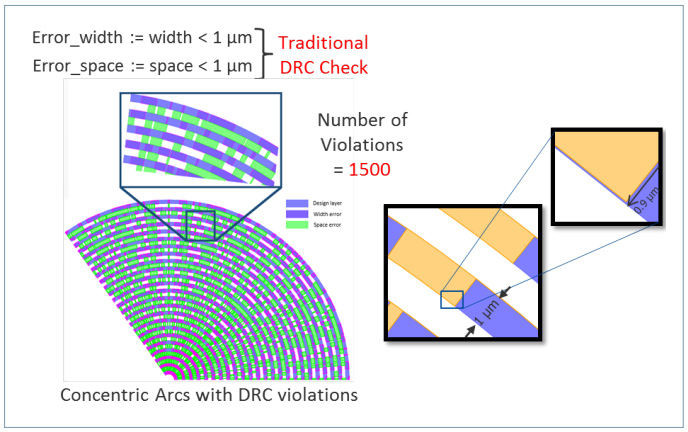

Figure 4: Using traditional DRC over curvilinear structures.

To filter out these false violations, the Calibre® eqDRC™ functionality enables designers to add equation-based DRC to traditional DRC checks to detect the curved segments of the design and apply the necessary tolerance factors to eliminate the false errors. The introduction of equation-based filtering and checking enables a whole new range of DRC capabilities for silicon photonics, where multi-dimensional equations can be evaluated to check the geometric validity of photonics designs (figure 5).

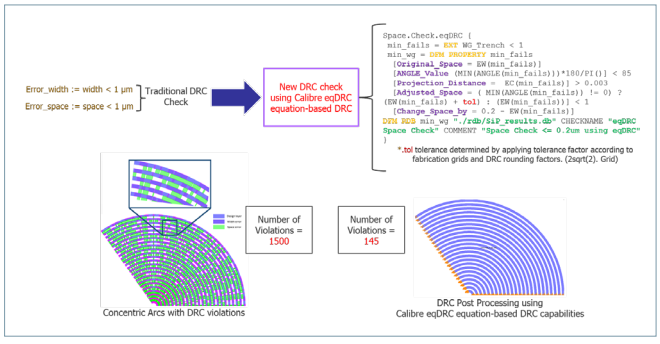

Figure 5: Using Calibre eqDRC equation-based functionality over curvilinear structures reduces false violations[3].

However, as the maximum edge length gets smaller, more edges are needed to represent a single polygon. Because DRC verification tools are edge-based, as the number of edges increase, the tool runtime also increases. Designers must confront the conflict of using a large number of edges to accurately represent photonics components vs. the possible runtime impact. To perform proper DRC for PIC layouts more efficiently, PIC designers must adopt a new coding style, in which the maximum edge length plays a significant role in performance tunability vs. results accuracy. In some physical verification tools, such as the Calibre nmDRC™ platform, runtime may not incur any significant impacts, due to the multiple runtime optimizations the Calibre platform uses for full-chip runs, such as hyper-scaling and hierarchical injection. However, runtime impact should always be considered when developing DRC process design kits (PDKs) for silicon photonics.

Circuit verification challenges

Another challenge in building a silicon photonics design flow is the absence of a SPICE source netlist. Electronic IC schematic capture and simulation (design, automated layout, layout vs. schematic [LVS], parasitic extraction [PEX], re-simulation...) are heavily dependent upon SPICE circuit simulation, but there is no generically-equivalent silicon photonics simulation approach. TCAD-like tools are used for accuracy, but are capacity/performance limited, due to the lack of a common format for verification and validation across the flow.

The waveguides in PICs act as an optical interconnect between various circuit components, but are also the building blocks of most PIC devices. Unlike interconnect in electronic ICs, waveguides must be treated as devices instead of as ideal interconnect, due to the difference in the concept of connectivity in photonics. The parameters of a waveguide play a pivotal role in its operation, owing to their impact on the modes propagating the waveguides. Also, simple electronic concepts such as shorts and opens are different in photonics design. For example, two waveguides might overlap, creating a four-port network, without resulting in a shorted interconnect (figure 6).

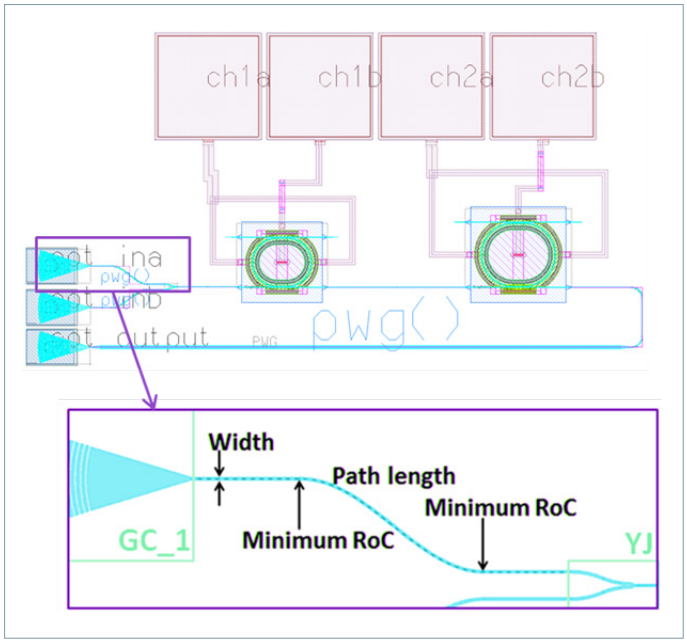

Figure 6: Extraction of device parameters in LVS.

Comparing a classic electronic LVS flow to the photonics LVS requirements can help determine the missing LVS components. As shown in table 1, the missing parts are optical connectivity and the validation of curved design shapes. Optical connectivity and photonic device functionality are validated through parameter extraction and comparison: width, curvilinear path length, and bend curvature, with the limitation being that we must assume a curve type for said curve (e.g., circular arc, Bessier, adiabatic, etc.).

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Table 1 - Classic LVS vs. Photonics LVS

Classic Electronic LVS	Photonics LVS
√ Device type and count	√ Device type and count
√ Connectivity	? Connectivity (optical)
√ Device parameters	? Validate curved shapes (photonic devices and waveguide interconnections)

device functionality are validated through parameter extraction and comparison: width, curvilinear path length, and bend curvature, with the limitation being that we must assume a curve type for said curve (e.g., circular arc, Bessier, adiabatic, etc.).

Traditional LVS would extract the assumed curvature and match it to a source. Shape-matching LVS, a new method of validating curvilinear design, starts with the source and validates curvature (figure 7). Table 2 describes the difference in parameter extraction between traditional LVS and shape-matching LVS.

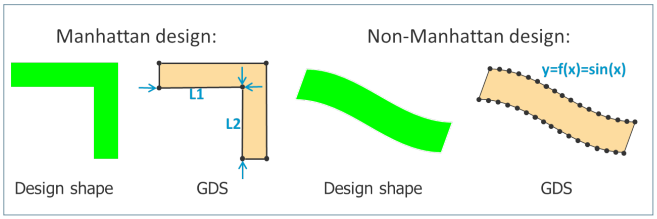

Figure 7: Shape-matching LVS.

Table 2 - photonics parameter extraction

Design example	Critical metal line	Critical waveguide interconnect
Festures to be extracted and/or validated	Width, Length	Design shape
Netlist	Instance pinA pinB Width Length	Waveguide instance pinA pinB + side-file

As for methods used to match device shapes, multiple options exist:

- Re-instantiation of Pcell, where Pcell is overlaid to the intended location and XORed, which will find differences/error due to placement.
- Pattern matching, which is easy to implement, but requires at least some Manhattan edges for matching. There is also a need to determine allowed tolerances and how to extract parameters based off these tolerances.

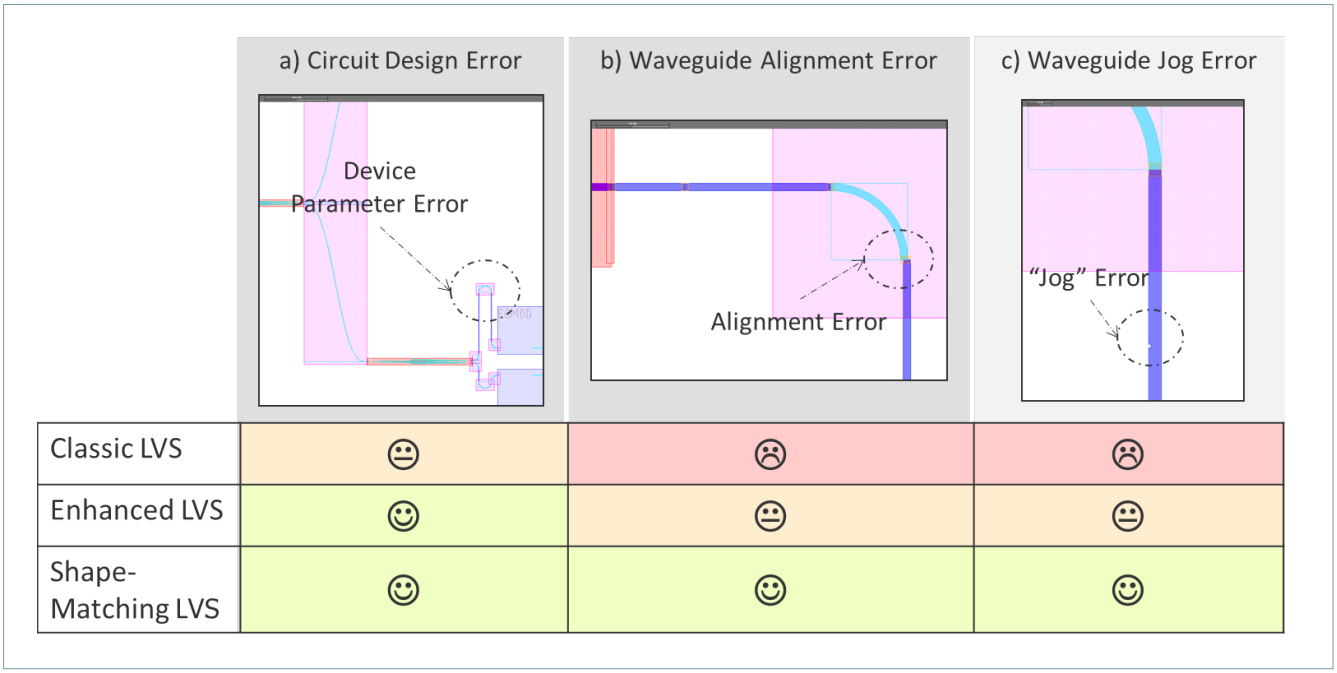

Figure 8: Comparison between various LVS techniques for silicon photonics.

A comparison between classic LVS, enhanced LVS, and shape-matching LVS in figure 8 shows the superior coverage of shape-matching LVS.

Litho-friendly design simulation

Historically, IC design processes, particularly at older nodes, assume that what is drawn is what will be delivered (mask to silicon). At advanced nodes, to compensate for the finite size of the lens (which does not capture all the mask diffraction order), lithography techniques such as optical proximity correction (OPC) must be used to modify the layout before manufacturing to ensure it will comply with the original drawn intent.

For silicon photonics, it is crucial that designers properly model the final shapes of the circuit, due to the direct impact on circuit performance. For multi-project wafer (MPW) runs, designers typically require multiple iterations of physical device manufacturing to understand and improve the circuit behavior (figure 9). However, physical iteration is very time-consuming and extremely expensive.

Alternatively, designers can take advantage of litho-friendly process design kits (PDKs) supplied by the foundry. Foundry lithographers and technology access groups (TAGs) use litho-friendly design (LFD) software

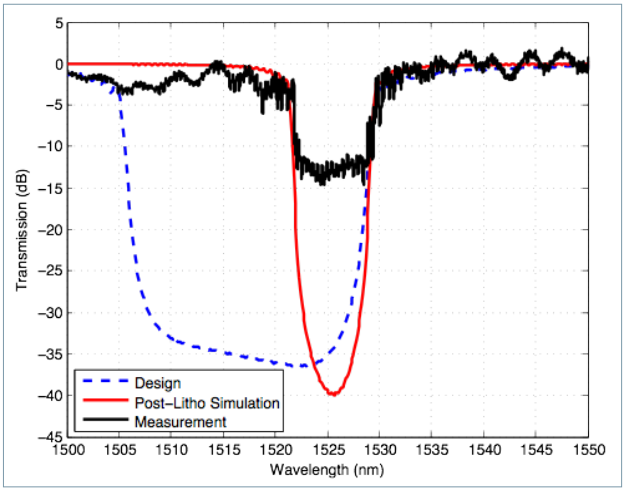

Figure 9: Fabricated Bragg waveguide bandwidth is smaller than design intent bandwidth.

like the Calibre LFD™ tool to develop these PDKs. Using the Calibre LFD tool in conjunction with an LFD PDK enables designers to perform a variety of process simulation checks (previously only available to lithographers working in semiconductor foundries) that can identify potential lithographic resolution issues prior to tapeout (figure 10). Design teams can then apply the necessary design modifications or OPC techniques to

ensure manufacturability and performance. With access to an automated virtual lithographic process, designers can shave months from their schedules while avoiding spending money on silicon that does not meet design intent.

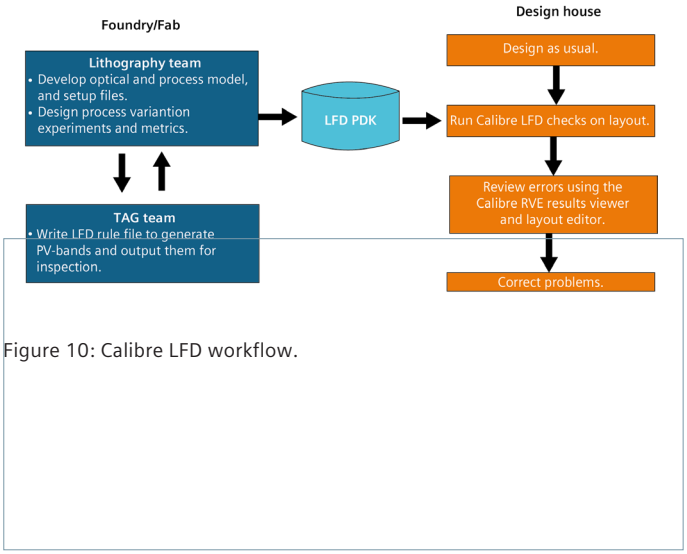

Figure 10: Calibre LFD workflow.

Conclusion

The growing market for silicon photonics circuits has led to the need for reliable, automated physical verification and manufacturing verification process flows that address the unique physical characteristics of silicon photonics designs. Fortunately, there is no need to reinvent the tools and processes already in place for electronic IC verification. Expanding the use of established functionality like eqDRC, shape-matching LVS and litho-friendly design enables designers to accommodate the new components and design concepts of silicon photonics designs.

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