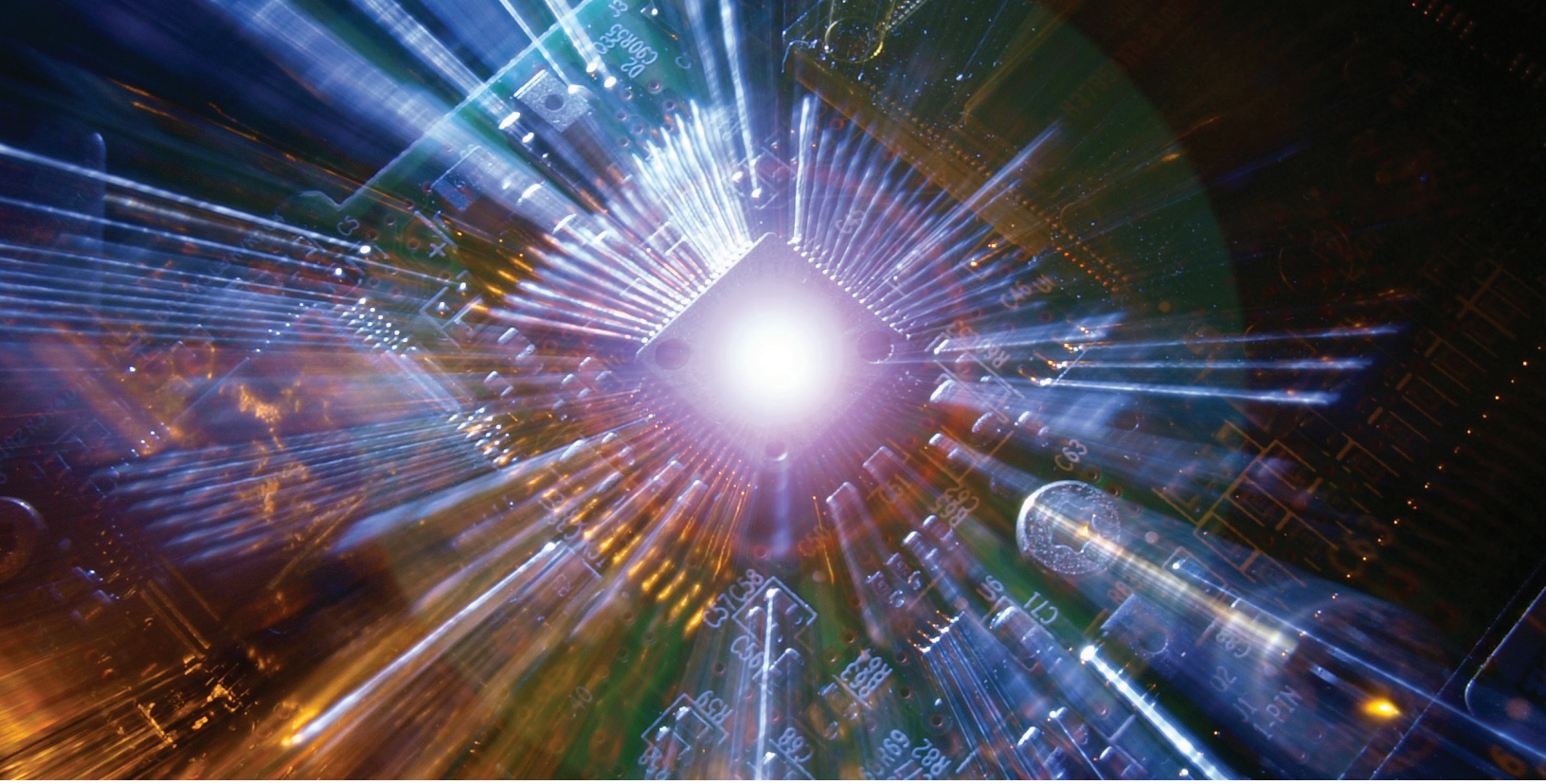

DIGITAL INDUSTRIES SOFTWARE

Siemens EDA's full-flow portfolio helps engineers achieve optimum IC design verification efficiency

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Contents

Introduction

Designers demand an integrated set of tools that run seamlessly from front-end to back-end design. The Siemens EDA full-flow portfolio provides the tools to perform all essential tasks required in an analog/mixed-signal integrated circuit (IC) design. A quick overview of the front-end flow using the S-Edit schematic capture environment will be covered in this white paper, followed by a more detailed description and steps for using the Analog FastSPICE™ (AFS) platform simulator to go through the verification of a basic amplifier design.

S-Edit

S-Edit seamlessly integrates with all Siemens simulator offerings through an intuitive and highly customizable GUI. S-Edit is very easy to use out of the box, eliminating the steep learning curve often required when switching tools. The comprehensive and customizable toolbar at the top of S-Edit enables easy access to many design entry shortcuts and accelerates productivity as there is no need to look under complicated sub-menu and drop-down options. The libraries and cells associated with the design, the command window, and properties associated with an instance or test bench are conveniently located in S-Edit and can be detached and easily reconfigured to suit any work style or display area.

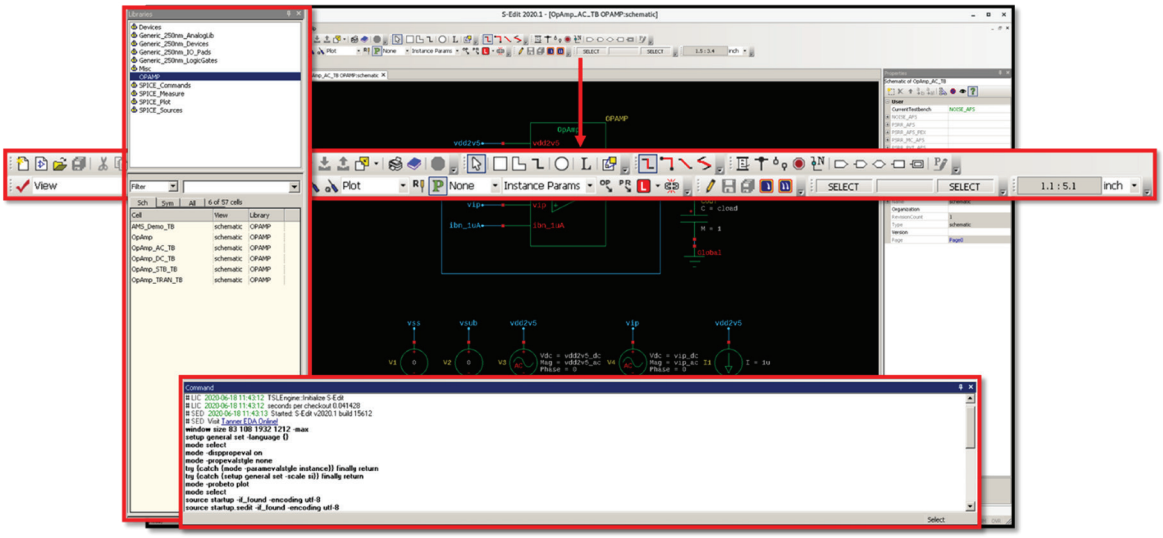

Figure 1: S-Edit schematic capture environment.

Op Amp design

A simple schematic is drawn in S-Edit for an eight transistor, two-stage operational amplifier (op amp) design implementation. The dummy devices are drawn at the bottom to construct a complete rectangular, common centroid layout for the NMOS current sinks.

A simple DC test bench for an output compensated amplifier in unity-gain feedback configuration is shown in figure 3 for the op amp design.

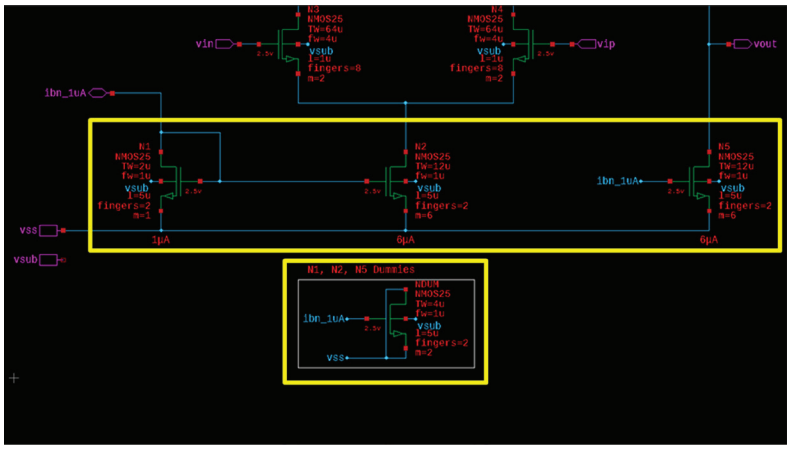

Figure 2: Schematic of a two-stage operational amplifier.

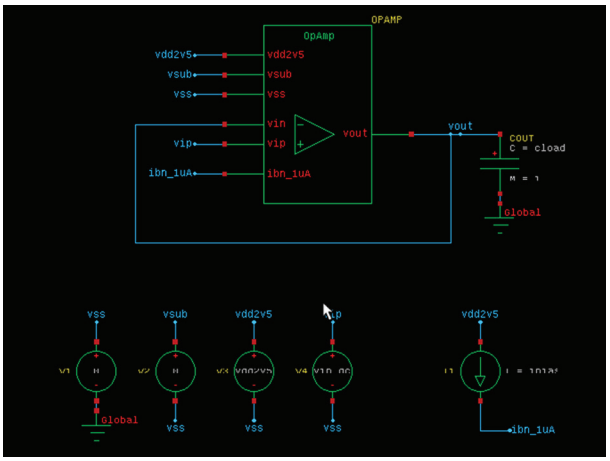

Figure 3: DC test bench.

Simulation Setup

Simulation Setup

The Simulation Setup allows the user to set up options and simulation test benches for various types of analysis and can be launched using the relevant toolbar button as shown in figure 4.

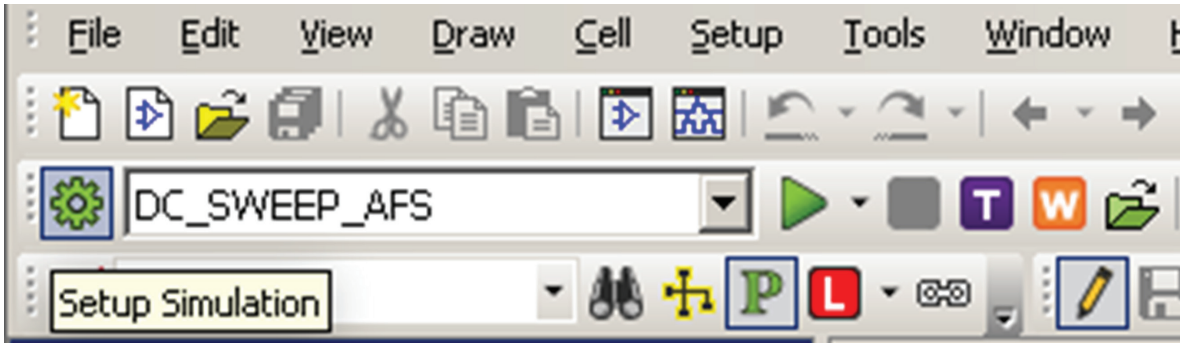

Figure 4: Menu icon to launch Simulation Setup menu.

From the Simulation Setup menu, test benches can be created using the Sim test bench pulldown. Once a simulator is selected, all relevant simulation options and analysis on the GUI adapt accordingly. S-Edit supports three simulators: T-Spice, Eldo™, and AFS. For this design several DC simulation test benches have been created. A schematic test bench can be associated, with several different simulation test benches, all created, renamed, copied and saved under this menu.

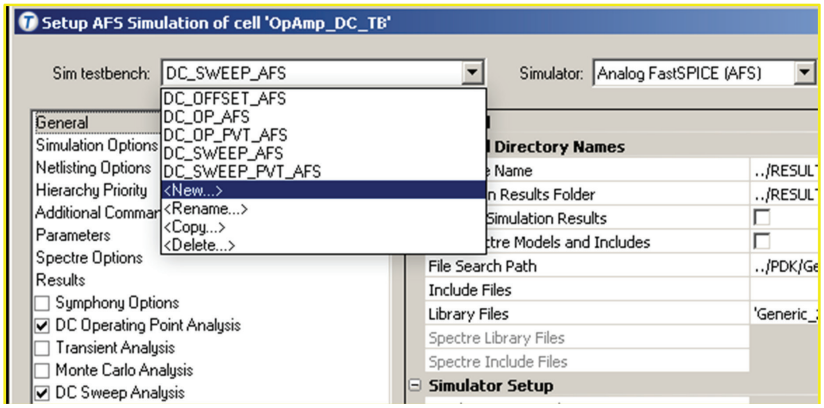

Figure 5: Simulation test bench setup for DC Sweep analysis.

It's worth noting that there are no hidden options or popup menus, and everything is shown on each corresponding sub window in the Simulation Setup. For example, the Simulation Options sub menu for AFS is shown in figure 6. Selecting an option shows a brief description from the user manual at the bottom. But let's look at each page analytically.

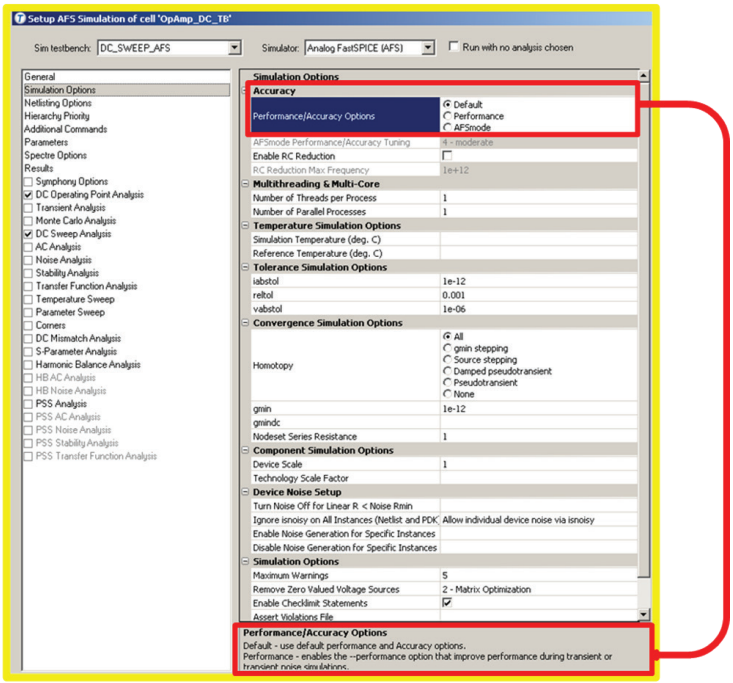

Figure 6: Simulation Setup menu with help.

General options

The general options are where simulation netlist results and related files are generated and stored. Industry-standard models are supported and the definitions to the libraries are included on this page. This is a simple DC simulation test bench using typical Spice models of internal Siemens EDA generic process design kits (PDK). The ability to save all simulation results, time-stamped accordingly, or the ability to keep overriding existing ones is set on this menu.

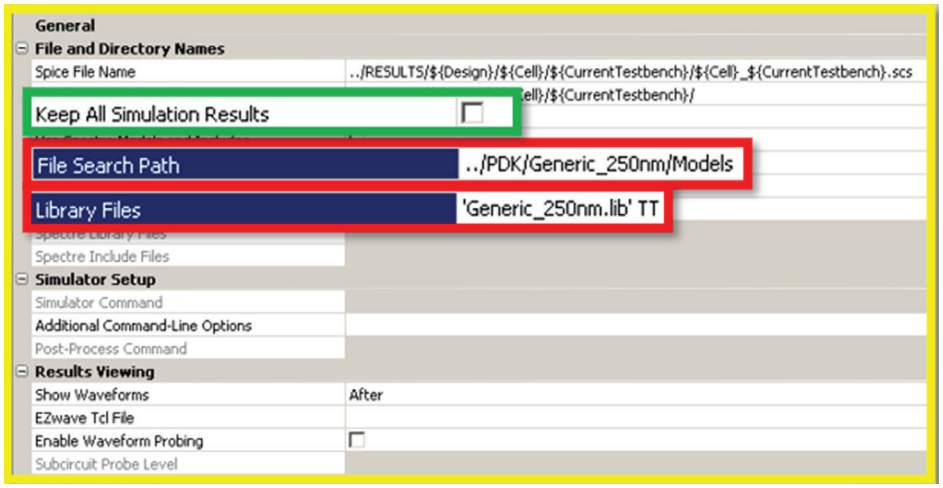

Figure 7: General setup for simulation.

Hierarchy priority

The hierarchy priority page will supersede the hierarchy setup in the schematic (selected by right clicking on an instance to select the view). The actual view type can be different on multiple instances of the same cell throughout the schematic hierarchy and can be easily selected by right-clicking on the schematic directly. The default hierarchy priority is Schematic, SPICE, Verilog-A, Verilog-AMS, Verilog, VHDL-AMS and VHDL.

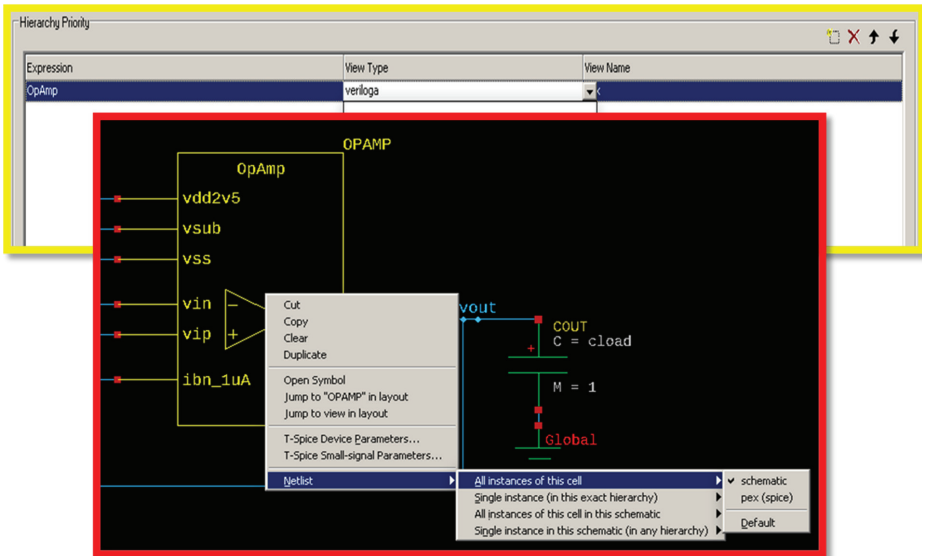

Figure 8: Hierarchy priority menus

Parameters

The Parameters page is where all design variables and parameters are entered. You can easily enter a new parameter by clicking on the corresponding button and filling out at a minimum the Name and Value fields. Holding down the control key when pressing the same button automatically imports all variables found in a design.

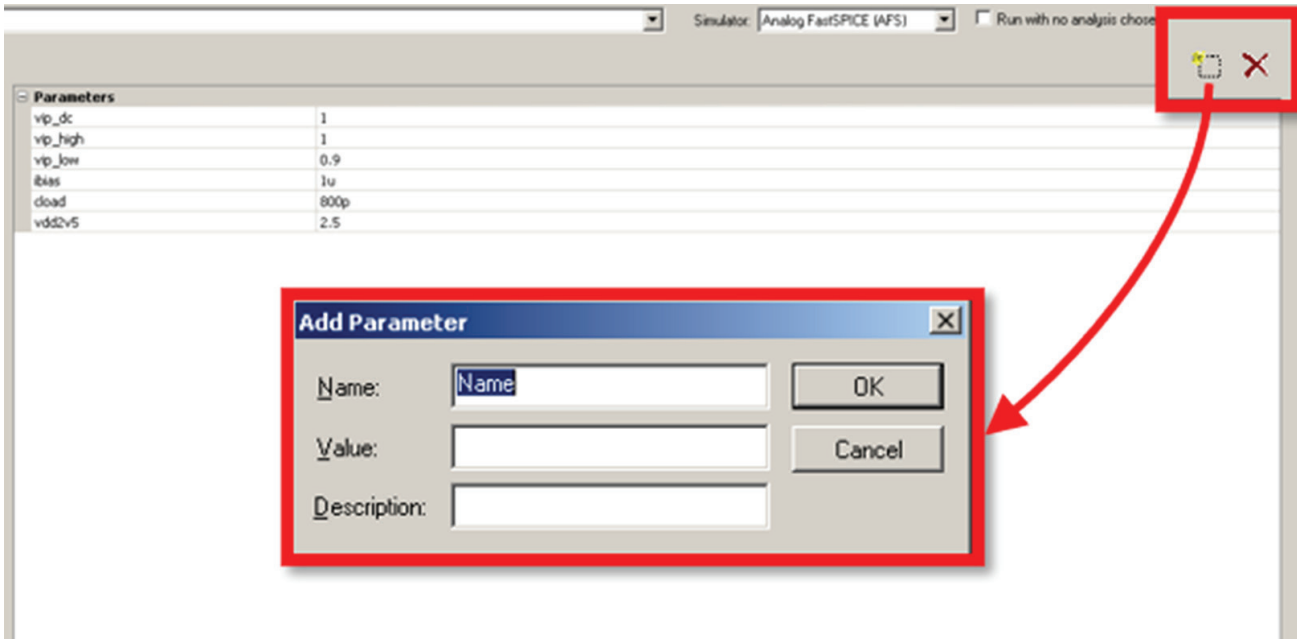

Figure 9: Menu to set up parameters for simulation.

DC OP and sweep analysis

All simulator related and supported analyses options can be selected through the checkboxes on the Simulation Setup GUI and stored in various simulation test benches. In figure 10, a simple DC OP simulation and DC sweep analysis are carried out. The positive input voltage of the amplifier is swept from 0.4 volts to 0.8 volts in steps of 100 µV, ultimately checking to see if the N2 tail current sink is pushed into a linear region at low voltages or not.

The amplifier's tail current sink, N2, as shown in figure 2 must be in saturation to be a proper current sink. If N2 goes into linear region, it acts as a resistor (not a current sink) and the amplifier performance starts to degrade. N2 is in saturation when N2_Margin=Vds-Vdst > 0 (most designers allow enough margin, so at least 50mV instead of 0). By sweeping the positive input voltage of the amplifier (the amplifier is in unity gain feedback) from a very low voltage to something higher, we can quickly identify the minimum input voltage we can get away with for N2 to be saturated.

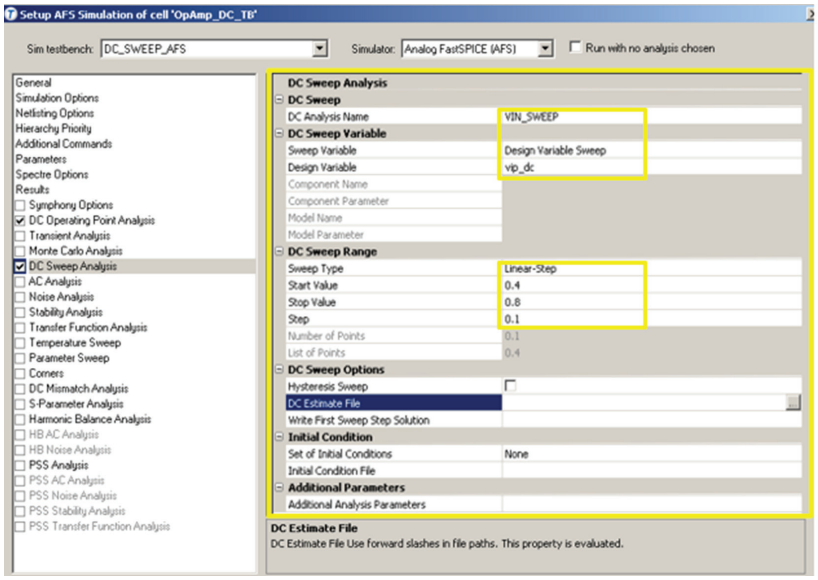

Figure 10: DC Sweep Analysis setup.

Running a simulation

When all simulation test bench customizations are finished, you can simply run a simulation or click OK to save the changes. The simulation netlist can also be generated and viewed before a simulation is run simply by clicking on the "T" button in the toolbar. The simulation can also be launched from the S-Edit toolbar.

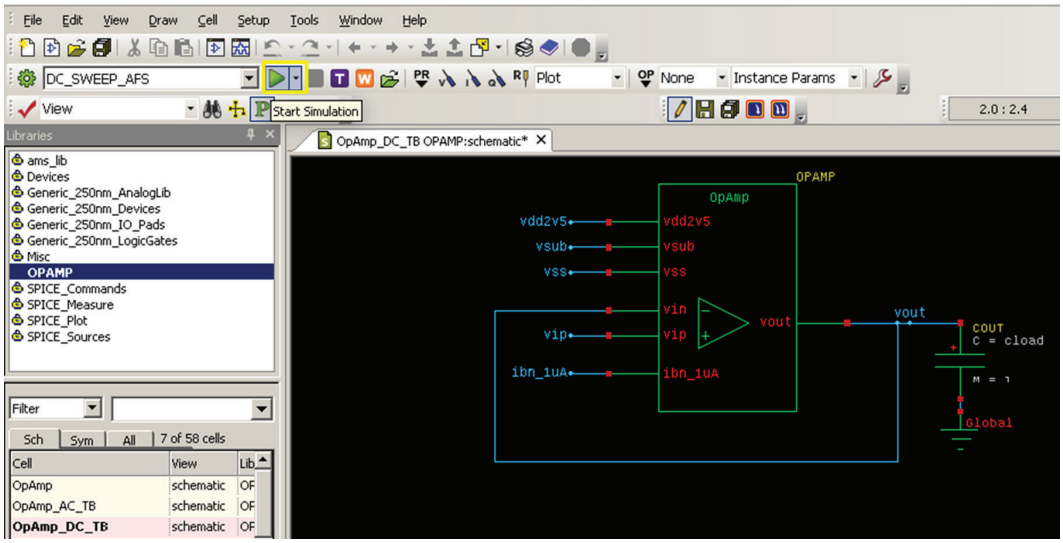

Figure 11: Start simulation icon.

Simulation netlists and log files

Regardless of the format choice of the simulation models, S-Edit exports a netlist and then launches the AFS simulation in the background. While the simulation is running, the simulation status and AFS log file are printed in the command window. When the simulation is finished, links to the netlist, log file and results directory are shown in the command window alongside the simulation statistics. Clicking on the netlist opens the simulation netlist in the S-Edit text viewer. While clicking on the log file link, the log file opens in a separate text viewer tab.

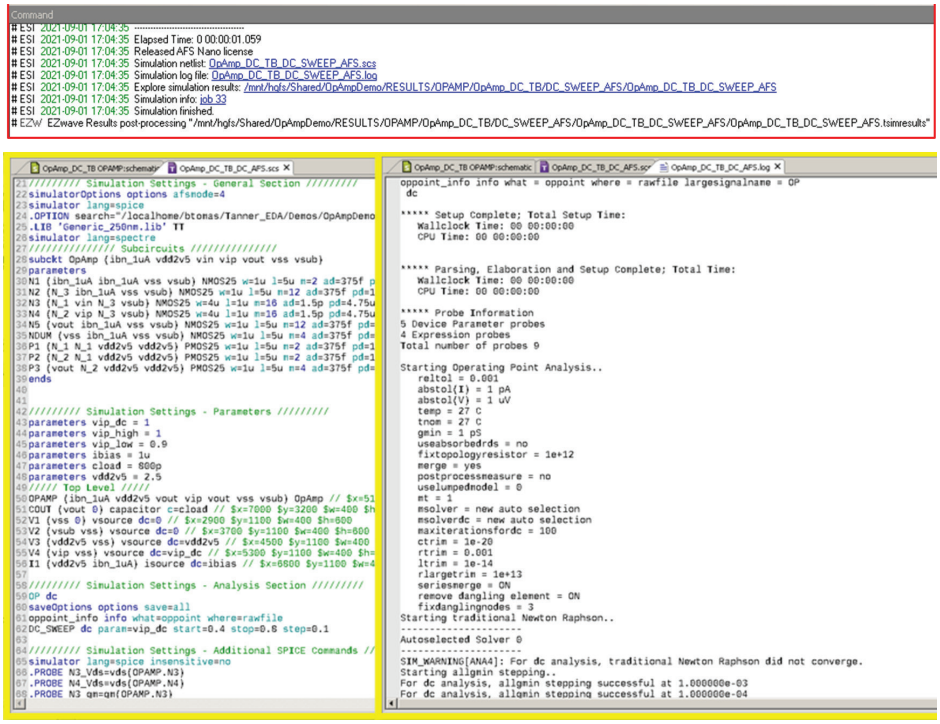

Figure 12: Simulation netlists and log files.

DC sweep simulation results in EZwave

EZwave™ is the default waveform viewer and results postprocessor for AFS and is immediately launched after an AFS simulation finishes. Expanding the DC sweep simulation database shows all available results and measurements taken from the simulation. Plotting measurement N2_margin across the input voltage sweep shows that the tail current sink N2 is saturated for any input voltage higher than approximately 521µV. As the input voltage gets lower, so does the tail voltage of the amplifier (i.e., the drain of N2) which reduces the Vds of N2 and hence N2_Margin. Visual Distress Signal = Drain-Source voltage, Vdsat = Saturation voltage, gram = Transconductance. It's nice to show what happens to the gm of N3 (this is the amplifier input device) when the input voltage (vip) is too low, and as a result N2 is in the linear region (i.e., not a good current sink, if at all a sink). N2 is in the linear region when N2_Margin < 0V or so.

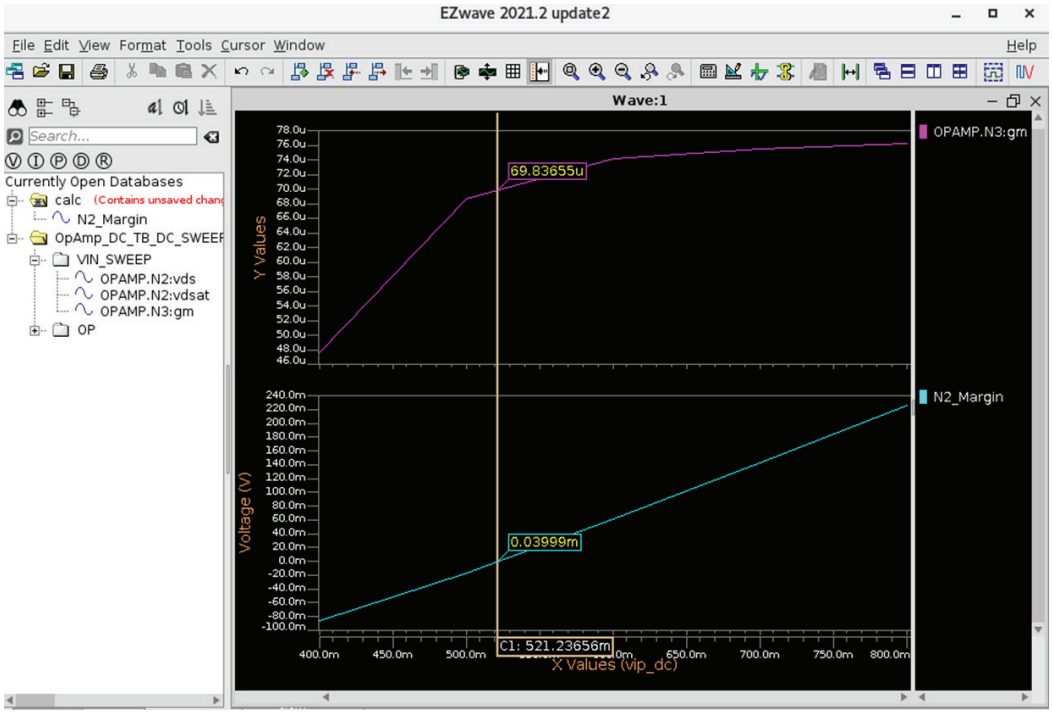

Figure 13: DC sweep simulation results in EZwave.

EZwave comes with an advanced calculator for the postprocessing of results. The calculator can be accessed through the menu or relevant toolbar button. It features loads of built-in functions, such as Measurements, Signal Processing, and Statistical, to mention a few. A waveform can either be dragged and dropped into the calculator from the database navigator or directly from a graph.

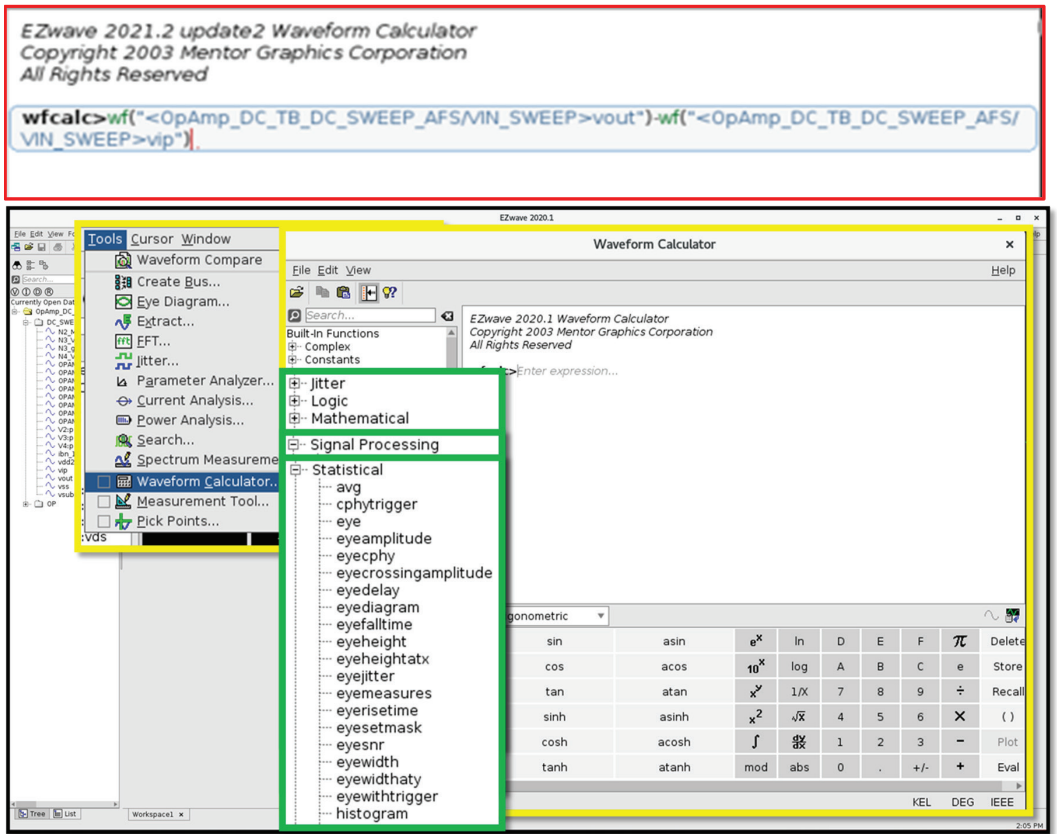

Figure 14: EZwave Waveform Calculator.

Expressions can easily be constructed, in this case the output voltage minus the input voltage to get the systematic offset of the amplifier across the DC Sweep, and evaluated. The output voltage and the offset voltage graphs are appended as shown in figure 15, where name and other visual effects can easily be changed to the desired ones.

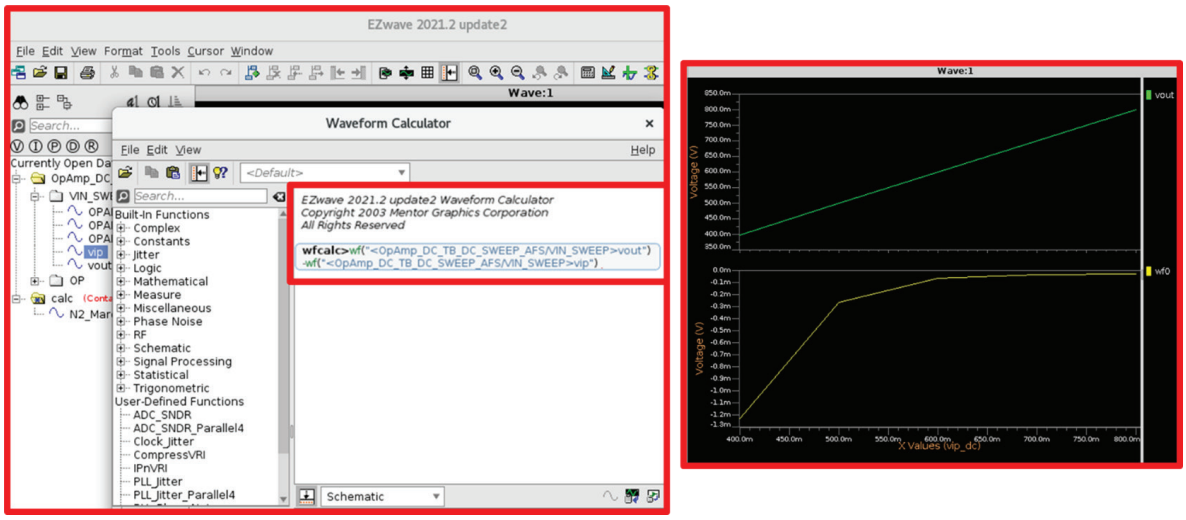

Figure 15: Output voltage and systematic offset waveforms.

Results back annotation

Once a simulation is run, the DC OP voltage or current can be back annotated on the schematic. This can be done using the toolbar dropdown menu and selecting voltage or current. The node voltages are back annotated, and the currents show that this op amp consumes a static current of 13µA.

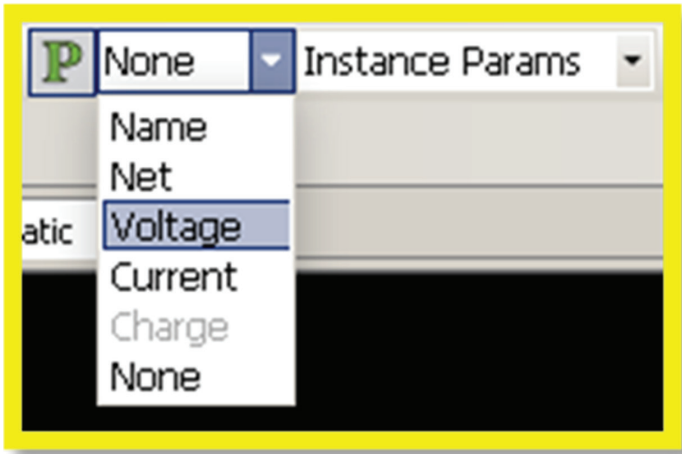

Figure 16: Results back annotation.

In addition, small-signal parameters can be back annotated using this toolbar icon. All relevant parameters and device region information are shown for the op amp. All available data set results associated with the simulation test bench can be accessed and switched to using this toolbar icon.

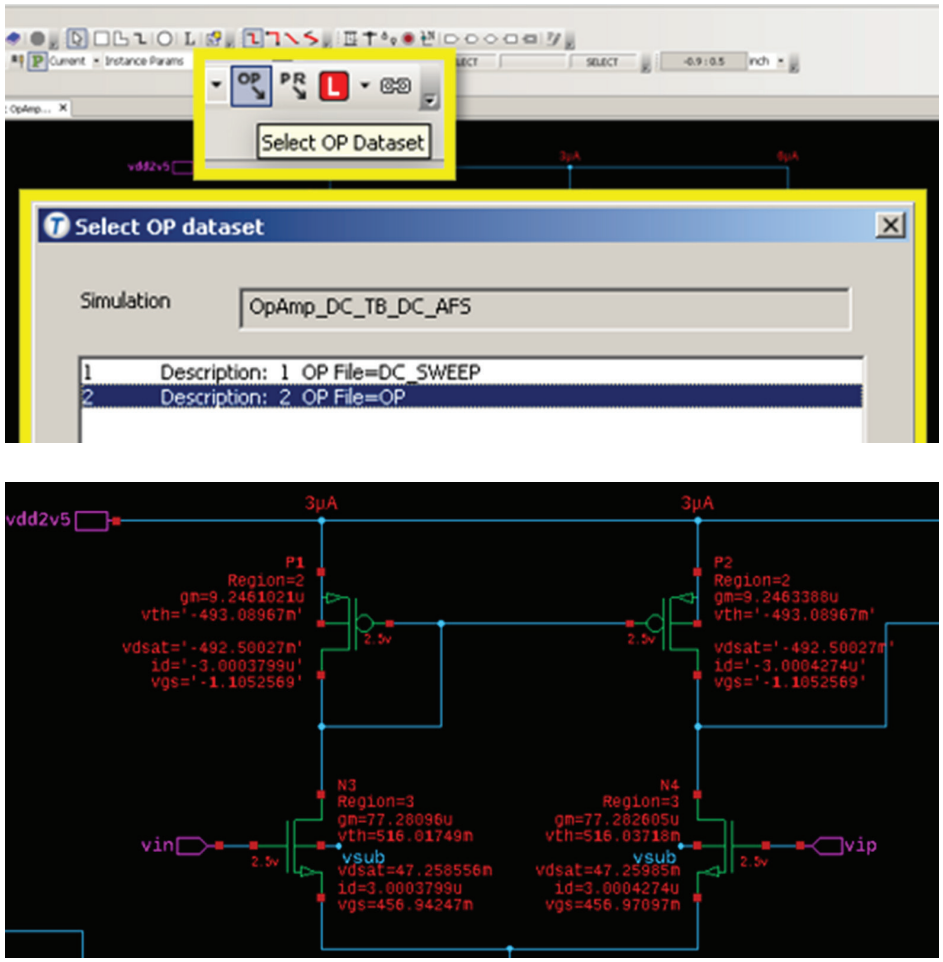

Figure 17: Small-signal parameters back annotation.

Seamless EZwave calculator integration

In the Simulation Setup GUI launched directly from the schematic test bench, there is a new Results pane which integrates the EZwave calculator seamlessly for any advanced expression and output measurement construction during design.
Net voltages and node currents to be saved or plotted are easily selected using the toolbar icons and stored under the corresponding signals section in the Results pane.

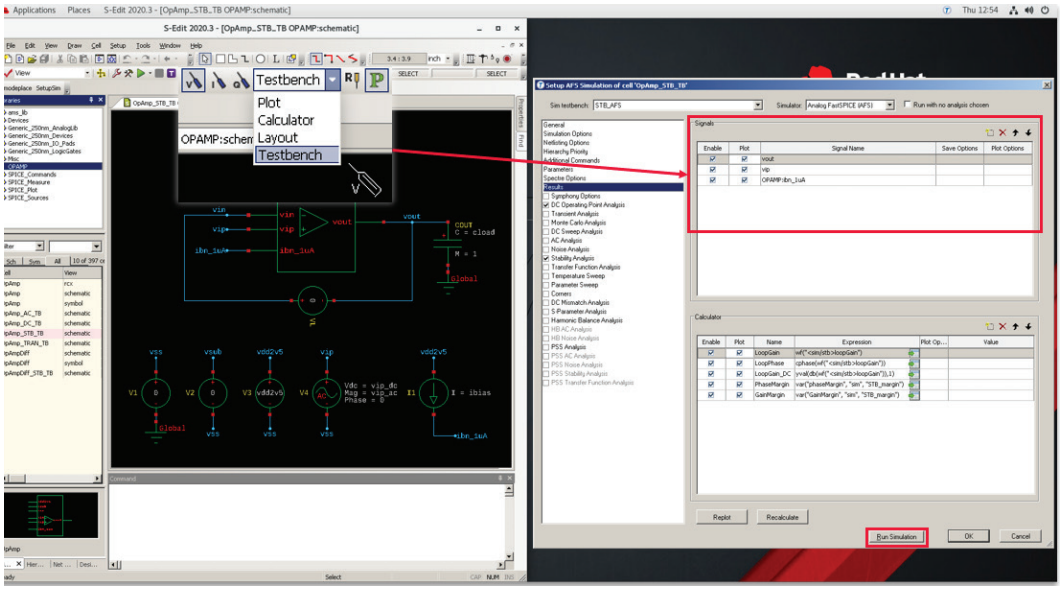

Figure 18: Seamless EZwave calculator integration.

After a simulation is run, EZwave pops up and plots the expressions from the Results pane that evaluate a waveform. Scalar results, like the phase margin or the DC loop gain, are also evaluated and shown in the same pane.

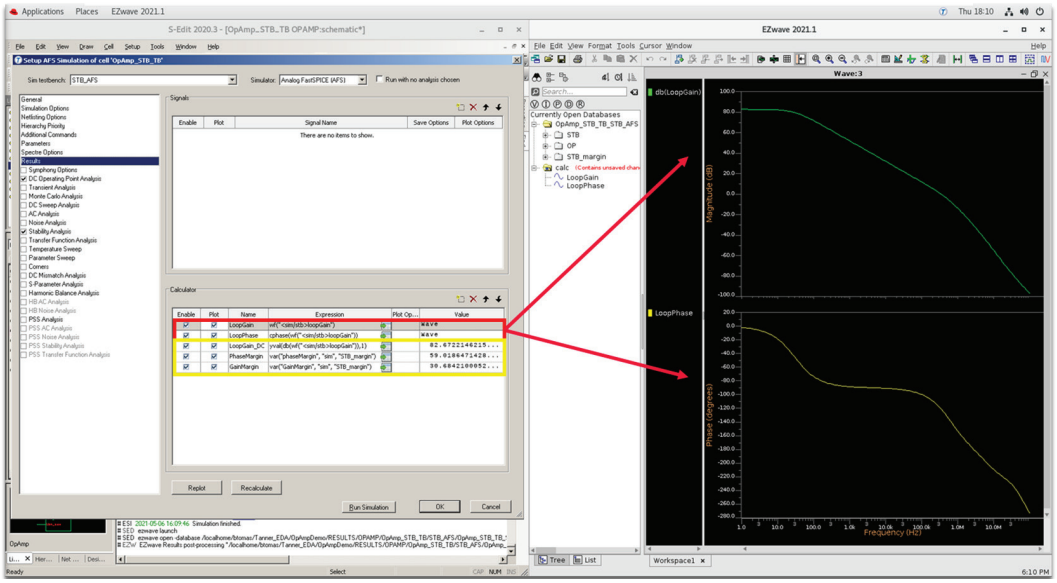

Figure 19: EZwave plots from calculator expressions.

An expression can be sent to and from the calculator for further editing or be manually modified in the Results pane. Right-clicking on an expression and selecting recalculate evaluates a new measurement. All scalar expressions and waveforms can be re-evaluated and plotted again at any point, providing that the results are present.

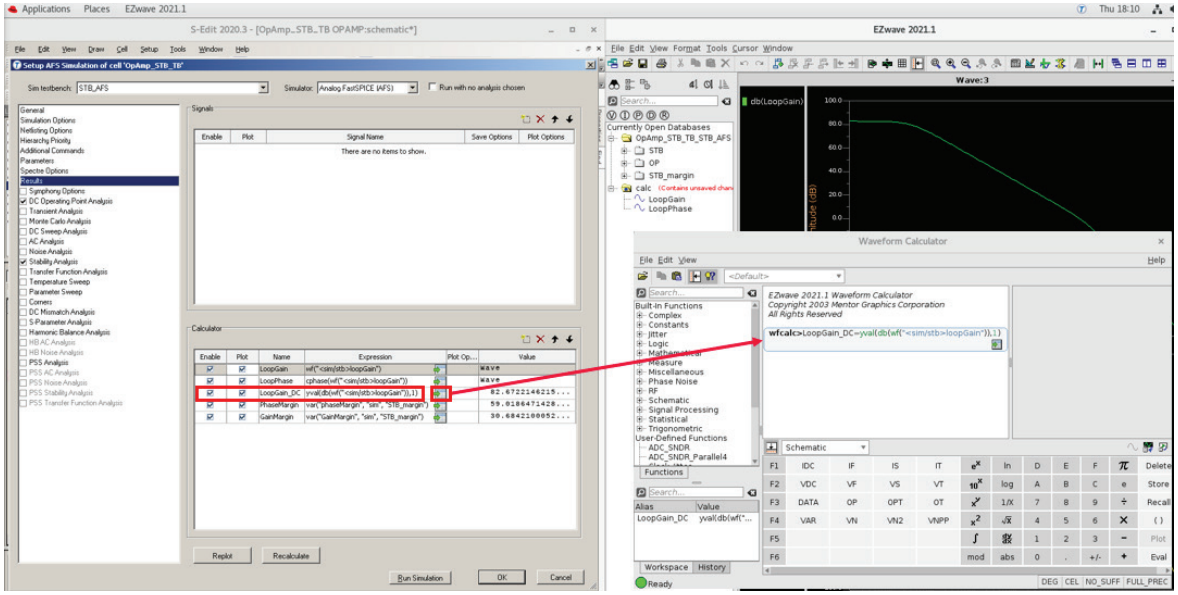

Figure 20: Menu to send expressions to EZwave for recalculation.

Monte Carlo simulation setup and results

A Monte Carlo simulation using the initial DC schematic test bench is set up using the corresponding simulation test bench selected under the same Simulation Setup menu. A mismatch on a Monte Carlo simulation of a 100 runs is set up and ready to be run. Note the input voltage offset measurement and histogram command in the Calculator menu from the Results page.

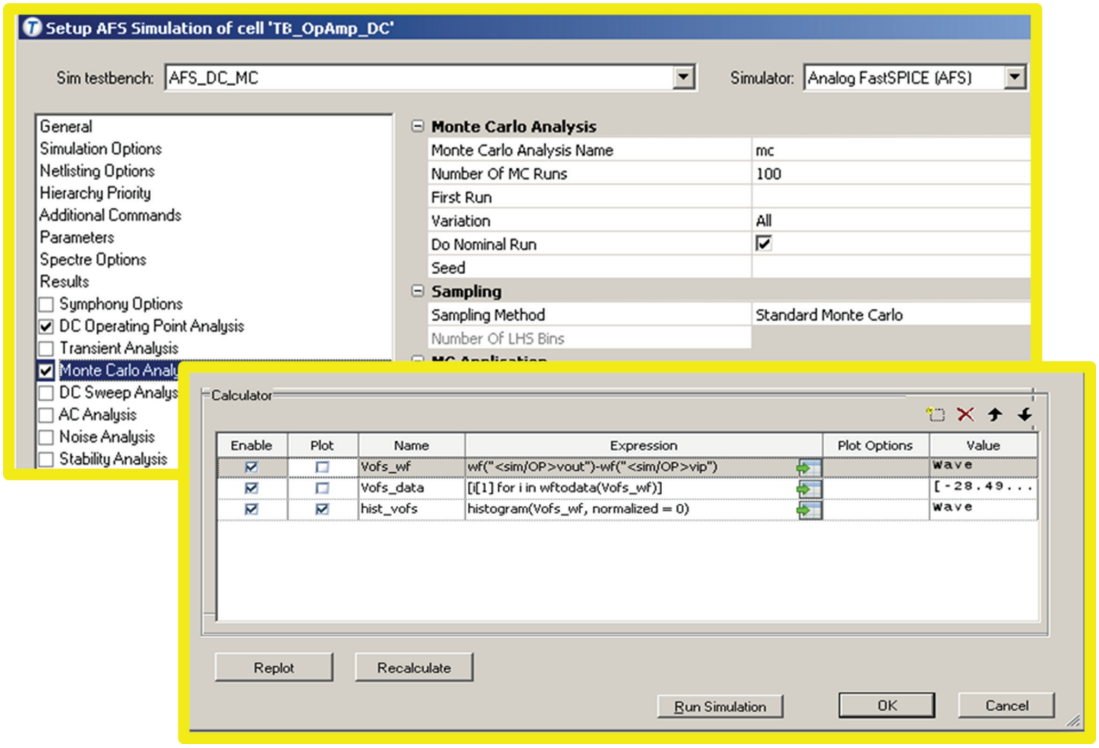

Figure 21: Monte Carlo simulation setup and calculator expressions.

In this simulation the random offset of the amplifier is being characterized. That is the input minus the output voltage, which in theory (for a very high gain op amp) should be zero. The random offset mainly comes from the amplifier's input devices (i.e., N3 and N4) in figure 2. On the schematic level (without any layout or real-world effects) for a fixed power budget, this is mostly determined by the input device's operating region (must be in saturation and ideally moderate or weak inversion) and size.

When the simulation finishes, EZwave appends the Monte Carlo results under the Currently Opened Databases menu and the histogram plot of the random offset voltage of the amplifier is displayed. A Gaussian approximation curve and all relevant statistical details and measurements are also shown in the graph. These details can be customized under the EZwave display preferences setup.

The offset voltage can also be plotted across the Monte Carlo runs by simply double-clicking on the measurement as shown in figure 23.

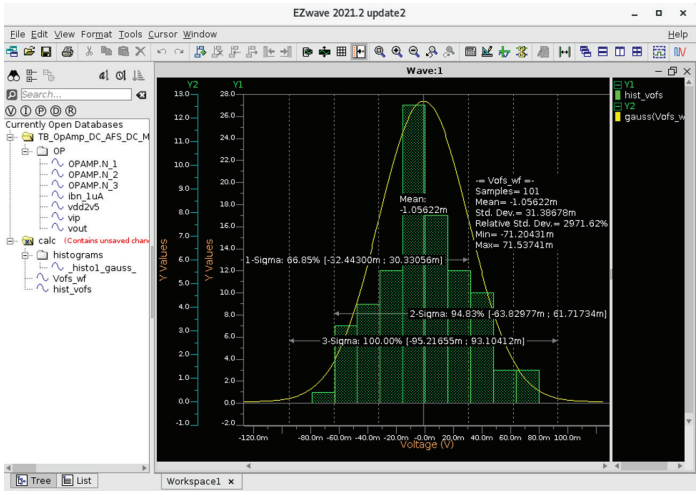

Figure 22: Histogram plot of the random offset voltage of the amplifier.

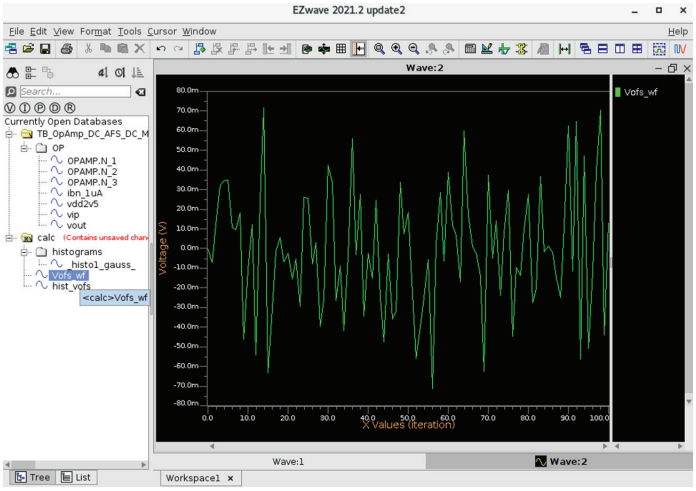

Figure 23: Offset voltage plot.

Stability analysis

Stability analysis is an important simulation for an amplifier. It shows how stable your design is across any perturbations. If the design is less stable, any signal perturbation affecting the amplifier produces ringing effects that can be seen in the transient response. The more stable a design is, the slower it gets; generally, therefore we need a nice balance. We use metrics to measure the stability performance of an amplifier, and these are the phase margin and gain margin. A good amplifier has 60˚ of phase margin and anything over 10dB of gain margin.

A test bench for a loop-stability analysis of the op amp where the loop is broken using a standard DC voltage source of zero volts is shown in figure 25. The source probe name determines where the loop is broken, and the rest of the stability page is the same as that of an AC analysis. A stability simulation test bench across a specific PVT corner set has been defined for the process, output capacitance, voltage, and temperature variables.

After running the PVT simulations, the stability results are appended at the bottom of EZwave as before. AFS automatically exports all required stability summary measurements under the measures section and the phase margin measurement is plotted across the corner run number.

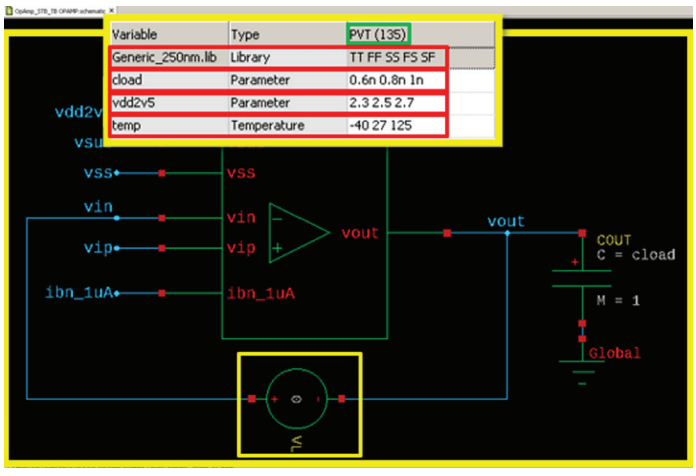

Figure 24: Stability analysis setup.

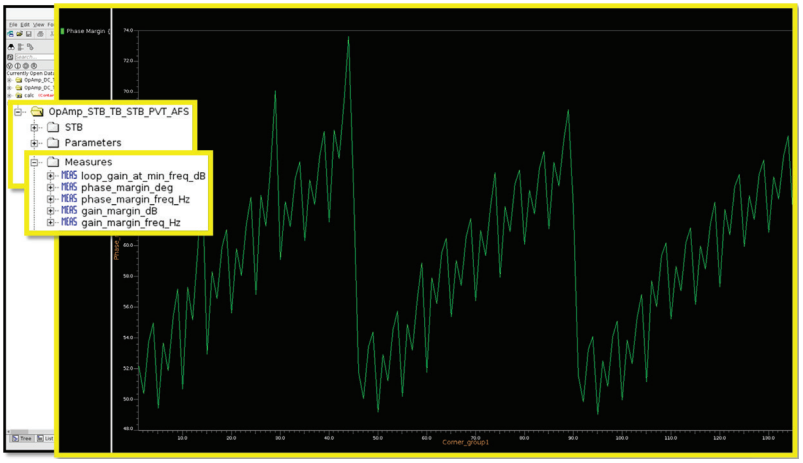

Figure 25: Phase margin measurement.

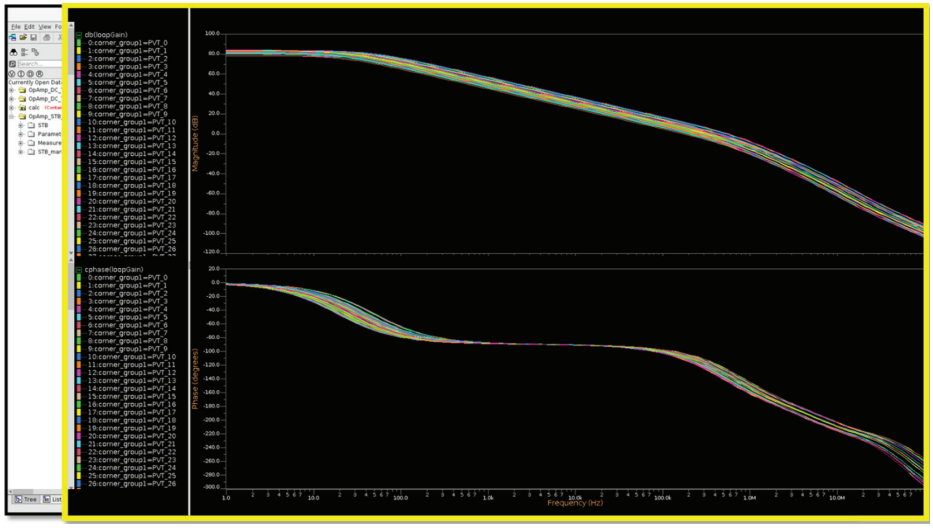

Figure 26: Stability analysis magnitude and phase waveforms.

Also, the classical loop-gain magnitude and phase waveforms can be accessed and plotted for all 135 PVT corners.

AC analysis

There is a more advanced simulation that tests the circuit's ability to reject power supply noise. An ideal amplifier only has gain from its input to its output; any other perturbation should be rejected. If the power supply varies, the output of the amplifier should remain intact. In practice, it never does. The way to measure the amplifier's performance in that regard is by using a metric called Power Supply Rejection Ratio (PSRR). PSSR is defined as the small-signal gain from the power supply in

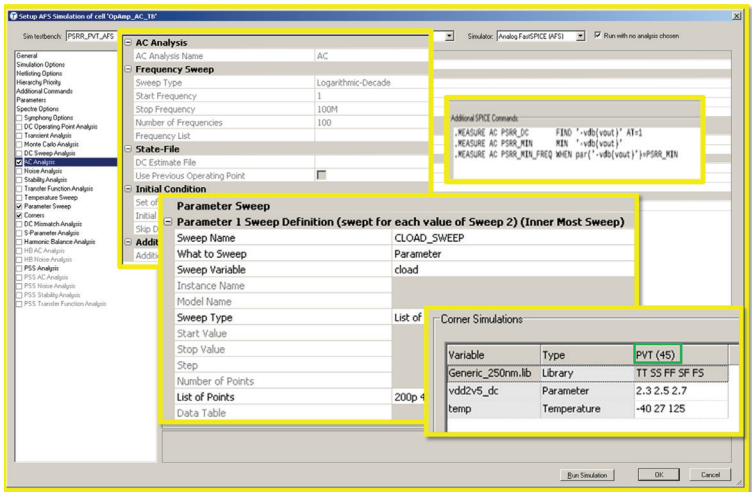

Figure 27: Setup Simulation for PSSR.

question to the output, divided by the loop gain of the amplifier (i.e., input to output). For an amplifier with high loop gain (Aβ>>10), this ratio turns out to be the same as the small-signal output voltage divided by the small-signal power supply perturbation voltage. Setting the latter to an AC signal of a magnitude of 1 simplifies the calculation of PSRR to be equal to the output voltage of the amplifier.

The AC analysis test bench in figure 28 has a small signal applied on the power supply VDD2V5 of the op amp in closed-loop mode. The output voltage across a frequency sweep provides the PSSR of the op amp for a frequency up to a decade or so below its gain bandwidth. A similar PVT corner is defined as the previous PVT corner set, with the exception that the output capacitance is swept under the Parameters Sweep analysis; therefore the corner setup consists of only 45 combinations.

The Setup Simulation menu supports an Additional Commands page for those users who need to enter additional Spice/Spectre commands or have test benches already setup with probe and measurement commands. For this example, three. MEASURE commands have been added under the additional commands page for this test bench.

PVT simulation

After running the Process Voltage Temperature (PVT) simulation, the AC results are displayed in EZwave. The output voltage can either be plotted directly from the results or cross probed from the schematic as follows. In S-Edit, a voltage or current can be cross probed to EZwave by simply clicking on the corresponding probe icon on the toolbar and selecting the desired node on the schematic. EZwave then plots the probed net, in this case, the output voltage magnitude and phase.

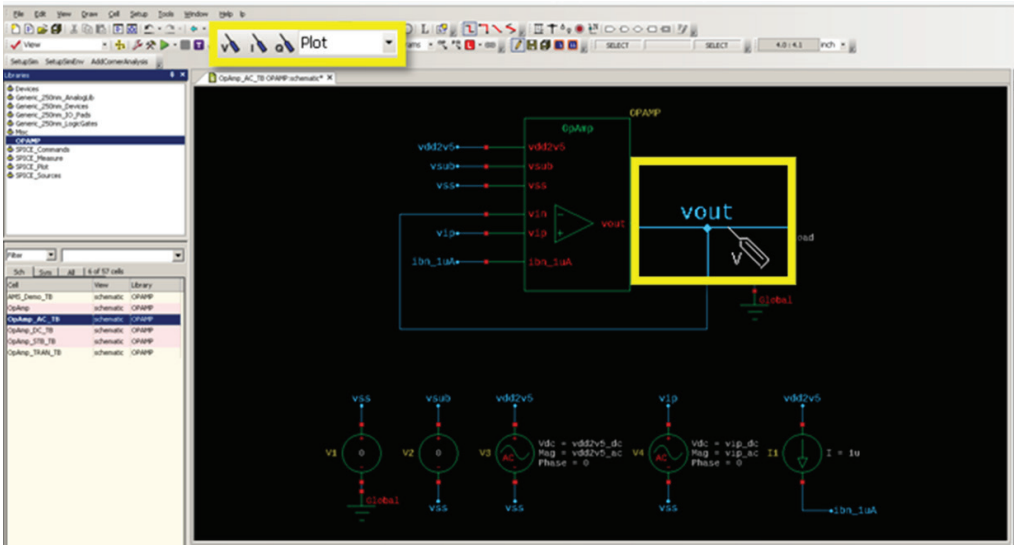

Figure 28: Probe nets to plot waveforms.

In addition, the minimum PSRR measurement across the AC sweep can be plotted against the parameter sweep C-load for all PVT conditions. This same measurement can be plotted against a different x-axis by simply right-clicking on it in the results browser and selecting, for example, corner_group1 as shown in figure 29.

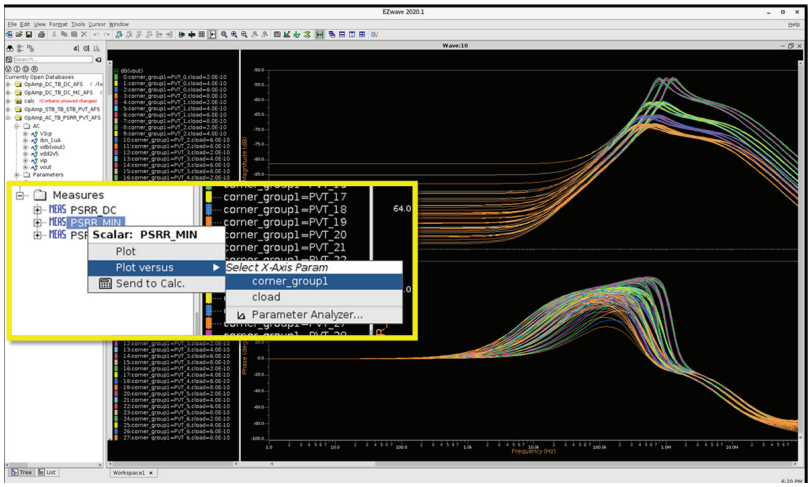

Figure 29: Power Supply Rejection Ratio waveform results.

Transient analysis

Finally, figure 30 shows a test bench for a transient analysis where an input voltage pulse is applied to the positive input of the op amp in the unity gain feedback mode. The Transient Analysis section of the simulation test bench shows the stop time, accuracy, and maximum time step to be used. A similar PVT corner set is used, including two different values of the output capacitance, resulting in a total of 90 corner simulations. Measurements are calculated during simulation to ultimately calculate the worst-case overshoot and undershoot values using the built-in calculator functions.

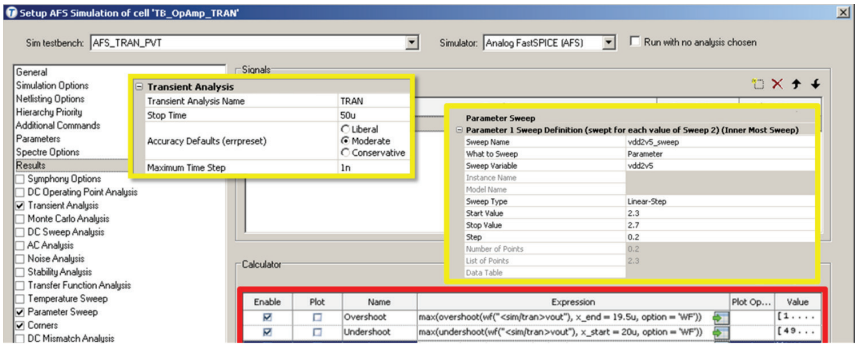

Figure 30: Simulation Setup for transient simulation.

The transient analysis results are displayed under Currently Open Databases in the EZwave results browser. The output voltage is plotted for all PVT combinations as shown in figure 31, and the overshoot and undershoot measurement results plotted as histograms in figure 32.

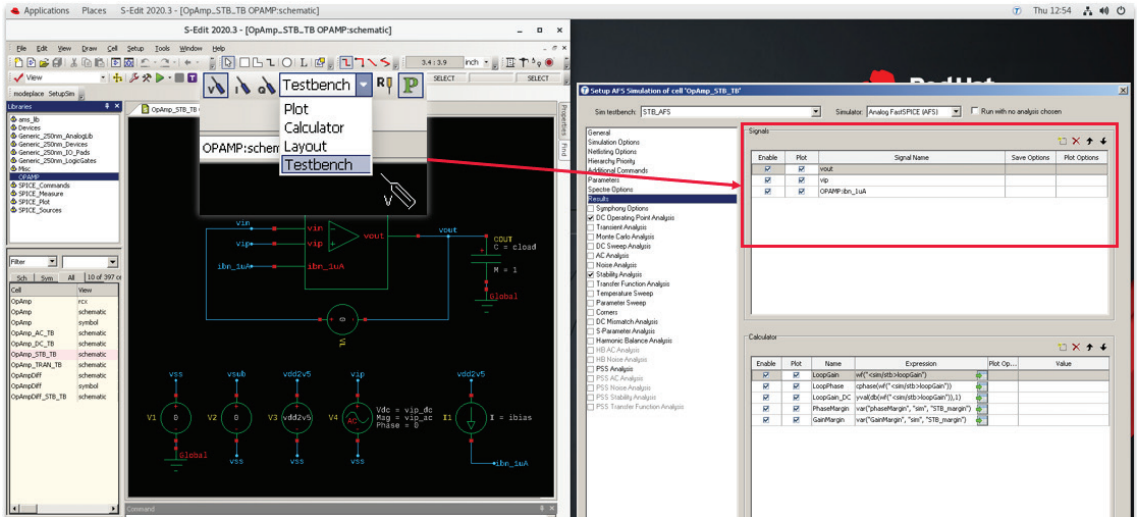

Figure 31: Output voltage is plotted for all PVT.

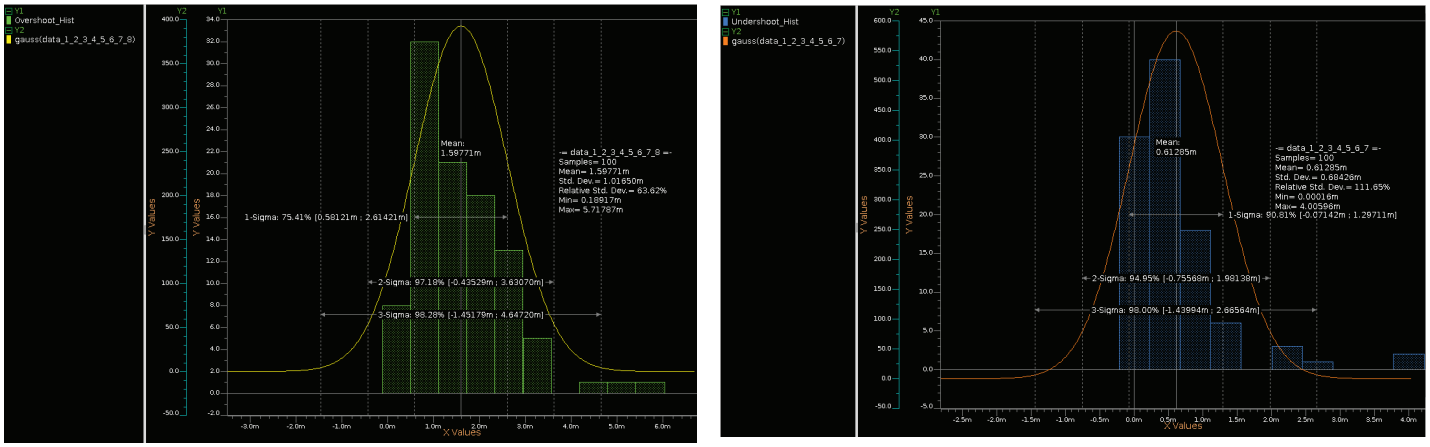

Figure 32: Overshoot and undershoot histograms.

Conclusion

Greater efficiency in analog design verification can now be achieved using our enhanced inter-tool communication in Siemens EDA's full-flow design environment. Integrating S-Edit, AFS, and EZwave helps engineers achieve an optimum IC design outcome. The tight integration with the EZwave calculator allows for easy construction of advanced expressions and pre-simulation or post-simulation measurement modifications that are all stored in states under a schematic test bench.

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