

Automotive IC Design Demands Next-Generation High-Sigma Verification

Old approaches to automotive IC design, like Monte Carlo analysis, require millions of simulations to achieve 5-sigma levels, but that's still not enough.

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High-sigma analysis is required for verifying replicated components, like memory blocks and standard cells, and for demonstrating mission-critical reliability for automotive and medical applications. It is not feasible to verify to high-sigma using brute-force Monte Carlo, as this requires 10s of millions of simulations to reach 5-sigma and billions in order to reach 6-sigma. Solido High-Sigma Monte Carlo (HSMC) was invented 10 years ago to solve this problem, and has been the benchmark for high-sigma analysis ever since. HSMC is in use today by thousands of memory, analog, and standard cell designers across most of the top 40 semiconductor companies. It's fast, accurate, scalable, and verifiable, and has been used to verify tens of thousands of designs across dozens of foundry processes.

High-Sigma Verifier is the next-generation high-sigma technology developed by the same Solido team (now part of Mentor, a Siemens Business) that invented HSMC. It uses the same tried, tested, and true core from HSMC, but has been enhanced with a series of algorithmic breakthroughs:

- **Adaptive intelligence:** High-Sigma Verifier has an all-new machine learning modeling technology that can tell when there is enough data to build a sufficiently accurate model. It knows how long model building will take and how long more simulations take. It makes smart decisions about when to build models and when to run more samples. It predicts when it will be able to achieve the desired level of accuracy and automatically stops when it has converged on accuracy targets. This minimizes the number of simulations and algorithmic overhead, which saves on wall-clock time and CPU usage.

- **Automated rare failure detection:** binary (i.e. pass/fail) outputs and multi-modal distributions are tricky at high-sigma, as the high-sigma algorithm must seek out failure regions proactively. HSMC does this well, but needs to be configured by the user to do it. High-Sigma Verifier automatically finds rare failure modes and adapts to handle them when they are present, with no input or configuration from the user. This makes it easier to deploy at scale and to use in fully automated flows and it avoids the risk of missing rare failure modes due to configuration error.
- **Solve yield mode:** High-Sigma Verifier has an all-new algorithm for correctly finding the yield of a high-sigma design in a single pass, every time. HSMC can do this, but it can take multiple iterations when the user's guess at the approximate sigma of the design is far off, which then requires subsequent manual iterations to bisect in. High-Sigma Verifier can solve any sigma design in a single run with no user input or intervention and it can tell if the user has a 2.6 sigma design or a 7-sigma design, with extremely high accuracy.
- **Fast high-sigma estimation mode:** High-Sigma Verifier includes a new algorithm that can produce high-sigma estimates to any sigma level with next to no algorithmic overhead. It can tell the user in just a few hundred simulations whether the design is close to the high-sigma mark or not and it shows the full estimated probability distribution function, so the user can see approximate performance at any sigma really quickly. Jobs can be continued with a single click to produce verification quality high-sigma answers using the full high-sigma algorithm.
- **Any sigma in constant runtime:** demand for verification beyond 6-sigma is increasing and it is now important to get out to around 7-sigma in production runtimes for very highly replicated structures like large memories and to identify over-margining. High-Sigma Verifier goes out to any sigma level in the same amount of time that it takes to solve a 6-sigma problem. It is about two orders of magnitude faster than HSMC at 7-sigma, and is pragmatic to use beyond 7-sigma.
- **Instant high-sigma feedback:** right from the very first samples, High-Sigma Verifier shows how the design is behaving at true high-sigma. This helps users to understand early in a run if there is a design problem, enabling faster iterations. HSMC could only start showing results about half way through the job.

High-Sigma Verifier introduces a suite of new algorithmic breakthroughs, making high-sigma analysis faster, more accurate, and easier to deploy and use than ever. Figure 1 shows solving write margin on a bit cell in just a few minutes – about 2X faster than HSMC, and with a single iteration.

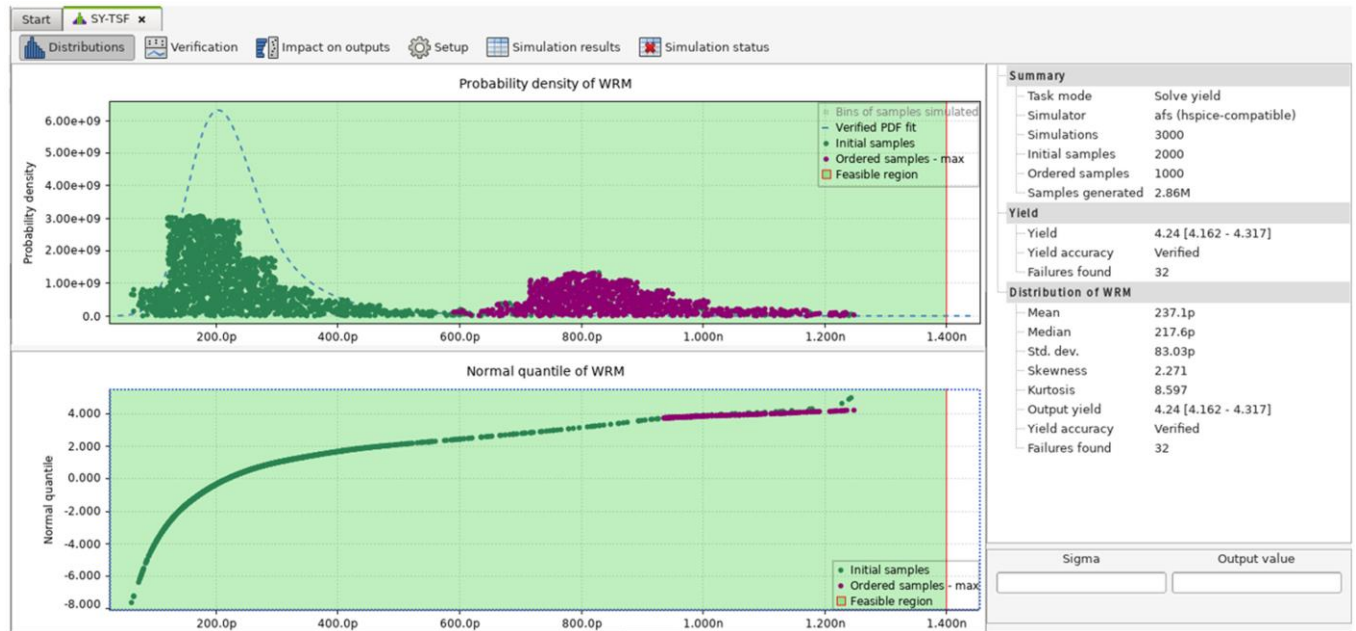


Figure 1: Example analysis result.

These advances make High-Sigma Verifier substantially faster than HSMC, while being just as accurate as a well-configured HSMC job. It is typically around 2X faster than HSMC for continuous distributions, and up to 10X faster for n-ary distributions. It is about 100X faster than HSMC at 7-sigma. And it always does the right thing in the first iteration with no user configuration or input, whereas HSMC may need, in some cases, 2 or 3 iterations driven by the user to arrive at the right answer.

As Figure 2 shows, at 4.2 sigma, High-Sigma Verifier's estimation mode (HSV-E) is significantly faster and uses only 12.5% of the simulations compared with HSMC. High-Sigma Verifier's verification mode (HSV-V) saves 25% of the simulations, cuts wall-clock nearly in half, and provides identical accuracy. On the 7-sigma case, High-Sigma Verifier is orders of magnitude faster than HSMC.

	Bitcell (4.2 sigma)		Bitcell (7 sigma)	
	# sims	runtime (s)	# sims	runtime (s)
HSMC	4000	396	4000	23400
HSV-E	500	24.7	500	41.92
HSV-V	3000	231.7	3000	233.5

Figure 2: Comparing HSMC to High-Sigma Verifier modes.

The new adaptive algorithmic advances also make High-Sigma Verifier ideal for large scale deployments. It is very easy to use and does the right thing automatically, which makes it readily deployable to large numbers of engineers with very little training or support. It is also excellent for automated verification of large batches of standard cells, memory IP, and timing arc verification, as it requires no scripting or user intervention to handle corner cases. High-Sigma Verifier is included with Mentor's [Solido Variation Designer](#).



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