DIGITAL INDUSTRIES SOFTWARE

A systematic analog verification approach using Analog FastSPICE Harmonic Balance

Analog mixed-signal

Executive summary
In this white paper, we focus on the application of Analog FastSPICE (AFS) Harmonic Balance (HB) engine that provides improved convergence, enhanced runtime and memory reduction via three case studies of circuits commonly simulated using HB. We will provide a summary of performance and memory advantages of AFS HB. We conclude the paper with a summary of the latest advancements for post-layout designs with Siemens EDA's AFS eXTreme (AFS XT) and a summary of the latest suite of AFS HB analyses.

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Introduction

The demand for more data access and enhanced connectivity continues to drive technology towards higher data rates, advanced process nodes, lower power, and increased functionality. Designers are under tight deadlines to design and validate a competitive product to meet stringent specifications that cover performance, power, noise, linearity, and reliability. To address today's radio frequency (RF) design challenges of high accuracy, high capacity and low power,

a silicon-accurate high-performance and world-class RF engine is required. Both single-tone and multi-tone harmonic balance analyses are essential in addressing these challenges for linear and moderately nonlinear periodic circuits (LNA, PA, Mixer, Rx, Tx, etc.), along with some of the most common building blocks, including VCOs (LC-tank, ring) and oscillators (xtal, RTC).

Case Study #1: 5G MIMO Tx IP3 in 16nm process

Our first case study examines the transmitter (Tx) in a 5G MIMO application in an advanced process node (16nm) using FinFET devices. Refer to a simplified block diagram in figure 1 illustrated below. The circuit includes an input baseband with I and Q signals into a filter which then feeds into the mixer with an additional input of the local oscillator (LO) followed by a pre-power amplifier (Pre-PA).
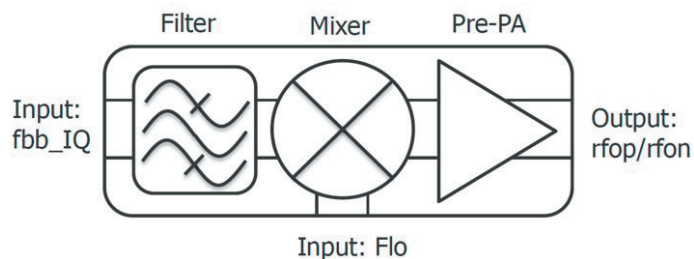

Figure 1: Transmitter (Tx) block diagram.

The target metrics for this design are the output power and the IP3, both widespread measurements for wireless transmitters as illustrated by figures 2 and 3.
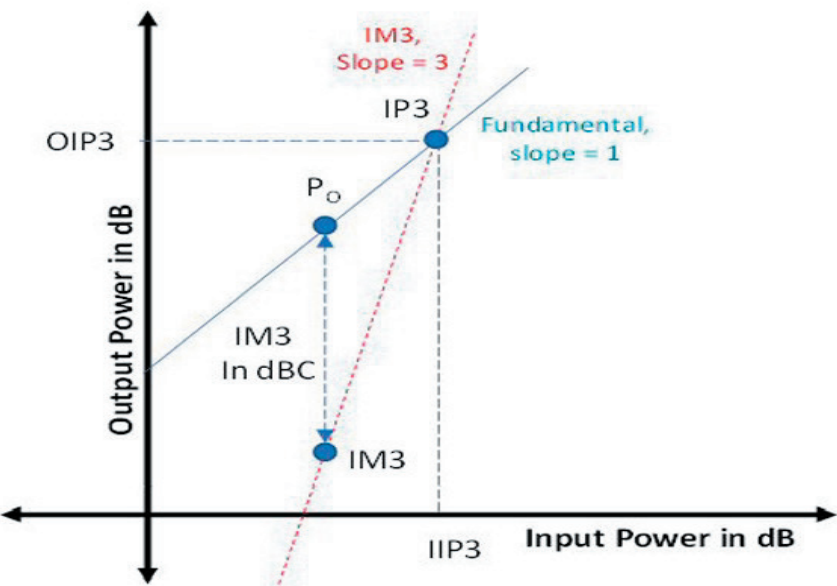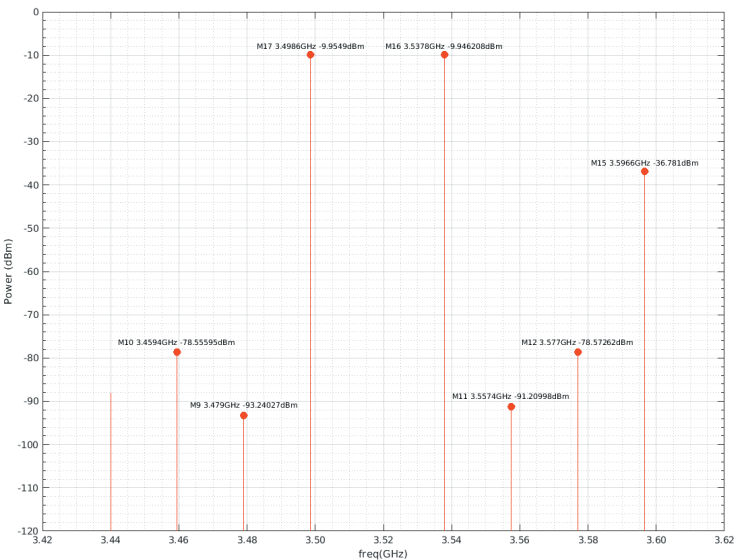

Figure 2: Transmitter IP3 example.

Figure 3: Transmitter power output plots.

These common measurements can be reasonably straightforward to simulate for designs in mature technology nodes. However, as designs move to advanced nodes with increasing process complexity and parasitics, these simulations can become challenging to obtain convergence, much less complete in a reasonable time for meeting high accuracy requirements.

Simulating with HB for these types of measurements becomes more challenging as we increase the design size (e.g., resistors, capacitors, transistors, inductors, etc.), increase the number of tones (e.g., 1 to 2 to 3), increase the number of harmonics per tone (e.g., 10 5 5 to 50 10 10), and include more complex models (e.g., BSIM4 vs FinFET). Post-layout extracted simulations are even more challenging than pre-layout schematic simulations requiring more harmonics for convergence.

Before discussing the simulation results, we first need to highlight how easy AFS is to adopt into the design flow. AFS supports the industry-standard netlist syntax and is seamlessly integrated into design environments. Therefore, no modifications to netlists are required for simulating a design previously simulated with a competitive simulator in an industry-standard environment to now being able to simulate with AFS. All outputs and plotting are fully supported requiring no additional work from the designer.

Since we are interested in the IP3 for the Tx, we must set up a multi-tone analyses in HB and include the three frequencies of interest. In our example, this includes an LO at 3.5966 GHz, baseband #1 at 58.8MHz, and baseband #2 at 98MHz. This design also included multiple S-parameter files to model various attributes of the circuit, which can often be very challenging to simulate although ideal for frequency-domain analyses such as HB. Often, poor convergence is caused by poor S-parameter characterization such as excluding DC, limited density of frequency points throughout the frequency range, or insufficient frequency range to capture effects of the number of harmonics required for the simulation. For this design, the S-parameters were of good quality.

Let us start with the pre-layout version of our Tx with approximately 38,000 elements. The TX requires a moderate number of harmonics per tone [35 5 5] wherein it completes in a few hours with about 56 GB of RAM but is 1.3x faster another RF simulator. As we move to the post-layout design, the parasitics increase the size to approximately 53,000 elements and require a significant increase in the harmonics per tone [100 35 35]. The runtime increased from a few hours and 195 GB of RAM in our pre-layout design to 1.5 days requiring 356 GB of RAM for the post-layout version. However, the other RF simulator could not converge after six days on the post-layout design and the simulation was killed by the designer, resulting in no useful information on the post-layout design from the other RF simulator's simulation.

After achieving acceptable results, the designer requested further reduction in runtime and was willing to accept some accuracy reduction. After further review of the testbench and setup, it was determined that reducing the harmonics and trimming some of the unused inter-modulation products was a viable path for improving performance. The conclusion was to reduce the harmonics to 70 (from 100) for the LO and reduce the harmonics for the baseband tones to 3 (from 5). An additional option (maximorder=10) was used to limit the inter-modulation products, resulting in only a 0.2dB loss in accuracy. The new settings reduced the runtime by 1.7x to 21 hours and reduced the memory by 9x to 40 GB.

The testbench setup and a summary of the performance and memory used are presented below in tables 1 and 2.

Table 1: Testbench setup summary.

	Pre-Layout	Post-Layout	Fast Post-layout
Process	16nm	16nm	16nm
Elements	38,000	53,000	53,000
Analysis	3-tone HB	3-tone HB	3-tone HB
Fund Frequencies	3.5966 GHz 58.8 MHz 98 MHz	3.5966 GHz 58.8 MHz 98 MHz	3.5966 GHz 58.8 MHz 98 MHz
Harmonics	35 5 5	100 5 5	70 3 3

Table 2: Performance and memory summary.

	AFS		Other RF Simulator		AFS Advantage	
Configuration	Runtime	Memory	Runtime	Memory	Runtime	Memory
Pre-layout	1.5 hrs	195 GB	2 hrs	173 GB	1.3x	1.1x
Post-layout	1.5 days	356 GB	DNC*	DNC*	∞	∞
Fast post-layout	21 hrs	40 GB	DNC*	DNC*	∞	∞
* DNC: Other RF Simulator did not converge after 6 days for the post-layout design						

In summary, AFS HB improved performance by 1.3x on the pre-layout testbench and was able to converge in 1.5 days on the post-layout design whereas the other RF Simulator fails to converge. This data was collected using AFS HB before the recent enhancements to AFS XT. Additional improvements in both performance and memory reduction are expected for the post-layout design without loss of accuracy as can be seen in the "Additional Examples of AFS Performance" section.

Case Study #2: 5G MIMO Rx conversion gain in 16nm process

Our second case study is the post-layout receiver (Rx) in a 5G MIMO application in the same advanced process node (16nm) as our previous case study. The receiver consists of an LNA, mixer, and buffer as shown in figure 4 below.
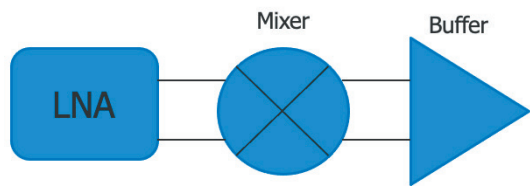

Figure 4: Receiver front-end block diagram.

This is a single-tone HB simulation at a fundamental frequency of 5.9 GHz followed by a small-signal analysis (HBAC) to capture the conversion gain from 1kHz to 1GHz. In contrast to our previous design where complexity is dominated by the number of tones and harmonics, this design has fewer tones (only one) and requires only five harmonics. The complexity in this design comes from the large

post-layout netlist containing more than 2.2 million elements and ~300,000 FinFET transistors. Convergence for these large designs is an area AFS has excelled at in all forms of analysis (DC, Transient, PSS, HB) and is no exception here. The biggest challenge for this type of design is to first achieve convergence; the subsequent challenge is to get performance of that convergence. With the same simulator options and settings as the other RF simulator, AFS was able to complete the steady-state solution (HB) 8x faster. The conversion gain matched the other RF simulator within 0.2dB across the frequency range of 1 kHz to 1 GHz. This allowed the designer to perform two to three iterations of the design in one day where the other RF simulator was only able to facilitate one design iteration per day (26 hours).

Table 3: Analysis summary for 5G MIMO receiver.

Runtime/Memory of AFS versus Other RF Simulator						
	Analysis	Process	Elements	Harmonics	Runtime	Memory
Post-layout	1-tone HB	16nm	2.2 M	5	8x	0.8x
Post-layout	HB + HBAC	16nm	2.2 M	5	3x	1.2x

In summary, AFS HB was 8x faster than the other simulator on the post-layout testbench and allowed the designer to iterate two to three times more productively. This data was using AFS HB without the recent enhancements to AFS XT, which we would expect additional improvements without loss of accuracy.

Case Study #3: High-speed SerDes VCO (25 GHz to 36 GHz)

Our final case study focuses on one of the most ubiquitous and critical blocks in many electronic systems, the voltage controlled oscillator (VCO). The two most common architectures include a ring VCO and an LC-tank VCO. The ring VCO often has lower power, area, and broader frequency range. In contrast, the strength of the LC VCO is its superior noise performance. Figure 5 shows simplified block diagrams of each architecture.
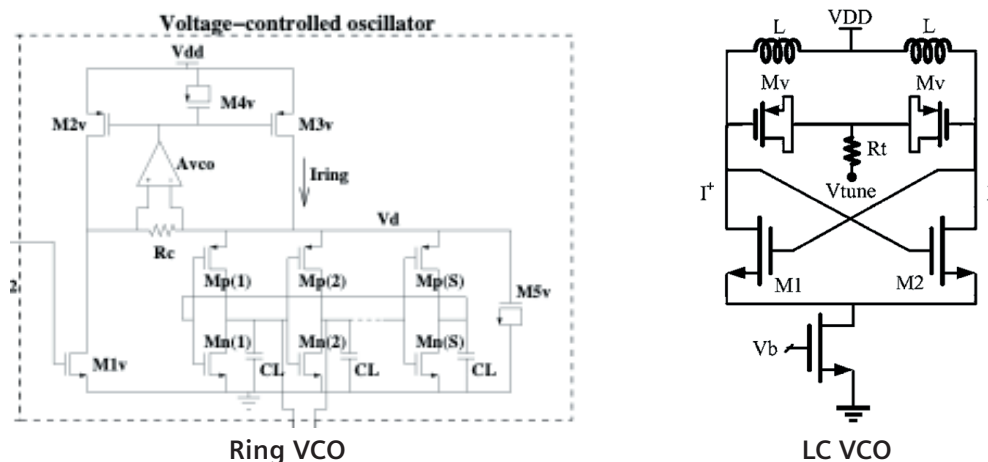
Ring VCO

LC VCO

Figure 5: Ring and LC VCO architectures.

Many of the challenges we cover will apply to both VCO architectures, especially as we move to more advanced process nodes with increasing parasitics and lower supply voltages. However, our focus will be on the specific challenges associated with high-frequency LC VCOs used in high-speed SerDes for wireline applications that demand low phase noise and integrated RMS jitter.

HB is an ideal analysis to apply for this architecture as the LC VCO is moderately non-linear and often uses frequency-dependent models (S-parameters) for the inductor and associated routing parasitics. As with any simulation, the quality of results is highly dependent on the quality of models used in the simulation. The foundry will certify models (resistors, capacitors, inductors, transistors) with an EDA vendor's simulator for specific versions of the simulator. However, designers must also account for non-ideal affects not included in the baseline models because of the high-frequency operation. A 3D EM solver is required to accurately capture the routing parasitics for high frequency applications. The core inductor model varies from simple 2-port S-parameter to much more complex models requiring hundreds of ports.

Exhaustive verification is required to ensure all specifications across process, voltage, and temperature (PVT) are achieved. This extends to extracting RCC for various scenarios, including typical to worst-case scenarios involving temperature dependence. Some of the common verification tasks include measuring power supply rejection ratio (PSRR) for both deterministic and random noise, duty cycle, gain (kVCO), frequency range tuning, amplitude, slew, phase noise, and various types of jitter. As noise is one of the limiting metrics for VCOs, we will focus our case study on VCO phase noise.

We considered three process generations (16nm, 7nm, 5nm) of an LC VCO used in high-speed SerDes PLL where the frequency range spanned from 25 GHz to 36 GHz. Our metric of interest is phase noise measured at offsets of 100 kHz, 1 MHz, 10 MHz, and 100 MHz, which requires successful convergence of HB large signal analysis followed by HBNoise small signal analysis.

The challenge for the first generation (16nm) was getting results in a reasonable time as the design migrated from a planar process where it contained ~100,000 elements with a runtime of less than one hour to a FinFET process where the element count increased by 10x to 1 million elements and the runtime increased by 6x due to the additional parasitic resistances and capacitances. However, AFS still provided a runtime of 3.4x faster than the other RF simulator with 20 percent lower memory consumption. Pre-layout simulations in 16nm, although they were much faster, were no longer sufficient to obtain accurate enough results and RCC extractions were required much earlier in the design cycle. This drastically impacted development costs due to longer simulation times, more simulation licenses, and additional hardware to meet tapeout deadlines.

The second-generation (7nm) migration was even more challenging as the resistance increased by 3x compared to 16nm. The simulation time increased by ~2.7x and the element count increased to 2.4 million. AFS still provided a 2x performance advantage over the other RF simulator for this design. In the 7nm process, more accurate modeling of the inductance and routing parasitics in the LC VCO was required. Hence, an accurate EM solver was used to extract the inductance and routing capacitance creating multiple S-parameters, one with over 100 ports. Adding complex S-parameters with hundreds of ports added another challenge as the initial models did not include a sufficient frequency density to accurately model the required frequency range, along with excluding DC. Adding the more complex S-parameter model resulted in longer simulation times for the EM solver and many iterations with the designer. All the results above were obtained from AFS. The next generation of AFS (AFS XT) was recently run and found to be 8x faster with a 7x reduction in memory versus AFS for the 7nm design while maintaining accuracy.

The final migration was to the 5nm process where the first iteration of the design (~2.5 million elements) took 1.2 days to complete. AFS was 2x faster than the RF simulator. The final version before tapeout grew to over 6 million elements and the references AFS simulation took two days, whereas the other RF simulator's simulation took five days. Running with the next generation of AFS XT, the simulation time was reduced to 10 hours with comparable accuracy (within < 0.5 dB), allowing the designer to make more iterations on the design and cover many more corners.

Table 4: VCO performance summary across advanced technologies.

Generation	Elements	AFS Runtime	AFS versus Other RF Simulator	AFS XT versus Other RF Simulator
16nm	1 M	6 hrs	3.4x	N/A
7nm	2.5 M	16 hrs	2x	8x
5nm	6 M	2 days	2.5x	12x

In summary, moving from planar to FinFET nodes increased simulation time drastically, and further advancement from 16nm to 5nm increased the parasitics (especially resistance) and hence the element count by 6x and runtime by 8x. AFS performance for all three generations was faster than the other RF simulator, ranging from 2x to 3.4x and AFS XT extended the performance lead by 8x to 12x. In addition, the other RF simulator was either much slower or failed to converge. Accurate modeling of the routing parasitics was also found to be critical for these types of designs.

Additional examples of AFS performance

In figure 6 below we share some additional performance and memory comparisons of AFS (not AFS XT) versus the other RF simulator. From the graph, we can see that AFS outperforms and in many cases utilizes less memory. We can also see that as the design becomes more complex (requiring more harmonics), AFS excels.
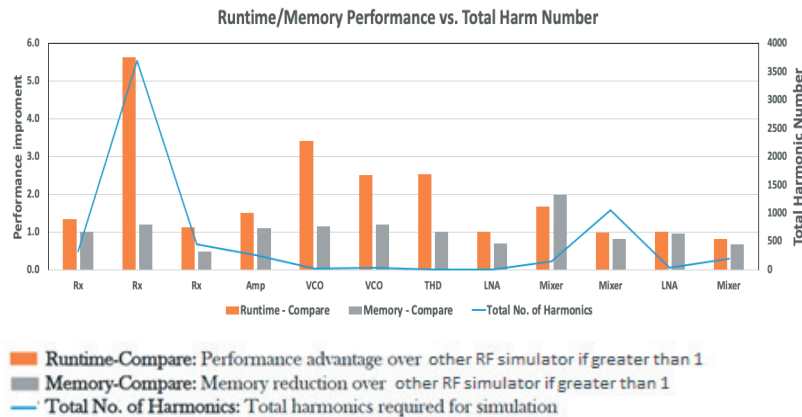

Figure 6: Performance versus harmonics comparisons of AFS and Other RF Simulator.

Performance is a critical aspect of RF verification but the ability to handle large designs is crucial, especially as we move to more advanced nodes. The graph below highlights the exceptional capacity handling capability that AFS and AFS XT provides.

Capacity refers to the number of elements contained in the netlist including active and passive devices, parasitic elements, etc.
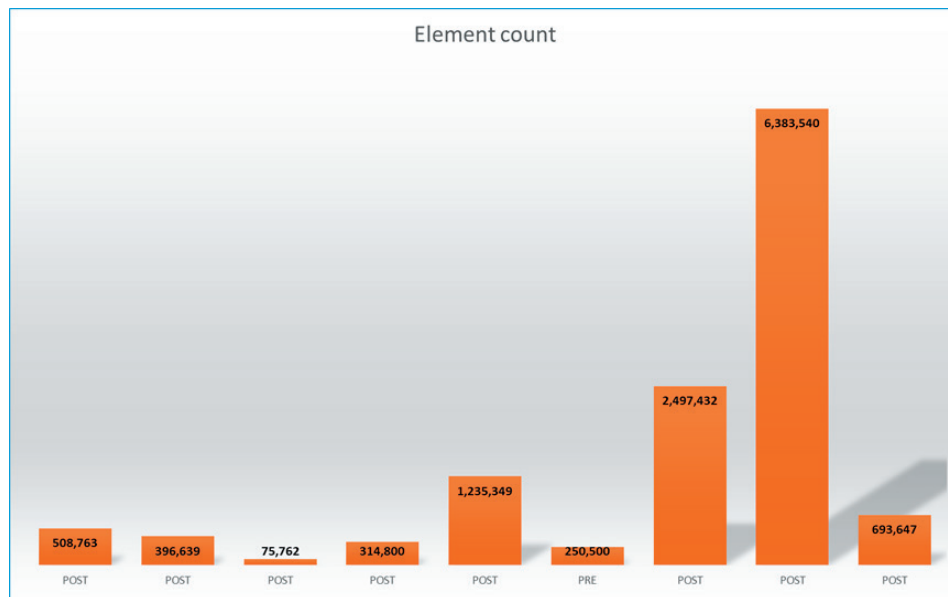
Total elements

Figure 7: AFS RF HB capacity examples.

Analog FastSPICE eXTreme technology

In October 2020, a major upgrade was done to the AFS technology via the introduction of AFS eXTreme (AFS XT) at no additional cost to new and existing customers. AFS XT is a revolutionary technology that boosts simulation performance for nanometer-scale verification of large, post-layout analog designs through a new adaptive matrix solver and new RC reduction algorithms. With AFS XT, designers can increase simulation performance while meeting user-defined accuracy. AFS XT can handle large netlists with over 300 million elements

for transient and DC analysis. AFS XT is utilized by a wide customer base and further empowers the AFS RF engine to perform Shooting Newton and Harmonic Balance analyses with boosted performance without choking on convergence or loss of accuracy.

Figure 8 below shows plots comparing the runtime improvements of AFS versus AFS XT and AFS XT versus the other RF simulator.
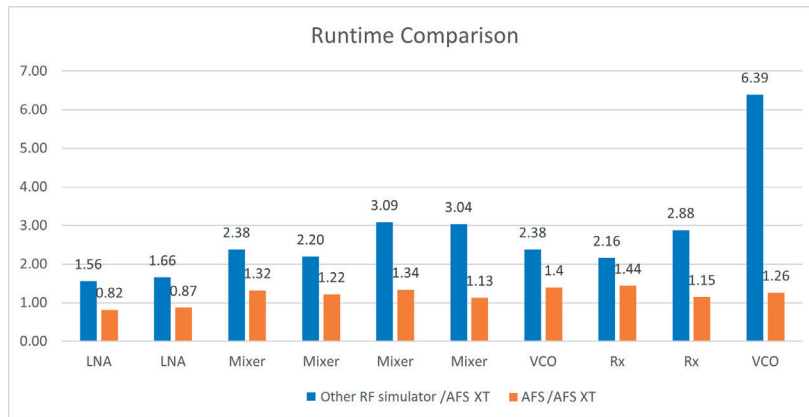
Figure 8: Runtime comparisons of AFS, AFS XT and the other RF simulator (value greater than 1.0 signifies speed up with AFS XT).

Figure 9 below shows plots comparing the memory improvements of AFS versus AFS XT and also AFS XT versus the other RF simulator.
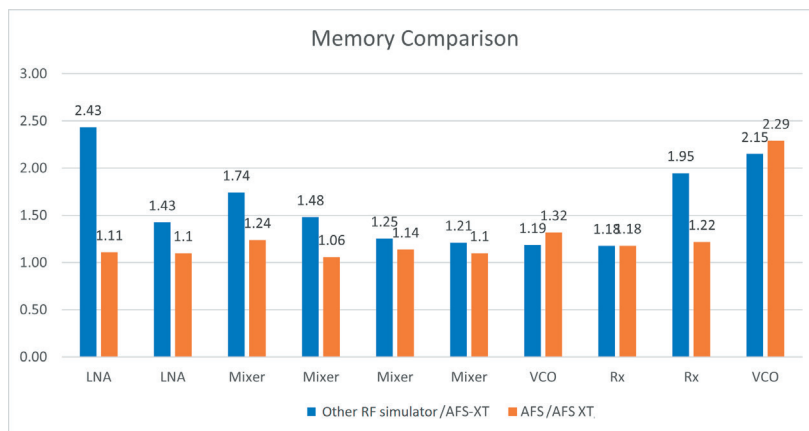

Figure 9: Memory comparisons of AFS, AFS XT and the other RF simulator (value greater than 1.0 signifies memory reduction with AFS XT).

Analog FastSPICE RF Harmonic Balance offerings

The AFS Harmonic Balance suite comprises of large signal HB analysis and small signal noise (HBNOISE), AC (HBAC), stability (HBSTB), scattering parameter (HBSP) and transfer function (HBXF) analyses. While single tone is supported for driven circuits and autonomous circuits, multi-tone (2-4) is supported for driven circuits.

For superior accuracy and performance on linear and moderately nonlinear circuits, the AFS HB solvers are further optimized for performance and convergence via automated intelligence algorithms, with no compromise in accuracy. Nanometer RF circuit design requires extensive sweeps, corners, and Monte Carlo analysis. AFS HB utilizes multi-threaded capability for an additional performance speedup versus single core operations. Integrated with Solido™ Variation Designer software, the AFS platform addresses comprehensive corner variation results efficiently. It allows a more effective verification that provides accuracy with a lesser number of simulations across all environmental corners, reducing the RF simulation complexity.

Table 4: AFS Harmonic Balance offerings.

Large Signal	Small Signal	Applicability
HB (Single Tone HB)		Large Signal DC operating point Driven and Autonomous Circuits
HB (STHB)	HBAC	Small Signal AC Driven and Autonomous Circuits
	HBXF	Small Signal Transfer Function Driven and Autonomous Circuits
	HBNoise	Small Signal Noise – Sampled and Modulated Driven and Autonomous Circuits
	HBSTB	Small Signal Stability Driven and Autonomous Circuits
	HBSP	Small Signal S-Parameter Driven Circuits
HB (Multi Tone HB)		Large Signal DC operating point Driven Circuits
HB (MTHB)	HBAC	Small Signal AC Driven Circuits
	HBXF	Small Signal Transfer Function Driven Circuits
	HBNoise	Small Signal Noise Driven Circuits - Modulated
	HBSTB	Small Signal Stability Driven Circuits
	HBSP	Small Signal S-Parameter Driven Circuits

The Harmonic Balance method computes the periodic steady state of the circuit utilizing the frequency-domain, similar to the Shooting Newton method, which utilizes the time-domain. After a periodic steady-state solution is found, small signal analyses such as HB noise can also be run.

▎Conclusion

As showcased by our case studies, whether a transmitter, receiver or a VCO, the AFS Harmonic Balance engine provides boosted performance with superior convergence without compromising on accuracy in advanced process nodes.

Siemens EDA's Analog FastSPICE (AFS) platform offers a Harmonic Balance engine for both single-tone and multi-tone analysis and the HB analysis suite is comprised of large signal and a variety of small signal analyses that are optimized for performance and convergence with no compromise on accuracy.

Furthermore, the Analog FastSPICE platform is foundry-certified accurate by the world's leading foundries, delivering nanometer SPICE accuracy. It provides the world's fastest circuit verification for nanometer analog, radio frequency (RF), mixed-signal, memory, and custom digital circuits. It boasts an additional performance boost up to 10x possible with the recently released AFS eXTreme technology for nanometer-scale verification of large, post-layout designs as compared to the previous generation. The AFS XT platform delivers the fastest mixed-signal simulation with Symphony™.

Come talk to us regarding your RF verification issues and try out our AFS Harmonic Balance engine to get through the hurdles of convergence with multi-tone analyses, while benefiting from industry proven performance!

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