Using machine learning (ML) methods in production-ready engineering solutions for IC verification

Utilizing ML to produce consistent, verifiable, and correct answers for SPICE-level IC verification

Executive summary

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Introduction

Semiconductor designs continue to push the envelope of performance, functionality, and efficiency while their application scope expands in high-performance computing, automotive solutions, and IoT devices. The increased design complexity, scale, and mission-critical operations of semiconductor designs mean that IC verification strategies must evolve to cover exponentially more scenarios.

At the SPICE level, this leads to a significant increase in design and IP verification requirements. In modern SoC design flows, factors like high instantiation count of IP components, variability from manufacturing effects, and extremely low target failure rates all drive the need for verification methodologies targeting 3, 4, 5, or 6-sigma and higher. Combined with the need to verify design performance and functionality over an extensive range of voltage and temperature corners, this results in millions to billions of simulations required to fully verify a design. Because of this, traditional brute force Monte Carlo methods are no longer able to scale to meet verification requirements.

Machine learning (ML) methods provide a way to overcome the limitations of traditional SPICE methods. ML solutions deliver results with orders-of-magnitude faster runtime compared to traditional methods, and many design and verification teams have started to apply ML techniques to introduce new advantages over previous generation methodologies. As a result, we are starting to see breakthrough speedups and coverage increases in this space.

However, with millions or billions of dollars in research, development, and production costs per semiconductor design, ML methods must not only be fast, but also be consistently and verifiably correct.

Verifiability, accuracy, generality, robustness, and usability

To be a production-ready engineering solution, ML methods must have proven capability in the following aspects: verifiability, accuracy, generality, robustness, and usability.

• Verifiability: The solution must have a method of self-verifying or enabling users to verify correctness of answers provided.

• Accuracy: ML results must meet engineering accuracy tolerances in the regions of interest.

• Generality: ML methods should work on a wide range of data, and not just for a niche dataset. To be a production-ready engineering solution, ML methods must have proven capability in the following aspects: verifiability, accuracy, generality, robustness, and usability.

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ML tool capability levels

Given the criteria for ML methods mentioned above, ML capabilities for IC verification can be categorized into five levels, progressing from having no ML capability to full production readiness.

Level 0: No ML. These are simply brute-force tools that are not ML accelerated. For SPICE simulation, this means using a brute-force Monte Carlo approach to verify designs.

Level 1: Partially reliable ML. These ML methods work on some cases, but fail on others, with no way to tell. Tools at this level are seldom useful for practical IC design or verification applications since they do not provide reliable indicators of correctness of its results. They are used mostly for demonstration purposes.

Level 2: Partially reliable ML with accuracy-aware self-verification. ML tools at this level have methods to determine when results are correct or incorrect. They are usable for certain tasks, but users need a backup plan for when the tools are unable to produce correct results.

Level 3: Adaptive, accuracy-aware ML. Tools at this level can identify when ML models are not delivering sufficiently accurate results and can continue adaptively collecting data and improving models automatically until accuracy criteria are met. Tools in this category are useful in production, as long as there is good support for occasional corner cases that cannot be automatically solved yet.

Level 4: Full production ML that "just works". Solutions at this level have extended level 3 adaptive tech by identifying and supporting all of the corner cases and deliver correct results in every case, every time.

As with most software applications, each tool capability level requires approximately an order of magnitude more development effort than the previous level. While level 1 prototypes can be developed in weeks, getting to level 4 requires years of focused R&D development for a large team and production hardening.

Solido machine learning: Toward level 4 ML capability

Solido™ software from Siemens EDA has developed ML tools that are near level 4 ML capability. In Solido tools, the first step is to perform an initial design of experiments (DoE). This is a sparse set of measurements that cover the entirety of the results space.

Building on the results of the DoE, the tool can construct a first-order ML model of the expected results space. Target areas of interest are identified where more model accuracy may be required.

The tool then produces more results and compares them against ML-generated results. If the results do not match within engineering tolerances, the tool optimizes further with additional data and updated models.

This process allows Solido tools to obtain a broad view of the results, with added granularity for fine-tuned results at areas of interest as well as built-in verification.
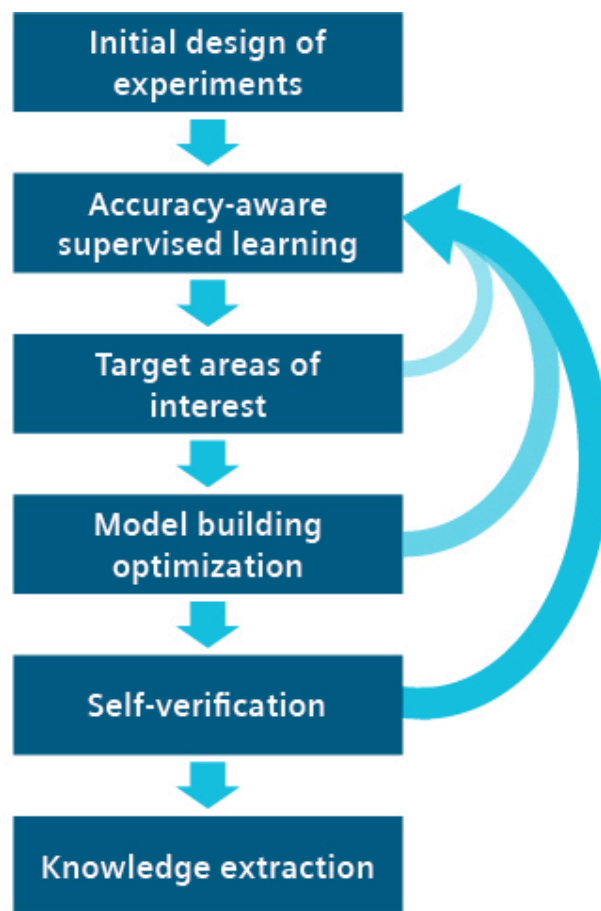
Figure 1. Level 3 ML capability with Solido machine learning.

An example of this technology in a productized solution is Solido High-Sigma Verifier, part of Solido Variation Designer. This tool achieves full bruteforce accurate verification results at any target sigma in orders-of-magnitude less SPICE simulation runtime compared to traditional methods. High-Sigma Verifier enables users to achieve higher verification accuracy and coverage while significantly reducing verification schedule times.
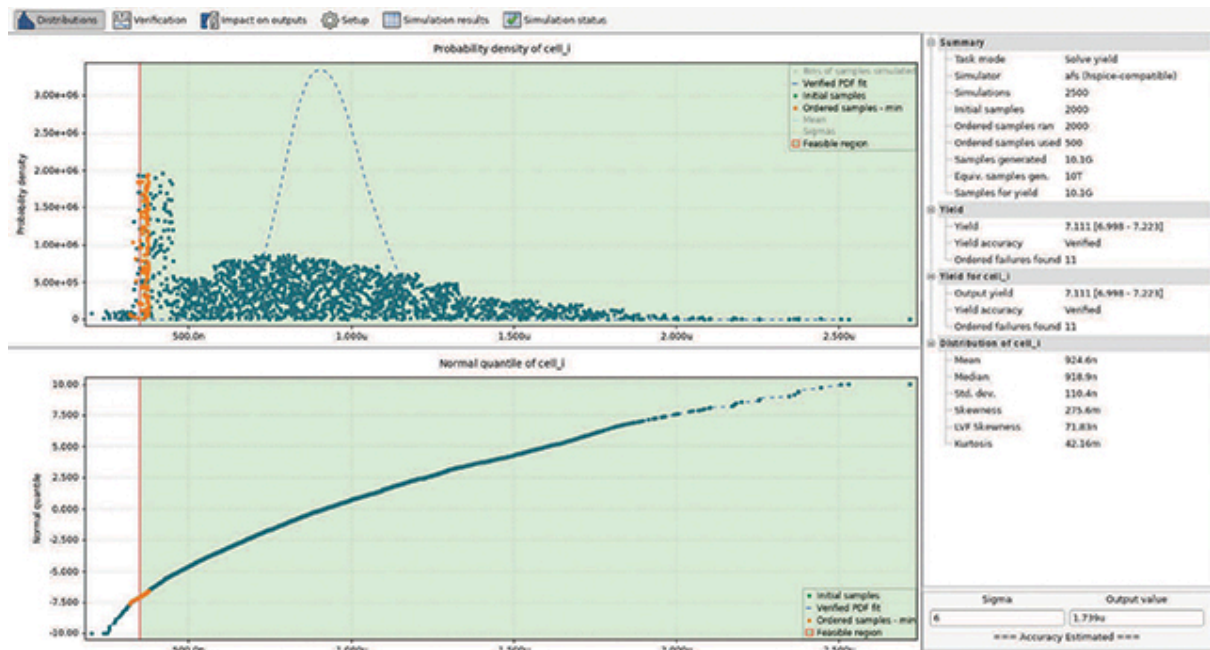
Figure 2. Solido High-Sigma Verifier uses ML to provide fully automated, brute force-accurate verification results at 4, 5 and 6+ sigma orders of magnitude faster than brute-force methods

Summary

Integrated circuit verification requirements have greatly expanded due to the increased complexity, scale, and mission-critical operations of semiconductor designs. For SPICE-level verification, ML methods provide a powerful approach to addressing the limitations of traditional brute-force Monte Carlo methods.

In addition to achieving SPICE verification at a fraction of the runtime of naïve solutions, several principal factors determine whether an ML solution is production ready: verifiability, accuracy, generality, robustness, and usability. ML solutions can be classified from level 0 (no ML) to level 4 (full production readiness). Each level of ML capability requires exponentially more R&D effort and production testing to achieve.

Solido High-Sigma Verifier, part of Solido Variation Designer, is an ML-enabled solution that provides full brute-force

accurate verification results at 4, 5, and 6+ sigma, with orders-of-magnitude less simulation runtime. With High-Sigma Verifier, design and verification teams can increase verification accuracy and coverage, while significantly reducing design schedule times. High-Sigma Verifier is an example of a level 3 ML algorithmic design, which is quickly approaching level 4 through large-scale production use and iterative improvement.

For more information on Solido Variation Designer, please visit the [Solido Variation Designer](#) information page at Siemens EDA.

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