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Fast and accurate variation-aware mixed-signal verification of time-domain 2-step ADC

Executive summary

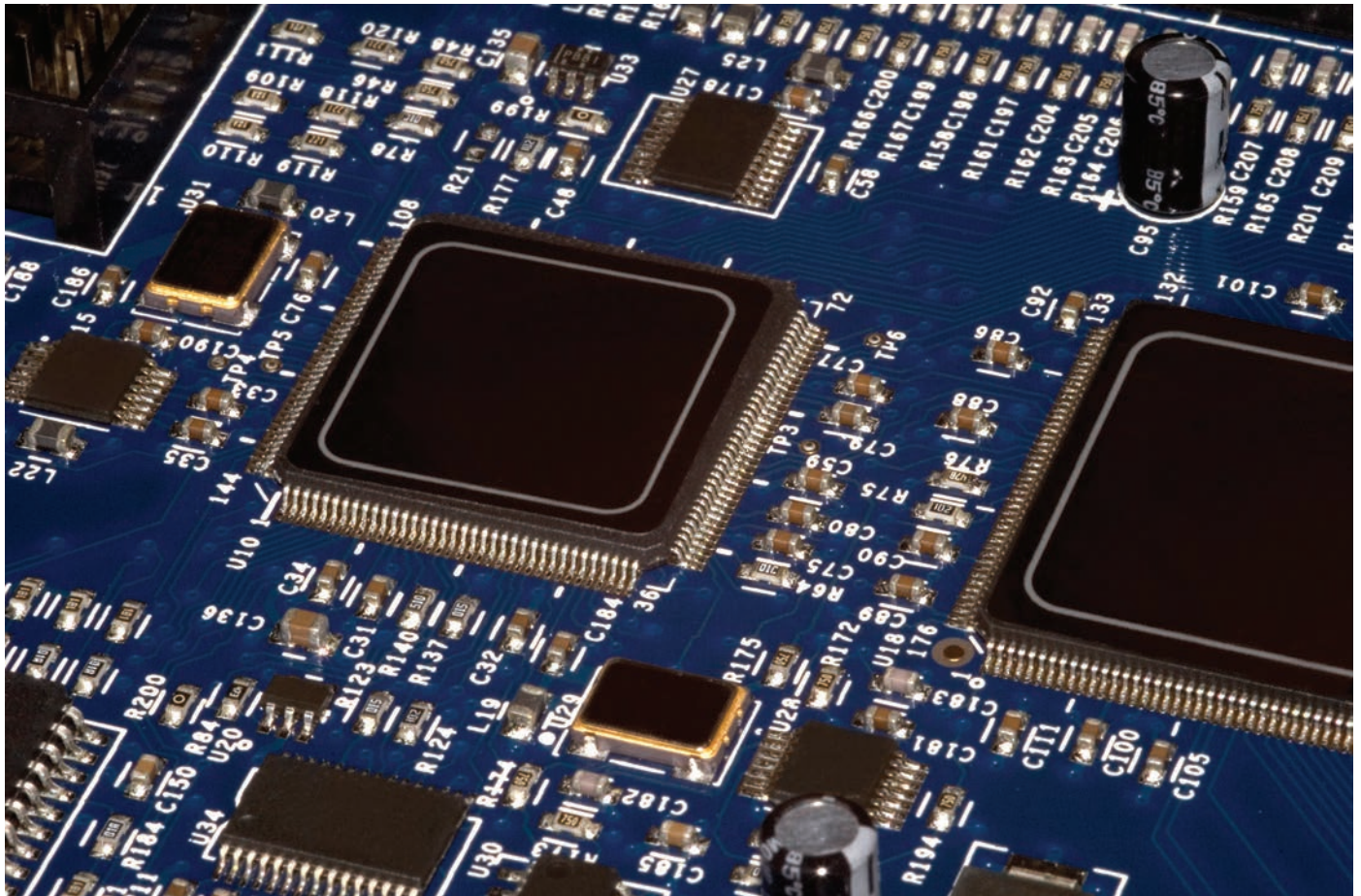
To meet today's analog-to-digital converter (ADC) specifications and to produce a high-yield design, teams typically need to perform extensive brute force mixed-signal simulations to account for all potential design variation. However, at nanometer nodes, the number of process, voltage and temperature (PVT) corners and parametric variation grow exponentially making the simulation impractical and costly. Teams attempt to employ extrapolation methods to shorten verification times. Learn how Analog Value Ltd. instead used Solido™ Variation Designer™ to perform PVT corner and Monte Carlo Simulation all at once to reduce simulations by orders of magnitude, but with the accuracy of brute force simulations.

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Introduction

Analog-to-Digital Converters (ADCs) are prevalent in today's SoC designs. The next-generation automotive, mobile and high-performance computing applications demand the use of nanometer nodes, to deliver more functionality and higher performance with lower power consumption. To meet the ADC's specifications and produce a high-yield design, designers need to perform extensive brute force mixed-signal simulations to account for all potential design variation. However, at nanometer nodes, the number of process, voltage and temperature (PVT) corners and parametric variation grow exponentially making the simulation impractical

and costly. Consequently, design teams are pressured to adopt extrapolation methods to shorten the verification cycle. The design team at Analog Value used extrapolation methods for verifying their Time-Domain 2-step ADC, to meet time-to-market demands, at the risk of impacting the design yield. This paper discusses the challenges they faced with the existing statistical variation verification methodology, and how they used Solido™ Variation Designer™ and Symphony integrated solution to achieve a robust variation-aware mixed-signal verification and meet their design yield requirement.



The motivation for time-domain 2-step ADC architecture

The Analog Value team selected the Time-Domain 2-step ADC architecture for their client's automotive RADAR application using a 22nm FDSOI GlobalFoundries process node. The traditional voltage domain high-resolution ADC at nanometer process nodes does not have enough dynamic range as the supply voltage level goes down. In contrast, the Time-domain 2-step ADC exhibits high resolution and better performance at nanometer nodes. This is achieved by converting the analog input into a time pulse and then digitizing it into digital codes¹. The architecture consists of a substantial amount of digital logic content to perform the bubble correction encoding and manage the algorithms to avoid meta-stability². The sensitive and high precision analog blocks, such as the comparator, are a vital part of this architecture. The dominance of and a bias towards digital design provides the opportunity to take advantage of automated design methodologies, resulting in high design efficiency and productivity. Recently, this has led to the proliferation of time-domain ADC circuits that are not dependent on the supply voltage, but take advantage of the benefits that come with high-performance nanometer nodes.

Figure 1 shows the Time-Domain 2-step ADC implemented by Analog Value. In the input stage (lower-left corner of the diagram) the voltage is converted to the time domain by using a pulse width modulation (PWM) technique so that each sample of the input signal is transformed into a time difference

between two signal edges. The voltage-to-time conversion and measurements are performed in two steps. Analogous to a measuring tape, with coarse and the fine divisions, the coarse time division is measured using the counters by counting the number of clock cycles. The fine time division is determined by using a set of close and equally distant clock phases. In this specific ADC, a set of 90 clock phases is used, and time resolution was approximately 5ps.

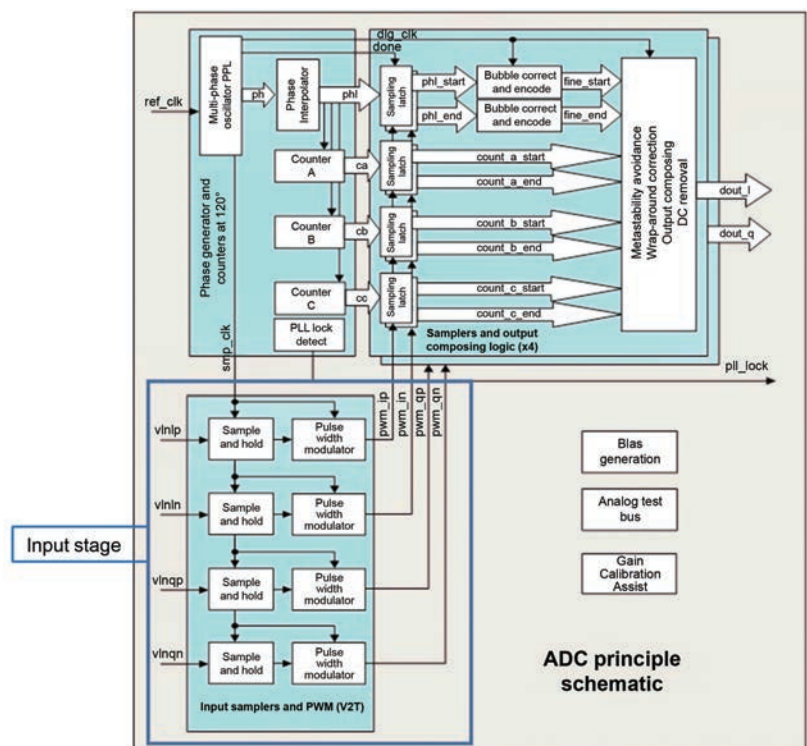


Figure 1. Time-Domain 2-step ADC block diagram.

The challenges with the existing traditional statistical variation verification

Analog Value's objective was to measure the impact of the comparator-latch sub-block statistical variation on the overall ADC's performance, measured in "effective number of bits" (ENOB). Their existing statistical variation verification methodology presented several challenges.

Performing the full brute force SPICE-accurate Monte Carlo simulation for the stages of the ADC is practically impossible as it required tens of millions of simulations. The team instead ran a limited set of brute force Monte Carlo simulations, 200 per corner as outlined in table 1, for a total of 3200 simulations. Then they used extrapolation to calculate the 4-sigma performance of the comparator-latch sub-block.

Process corners	4
Voltage supply variation	+/-5%
Temperature	-40 and 125 degrees C

Table 1. Simulation parameters.

To measure the influence of the comparator-latch statistical variation on the full ADC, the team ran only 100 top-level simulations. Extrapolation was again used to calculate the ADC's target 3-sigma performance, introducing the risk of compromising the accuracy of the results.

In addition, analyzing and identifying devices that are most sensitive to statistical variation and have the potential to cause functional failure in the ADC design was a considerable challenge.

The synthesized digital block performing the bubble-correct encoding was modelled in Verilog-A for top-level verification. Running SPICE-level simulation at the top using a Verilog-A model was very slow and did not verify the actual logic circuit that would end up in the chip.

Solido variation designer and symphony mixed-signal integrated solution for nanometer IC's

Analog Value used Solido Variation Designer and Symphony Mixed-Signal Platform integrated solution to address the challenges of accurately verifying the impact of statistical variation on their Time-Domain 2 step ADC.

Solido Variation Designer software provides a comprehensive suite of tools powered with machine learning to deliver unprecedented speed, accuracy and full variation-aware design and verification.

Symphony Mixed-Signal Platform, powered by Analog FastSpice™, enables fast and accurate mixed-signal verification with leading industry-standard HDL simulators providing an intuitive use model, powerful debugging capabilities and configuration support.

The Solido Variation Designer and Symphony integrated solution provides a variation-aware mixed-signal verification to meet the performance specifications and stay competitive in designing the best-performing quality nanometer ADC.

Verifying the comparator-latch

Analog Value used PVTMC Verifier in Solido Variation Designer to perform PVT corners and Monte Carlo simulation all at once, with orders-of-magnitude fewer simulations, but with the accuracy of brute force simulation. PVTMC Verifier enabled the design team to accurately extract the worst-case corner for the comparator-latch offset at the target 4-sigma without using extrapolation.

The measurement of interest for the comparator-latch simulation with PVTMC Verifier is the maximum standard deviation of the Offset_ps and its impact on ENOB. Figure 2 shows the worst-case standard deviation. The standard deviation offset of 7ps is unacceptable given the ADC LSB is specified at 5ps. This discrepancy in the resolution of the LSB was vital information for making design adjustments. The other key observation was that the quantile plot of Offset_ps shows that the tail of the

distribution is non-Gaussian. Hence, this is further validation that the existing statistical variation methodology based on extrapolation with the assumption that it is a Gaussian distribution would have led to inaccurate results, compromising the target yield of the ADC.

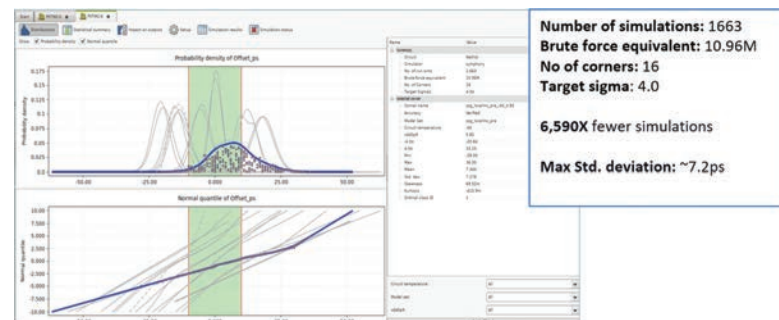


Figure 2. Comparator-latch PVTMC Verifier simulation results.

Improving the comparator-latch design

The powerful built-in sensitivity analysis capability in PVTMC Verifier helped identify the device in the comparator-latch with the most sensitivity to statistical variation and the most impact on the measured output. The designer gained insight on potential design adjustments to make and improve the performance of the comparator-latch design. In figure 3, the bar chart graph shows the device “phase latch p3” as the most sensitive to statistical variation. The scatter plot on the right shows its impact on the measured output offset.



Figure 3. Comparator-Latch sensitivity analysis results.

Verifying the top-level time-domain 2-step ADC

The Time-Domain 2-step ADC consists of substantial digital logic content as outlined earlier. Running SPICE-level simulation on the digital blocks with the precision required for the analog sub-block, such as the comparator-latch, was not feasible due to very long simulation run times. Hence, the design team decided to replace the digital logic with functionally equivalent RTL code.

Using the Solido Variation Designer and Symphony integrated solution, Analog Value applied the worst-case corner extracted from comparator-latch simulation and performed 100 variation-aware mixed-signal

simulations at the top-level ADC to achieve the target 3-sigma. Symphony identified which block is RTL and which is SPICE, and automatically inserted the appropriate boundary elements in the simulation. Figure 4 shows the Gaussian distribution and simulation results with an order-of-magnitude fewer simulations and the accuracy of brute force.

The ENOB loss of ~ 1.5 LSB for the 12-bit ADC is required to achieve the performance specification of $ENOB \geq 10.5$ bit. Solido's PVTMC Verifier provided the full real 3-sigma simulation data to verify the ENOB result.

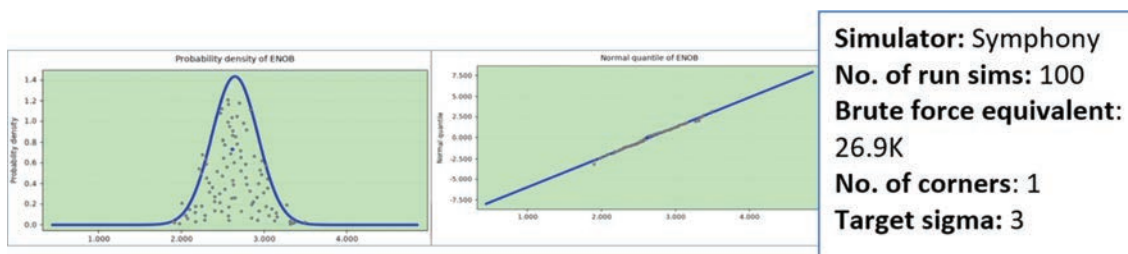


Figure 4. ADC top-level simulation results.

Conclusion

Analog Value's previous statistical variation verification methodology required extensive brute force simulation and extrapolation to calculate the target sigma performance at the analog sub-block level and for the top-level ADC. In addition, performing efficient variation-aware mixed-signal simulation with sensitivity analysis was not possible, thus introducing potential risk of missing the ADC design yield at nanometer nodes.

Analog Value adopted PVTMC Verifier in Solido Variation Designer. PVTMC Verifier helped achieve accurate and comprehensive verification coverage across 16 PVT corners for the comparator-latch stage. The design team gained significant productivity boost with 6590X fewer

simulations than brute force Monte Carlo at the target 4 sigma without extrapolation. Subsequently, for top-level ADC verification, they used the unique Solido Variation Designer and Symphony integrated solution to perform fast and accurate variation-aware mixed-signal verification to achieve the 3-sigma target. The powerful sensitivity analysis capability in Solido Variation Designer identified and provided insight into the devices with the most sensitivity to variation. The design team easily and quickly made design adjustments to meet the ADC's performance and to achieve high design yield.

References

1. A new highly-linear highly-sensitive differential voltage-to-time converter circuit in CMOS 65nm technology 2015 (IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon).
2. Implementation of mux based encoder for time to digital converters architecture (International Journal of Engineering and Techniques - Volume 4 Issue 3, May 2018).

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