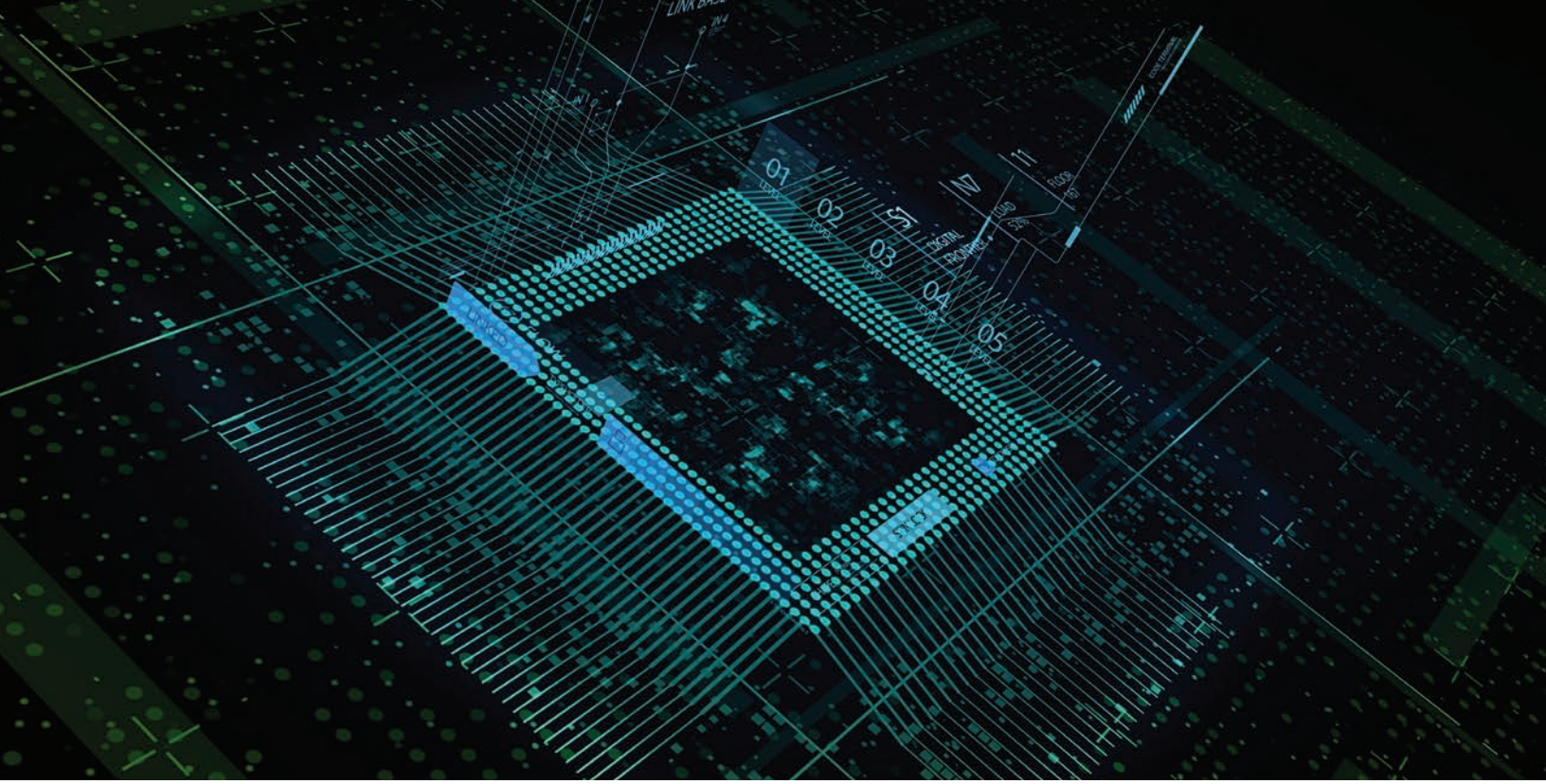

DIGITAL INDUSTRIES SOFTWARE

Analog mixed-signal verification methodology

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Executive summary
Complementary metal-oxide-semiconductor (CMOS) image sensors are a major driver in lucrative digital imagery markets. Used in today's digital cameras and mobile phones, CMOS image sensors (CIS) have strict high-resolution and high-frame rate requirements. As a result, design verification of CIS is a major challenge. This white paper details how a leading global manufacturer of electronic instruments and electromechanical devices adopted Siemens EDA's Analog FastSPICE™ (AFS) platform with AFS eXTreme technology and Symphony mixed signal platform to realize over a 3X speed improvement compared to competitive solutions while maintaining required accuracy.

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Introduction

CMOS image sensors drive surging digital markets

The CMOS imaging market has experienced significant growth over the last decade. Figure 1, graph(A) shows the upward trajectory of a double-digit cumulative aggregate growth rate (CAGR) of CMOS image sensors projected to 2024. Though the COVID-19 pandemic resulted in a dip in 2020, the upward trend continues with growth coming from diverse markets. Figure 1, graph(B) shows that although smartphone cameras continue to be the largest market segment, with an increasing focus on self-driving cars the automotive market is experiencing the fastest growth. Internet of Things (IoT), industrial and security applications are also showing a consistent upward trend.

CIS architecture and components

Figure 2(A) depicts a generic architecture of a CMOS image sensor that consists of a pixel array, column parallel ADCs, phase locked loop (PLL), image signal processor (ISP), DRAM and a SerDes interface. Figure 2(B) depicts a pixel array. It is a key component that consists of a photodiode and rows-columns circuitry. The charge from the photodiode is converted to a voltage at each pixel. If the row is enabled, a signal is sent to a noise-cancelling circuit that further relays it to the ADC.

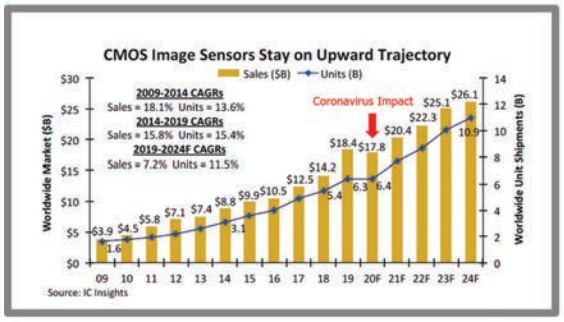


Figure 1(A): CMOS image sensor CAGR.

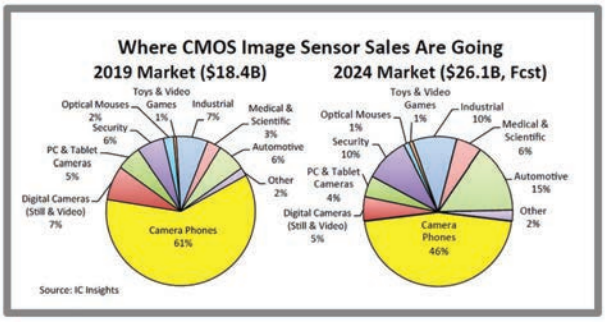


Figure 1(B): CMOS image sensor sales.

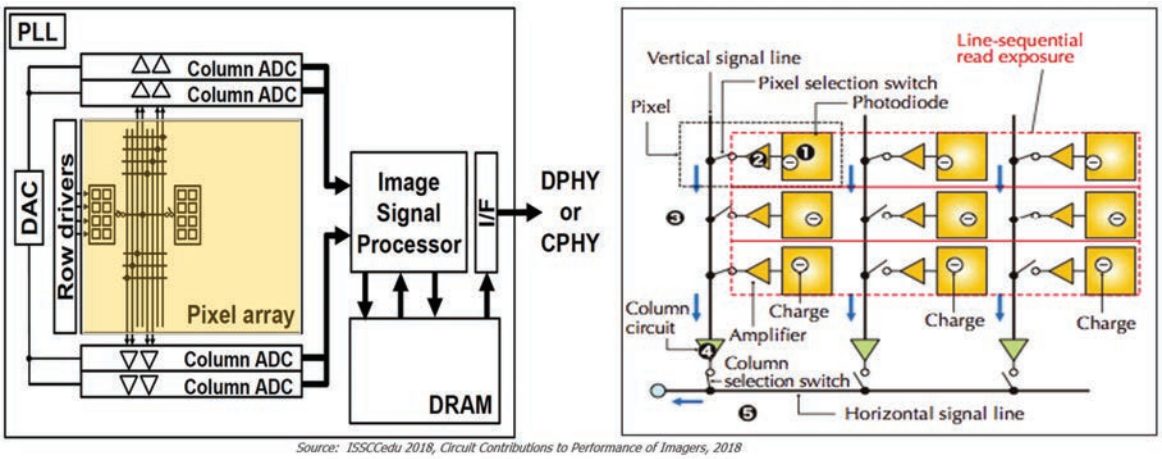


Figure 2(A): CIS architecture.

Figure 2(B): Pixel array.

CMOS image sensors: Design challenges

There is a constant drive to lower cost while improving the quality and reliability of CMOS image sensors. Optimizing for noise effects is one of the biggest challenges for designers today. They must account for very diverse noise including thermal, shot, kTC, 1/f, Dark Fix pattern and quantization noise as depicted in figure 3. Due to repetitive structure and signal coupling from adjacent readout columns switching simultaneously, there is a concern for crosstalk, especially when pixel pitch is close to 1um. There are also many switching currents, multi-modes of operations and requirements to have higher I/O performance. As these requirements are starting to grow, there is more and more digital integration coming into the picture to mitigate these challenges.

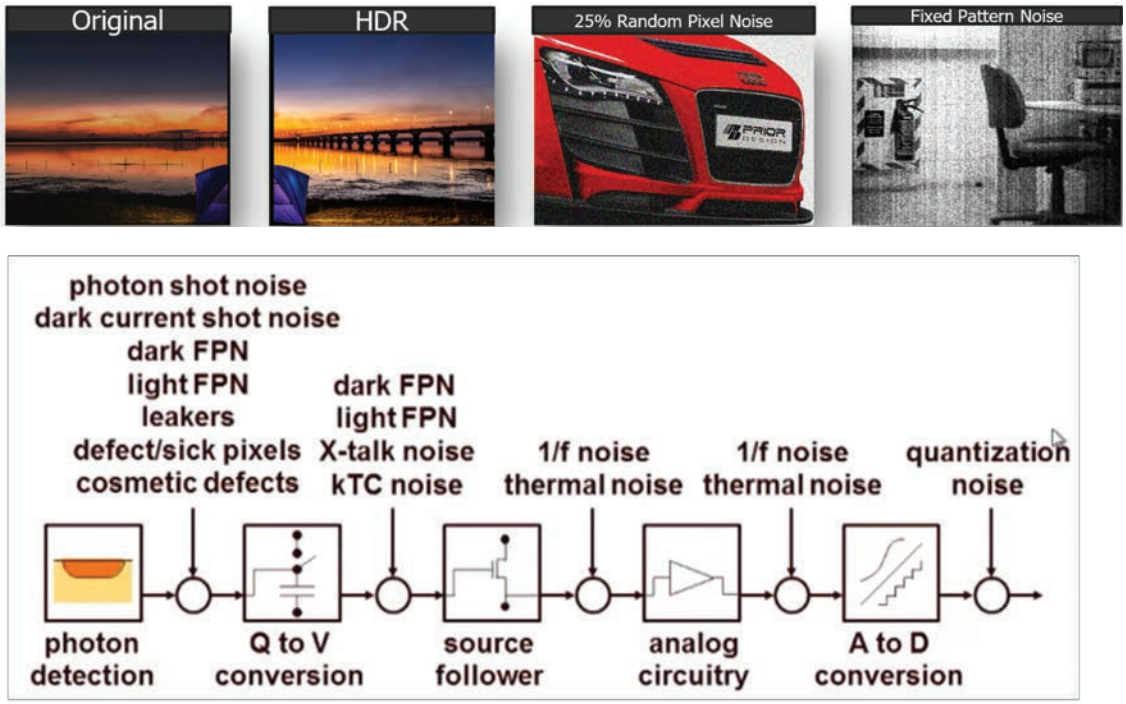


Figure 3: Sources of noise in CMOS image sensor. (Source: IEEE circuits & devices).

About Ametek

Ametek (formerly Forza Silicon) develops high-performance, low-cost, and low-power CMOS image sensors that are used in a wide-spectrum of applications including automotive, high-end medical devices, professional cinematography, and next generation broadcast cameras and networked video surveillance. Their expertise spans from ultra-high-resolution sensor design (208 megapixel) to complete digital cameras-on-chip systems and stacked CIS designs.

CMOS image sensor for high-end cinematography applications

There are a unique set of challenges in designing CMOS image sensors for cinematography and other high-end consumer applications. Particularly important are high resolution and high frame rates. Ametek has extensive experience in designing CMOS image sensors for four different categories of high-end camera markets.

Digital Cinema (> 4K Format | 60-120 FPS) • 24 MP, 6 µm pixel, 14bit, 100 fps	DSLR • 36 MP, 4.8 µm pixel, 14-bit, 10 fps, HDR
Broadcast (> 8K Format | 60-120 FPS) • 133 MP, 2.5 µm pixel, 12-bit, 60 fps	Virtual Reality/High Resolution (Up to 163 MP) • 163 MP, 1.5 µm pixel, 12-bit, 20 fps

Design specifications and architecture of an image sensor for cinematography applications

Figure 4 shows the building blocks and connectivity of a cinematography image sensor. The typical cinematography image sensor comprises of 100MP+ full-frame sensors with 60 to 120 frames per second (FPS) frame rate. The majority of the chip is occupied by the giant pixel array of 100MP or greater in the full-frame image sensor format. The pixel array is driven by the row-logic block which selects one row of the pixel array at a time and generates timing waveforms to stimulate the pixels for reset and transmit modes. It's a column parallel architecture where the output of each column of the pixel array is buffered by a source follower stage (called VLN), then sampled and converted to a 12-bit digital signal by the single slope ADC. An on-chip ramp generator driving the ADC and ADC counter latches signal-dependent values in the analog SRAM on chip. The digital logic samples the SRAM values for multiple columns and performs a 64/66b encoding before passing the data to the serializer. A 50MHz differential input clock is provided to the chip, which is received by the clock receiver. The clock receiver further generates a 50MHz CMOS reference clock for the PLL. The output of the PLL is a 2.5GHz (or higher) high speed clock signal which drives the serializer.

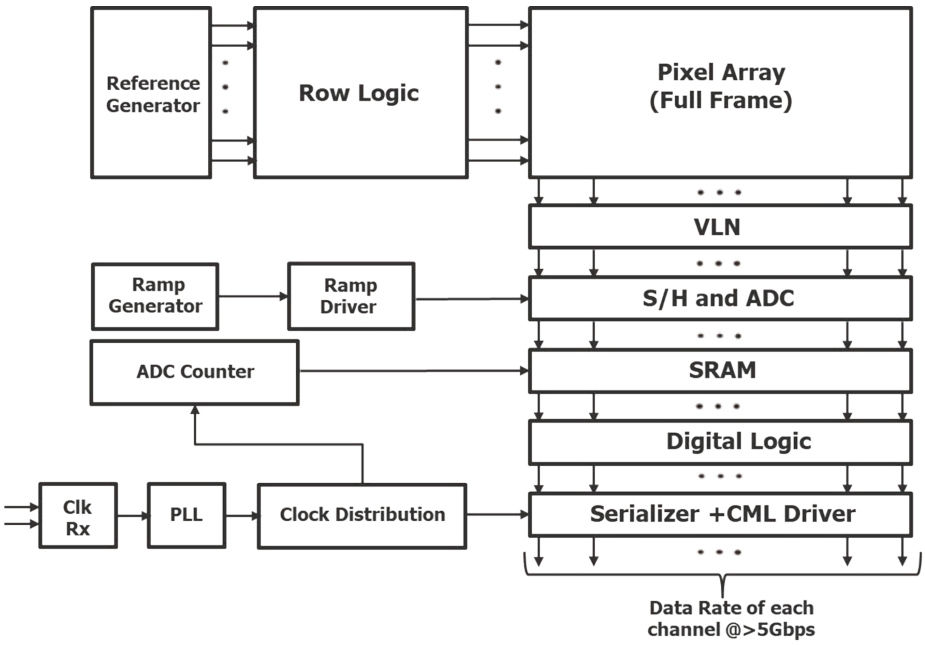


Figure 4: Block diagram of a cinematography image sensor. (Source: Ametek)

Figure 5 shows the block diagram of the analog readout chain. The analog readout chain is column circuitry that consists of the pixel array, VLN, Sample and Hold, ADC and SRAM. To verify each of these sub-blocks, separate test-injection points are configured at the interfaces of each of the sub-blocks. This facilitates the injection of known signals at these interfaces and facilitates the verification of each sub-block separately.

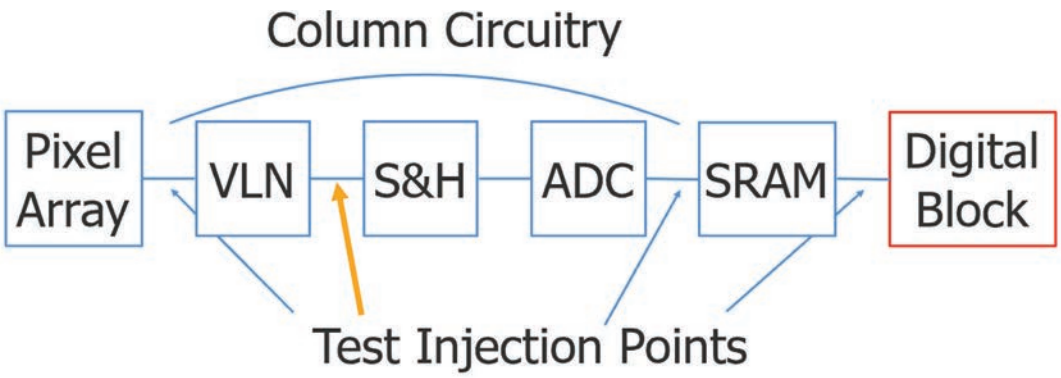


Figure 5: CIS analog readout chain.

Figure 6 shows the block diagram of the digital output chain of the CMOS image sensor. The ADC output is saved in the analog SRAM as a 12-bit digital data in gray code format. The digital logic first converts the 12-bit gray coded data to its 12-bit binary equivalent. After that, a packet of 64 bits is formed by concatenating five samples of 12-bit binary data and four bits of leftover from the sixth sample. In order to guarantee enough clock transition states for the CML driver, the 64-bit data packet is transformed into a 66-bit data packet via 64/66 data encoding.

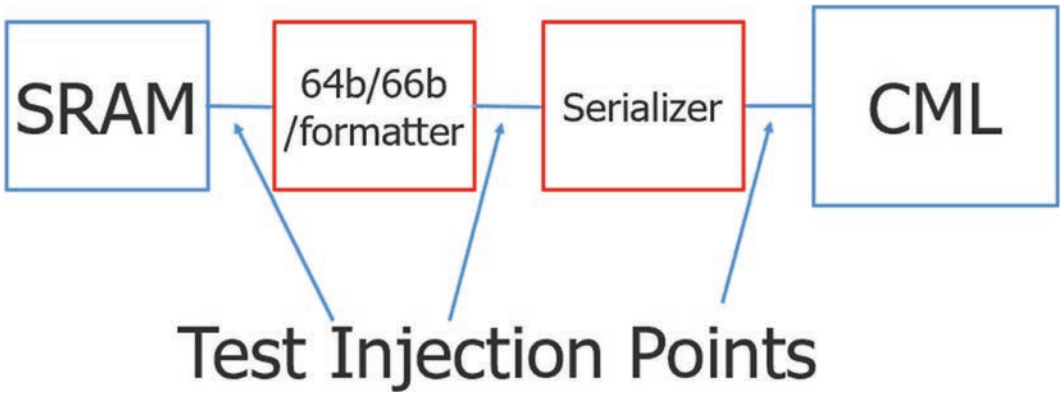


Figure 6: CIS digital output chain.

CMOS image sensor verification challenges

A typical CMOS image sensor system has a mix of analog and digital blocks. Sensitive analog blocks such as comparators require high accuracy simulations to account for noise effects. Pixel array is a key component and in order to verify large-array CMOS image sensors with layout parasitics, there is a need for a simulator that can perform high-capacity post-layout simulations. In addition to doing block-level characterization, design teams must verify the CIS top-level performance and functionality to ensure that noise, performance, and power specifications will be met in silicon.

Ametek verification methodology

The verification for the CMOS image sensors can be broken down in three stages as illustrated by figure 7. Firstly, at the pixel level, the interest is in characterizing performance in terms of device noise, dynamic range, linearity, etc. The second stage of verification consists of the analog readout signal chain consisting of the column circuitry. At this stage designers individually characterize the performance of each of the sub-blocks like VLN, S/H, ADC and SRAM both at the schematic level and post-layout extracted level. For the first two stages of verification, Ametek adopted Siemens EDA's Analog FastSPICE (AFS) platform with AFS eXTreme technology to achieve the desired accuracy at significant speed up compared to competitive simulators.

In the third and final stage, for full-chip functional verification of different modes, Ametek deployed Symphony, Siemens EDA's next-generation mixed-signal platform. Symphony is the industry's fastest and most configurable mixed-signal solution that accurately verifies design functionality, connectivity, and performance across analog/digital interfaces at all levels of the design hierarchy.

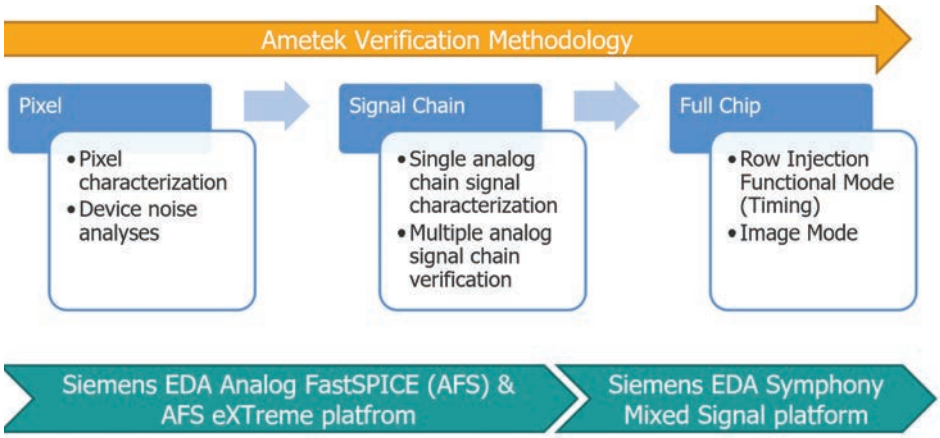
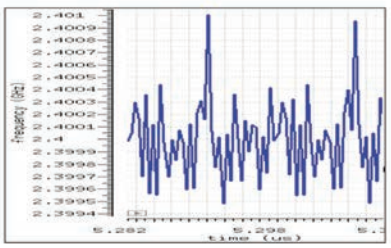


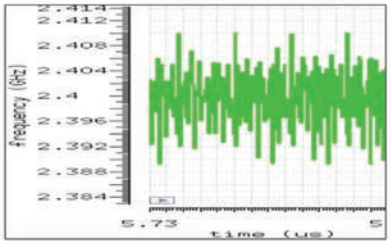
Figure 7: Ametek verification methodology.

Results of block level simulations

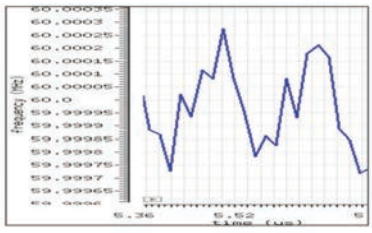
First, the output frequency and feedback frequency of the PLL are observed after it has locked. AFS eXTreme simulation results were compared with a competitor's tool across different simulator modes (red, green and blue modes for AFS and mode1, mode2 and mode3 for the competitor's tool). The modes are a sliding scale for speed/accuracy. It is evident that the output frequency and feedback frequency variation is higher in the competitor's tool compared to AFS eXTreme (figure 8).



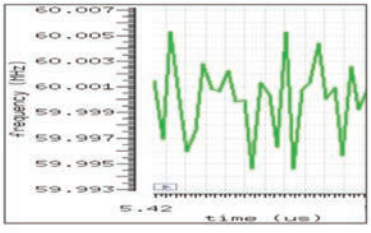
Output Frequency (AFS-XT blue)



Output Frequency (Competitor mode3)



Feedback Frequency (AFS-XI blue)



Feedback Frequency (Competitor mode3)

Figure 8: Output frequency and feedback frequency of the PLL.

One of the most important performance metrics for a PLL is its output jitter. When comparing the highest accuracy modes of AFS eXTreme versus a competitor, the design team observed that the AFS eXTreme red mode gives more accurate peak-to-peak jitter performance versus competitor mode1. A more interesting observation is that the AFS eXTreme blue mode gives a comparable jitter performance as competitor mode2 as highlighted in figure 9.

AFS eXTreme blue mode took 30 minutes versus the competitor's mode2, which took 100 minutes.

Therefore, at a comparable jitter performance AFS eXTreme outperforms the competitor's tool by more than three times in terms of simulation run-time (figure 10).

Though this graph showed PLL as an example, designers at Ametek experienced that AFS eXTreme helps reduce simulation time significantly while keeping acceptable accuracy for blocks, which needs to be verified by RC extraction like PLL, high-speed counter distribution, Serializer and CML. AFS eXTreme benefits significantly when running RC-extracted simulations.

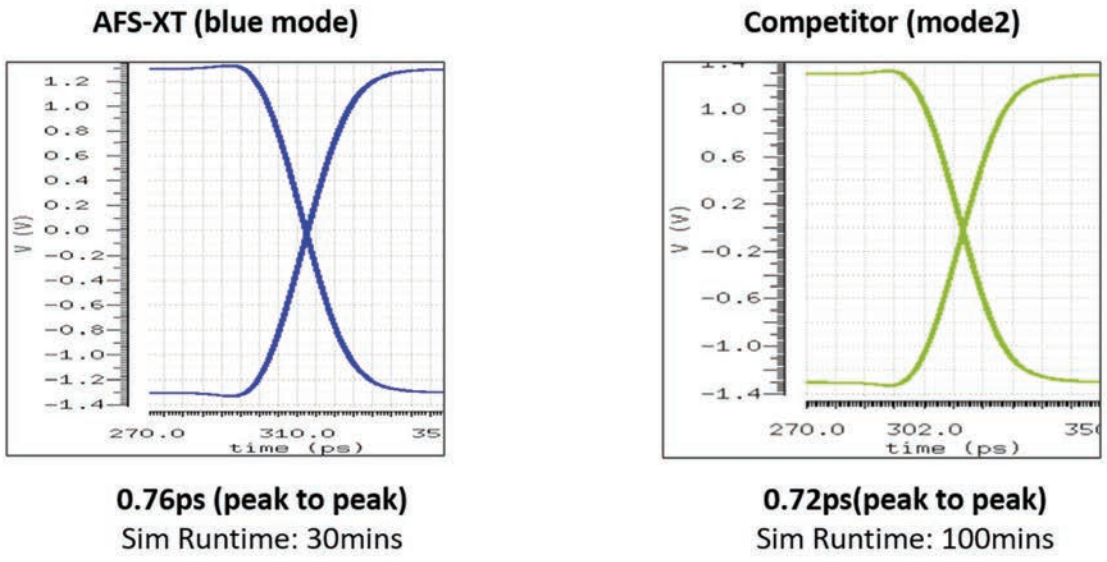


Figure 9: PLL jitter variation.

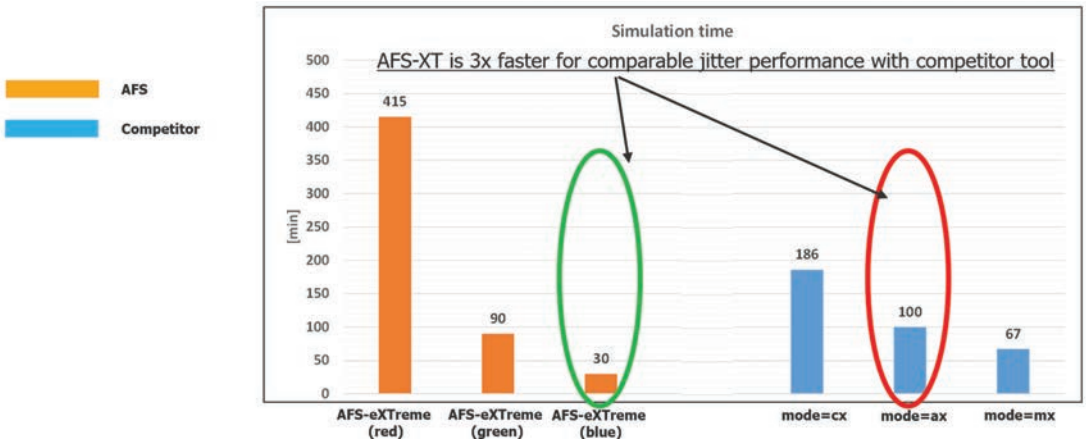


Figure 10: PLL simulation time (RC extracted).

Results of top-level simulations

The goal here is to do a full-chip functional verification with the Symphony mixed-signal simulator. The top level has more than 600,000 total elements in the Symphony netlist. Figure 11 shows the Symphony results. The upper set of waveforms show ramp signal, pixel output line signal and other sensitive analog nodes in the readout. The next set relates to important ADC timing signals which are in the digital domain. The next subsequent set shows vital pixel timing signals like Reset and Transmit. Finally, at the bottom are the gray-coded ADC counter and the output ADC latch signals with time of arrival proportional to the pixel signal level. The output of the ADC is latched onto the analog SRAM on-chip.

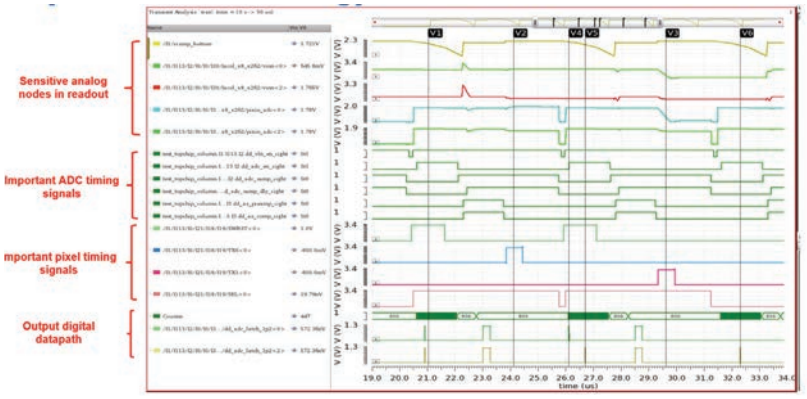


Figure 11: Simulation results: Top level simulation results (row and ADC timing).

Figure 12 shows the results of the 64/66b data encoding and serial data communication. The 48-bit gray coded output of the SRAM (for a particular row time) is first converted to its binary equivalent. The digital logic combines data from multiple row times in a 64/66b encoded data stream. The encoded data is serialized at a >5Gbps data rate and transmitted out using a CML driver to be decoded by an off-chip FPGA receiver. In this test case, the first packet from row 1 and row 2 are '0A5' '992' respectively, and the image snippet on the top-right shows the decoded data packet at the FPGA receiver. The decoded data pattern matches what was transmitted, validating the full chip operation.

Figure 12: Top level digital simulation results (full-chain mixed-signal sim using row injection).

Conclusion

CMOS image sensors for cinematography applications have very stringent high-resolution and high frame rate requirements. Verification of these designs are challenging due to the large size of parasitic extracted netlists and the accuracy requirements for precise noise analysis. For post-layout extracted analog block simulations, Ametek adopted Siemens EDA's Analog FastSPICE (AFS) platform with AFS eXTreme technology to achieve more than a 3x speed improvement compared to the competitor's tool while maintaining desired accuracy. For full-chip, Ametek leveraged Siemens EDA's Symphony mixed-signal platform for a flexible, easy-to-use solution to meet top-level functional verification objectives.

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