

DIGITAL INDUSTRIES SOFTWARE

A full-flow solution for analog/mixed-signal IC design

Custom IC design

Executive summary

Mixed-signal integrated circuits (ICs) are used in a wide variety of markets, including automotive, Internet of Things (IoT), imaging/display, industrial control, medical, sensors, radio frequency (RF), space and power management. Today's applications drive the need for higher levels of analog/mixed-signal (AMS) content on a system on a chip (SoC). These designs contain a hierarchy of tightly integrated analog and digital circuits, IP blocks, memories and I/O pads.

This paper introduces the tools that can meet the quality-of-results targets for engineers designing mixed-signal circuits on mature (planar) nodes at 22nm and above using the Siemens EDA IC full-flow.

Introduction

Siemens EDA IC full-flow

The Siemens EDA full-flow provides a rich environment that is highly configurable and flexible with many easy to use features for the mixed signal designer. The flow is optimized for creating custom analog or “analog-on-top” mixed-signal ICs at 22nm. It consists of highly-integrated front and back-end tools, from schematic capture to mixed-signal simulation and waveform probing, viewing, and RTL netlist synthesis to place and route, physical layout, and foundry-certified physical verification with the Calibre® platform. Open access (OA) for interoperability, multi-user and version control using third-party tool integrations are supported. The full-flow suite features a library manager, which provides a unified interface for managing and navigating all design libraries, cells, and views, including support for IC Manage, ClioSoft and SubVersion (SVN) version-control software.

Process design kits (PDKs) are a huge part of the analog and custom design environment which include OA data, CDF, callbacks, netlist procedures, and parameterized cells (PCells). Siemens EDA technology allows automatic conversion of third party PDKs, including callback and PCell code. Extensive automated QA process ensures identical and fully compatible results in Siemens EDA full-flow. There are broad offerings of PDKs that run in the IC full-flow environment. Siemens EDA has strong working relationships with key foundries resulting in fast enablement of PDKs for additional process nodes.

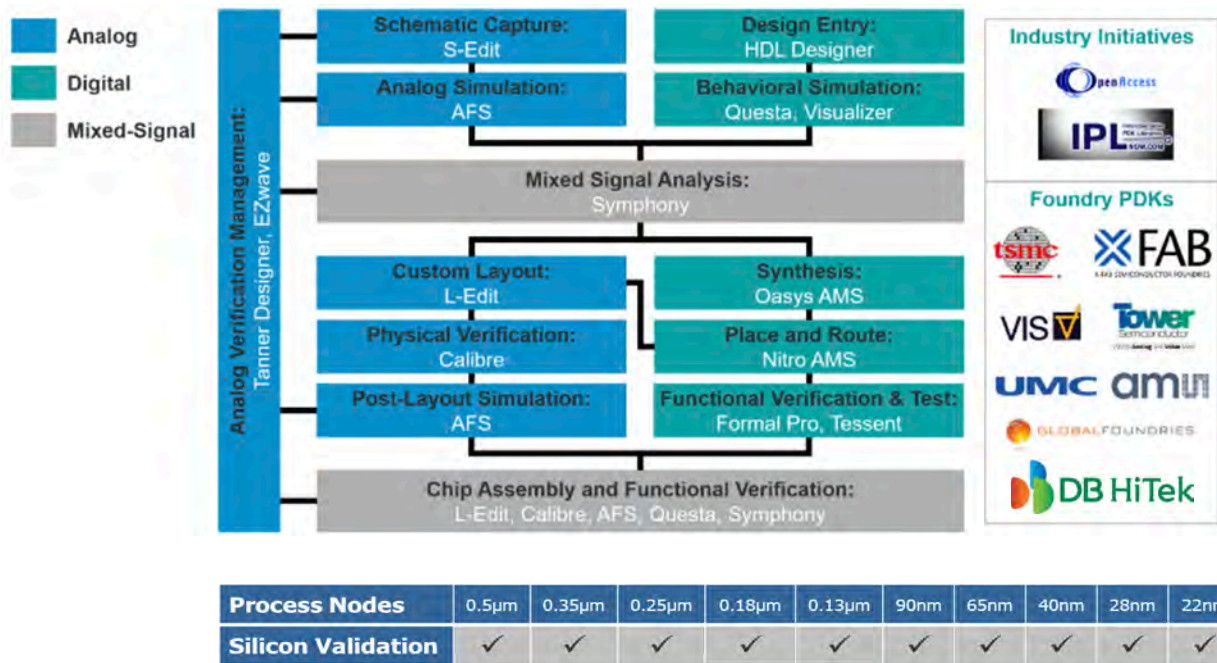


Figure 1: Siemens EDA full-flow.

Schematic capture with S-Edit

S-Edit

S-Edit is a full featured schematic capture environment, seamlessly integrated with all Siemens simulator offerings through an intuitive and highly customizable GUI. It is very easy to use out of the box with minimal user configuration effort, essentially eliminating the steep learning curves often required when switching tools. A comprehensive and customizable toolbar enables easy access to many design entry shortcuts, accelerating productivity as there's no need to look under complicated sub-menu and drop-down options. The libraries and cells associated with a design, the command window, and the properties menu are conveniently located in S-Edit and can be detached and easily reconfigured to suit any work style or display area.

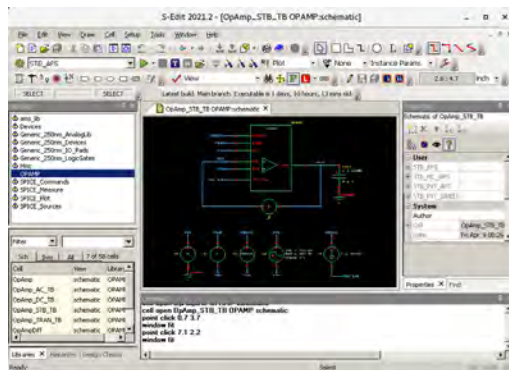


Figure 2: S-Edit schematic capture environment.

S-Edit has advanced array and bus support, easy to implement, fully compatible inherited connections and configurable schematic electrical rule checks (ERC). The designer can edit schematics and ERCs, and then netlist and simulate without the need to save design.

Multiple views

S-Edit supports schematic, SPICE, Verilog, Verilog-A/Verilog-AMS, and VHDL views, which enables designers to easily swap in abstract or detailed models on a cell-by-cell or instance-by-instance basis throughout the hierarchy.

Schematic compare

Often an existing chip design is used to create a variant where the designer would like to compare the original "golden" schematic to a current updated version, or they may find simulation results differ from a prior run and want to check the differences. S-Edit now has a very useful and quite unique feature to compare two schematic or symbol views to determine what changed. All differences are summarized in a dedicated detachable window, automatically zoomed-in and highlighted in the schematic canvas.

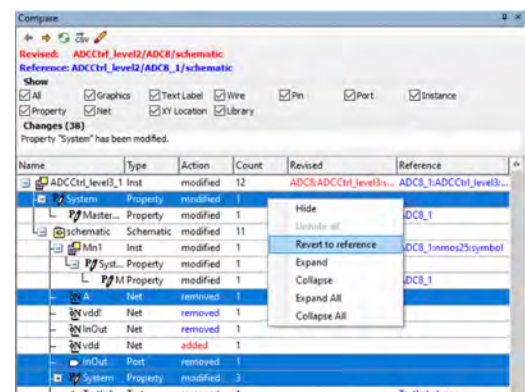


Figure 3: Schematic compare.

Customizable environment

The S-Edit environment can easily be customized through user-defined functions and menus, environment settings and bindkeys using Tcl scripting or the built in the Customize menu as shown below.

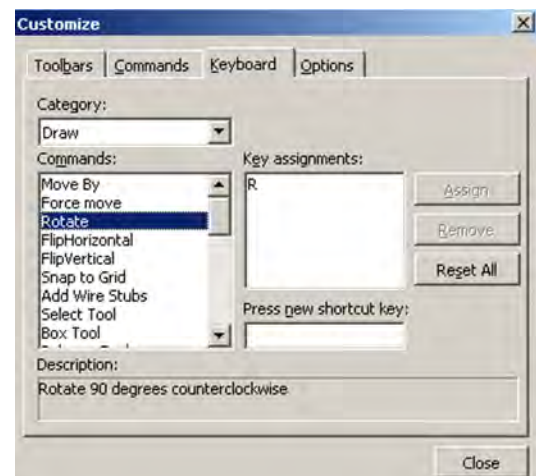


Figure 4: Customize menu.

Simulating with AFS and EZwave

AFS

The Analog FastSPICE™ (AFS) platform is the world's fastest nanometer circuit verification platform for analog, RF, mixed-signal and custom digital circuits, and is fully integrated with the S-Edit schematic editor. From the intuitive Setup AFS Simulation GUI within S-Edit, the designer can set up, launch the simulation and view the results in the EZwave™ software waveform viewer. All changes made in the Simulation Setup menu are stored in separate simulation testbenches with the associated schematic that simplifies verification at the start of a design. A user can simply open a schematic cell to access, review or re-run all stored simulation setups.

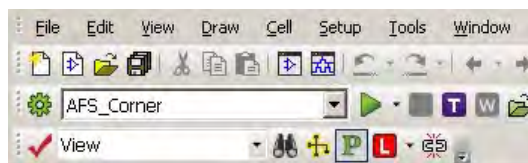


Figure 5: Pulldown to AFS Setup Simulation GUI.

Simulation results

In the S-Edit Simulation setup dialog, the designer can easily select the net voltages and node currents to be saved or plotted in EZwave using the toolbar icons in the Signals section in the Results pane. DC operating point voltages, currents and AC small-signal parameters can be back-annotated directly to the schematic. Below is an example waveform of the operational amplifier's PSRR performance.

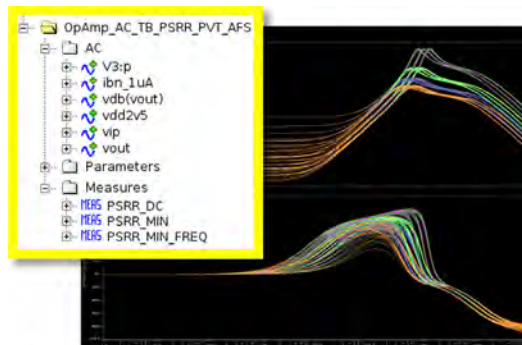


Figure 6: EZWave Waveform Viewer.

EZwave calculator integration

In the S-Edit Simulation Setup GUI there is a Results pane that seamlessly integrates the EZwave calculator for any advanced expression and output measurement construction during design. Output measurements and advanced calculator expressions are stored within S-Edit testbenches. After a simulation is complete, EZwave plots the expressions from the Results pane that evaluate to a waveform. Scalar results, like the Phase Margin or the DC Loop Gain, are also evaluated and shown in the same pane. An expression can be sent to and from the calculator for further editing or it can actually be modified in the Results pane manually.

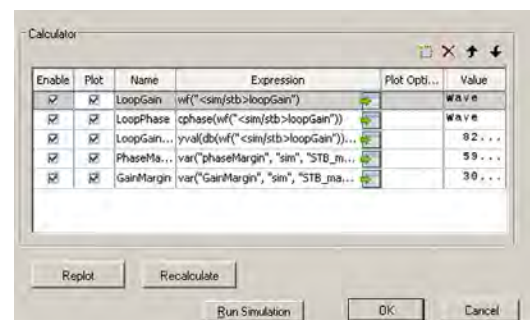


Figure 7: Calculator in Setup Simulation Results pane.

Tanner Designer

Tanner™ Designer software is an analog verification management tool that tracks simulation results in a convenient dashboard that allows the team to quickly see which blocks pass or fail specifications and to monitor verification progress. The enhanced inter-tool communication throughout the front-end flow (S-Edit, AFS, EZwave and Tanner Designer) provides greater efficiency in analog design, verification and debug.



Figure 8: Tanner Designer GUI.

Mixed-signal verification with Symphony

Symphony

Analog designers are challenged with implementing an increasing amount of digital content in their mixed-signal designs, for example high-speed ADCs with digital control logic. These designs require full-chip verification of large mixed-signal netlists with a high degree of accuracy and fast run times. The Symphony mixed-signal simulator is integrated in S-Edit, which combines the leading foundry-certified AFS circuit simulator. The Questa™ digital simulator provides fast and accurate verification of complex nanometer-scale mixed-signal ICs. The Symphony mixed-signal simulator can simulate digital and analog configurations with a streamlined and intuitive approach towards integrating both environments.

Symphony is proven on a wide range of ICs and IC subsystems, including ADCs, transceivers, PMICs, multi-GHz PLLs/DLLs and sensors. The efficient integration of Symphony with AFS fully leverages AFS performance, capacity and accuracy. The accuracy and performance in Symphony also enables running mixed-signal simulations for critical path checking of blocks at the transistor level in the context of the whole system.

Symphony is easy to set up and use. In S-Edit, the designer can select which view will be used in the simulation for specific instances using a click of the mouse. Supported views are Schematic, Verilog-A, Verilog, VHDL, and SPICE. For initial top level simulations, the designer may want to use different views. For example, Verilog-RTL for digital, Verilog-A for analog blocks, or transistor level views or parasitic Calibre views for more accuracy.

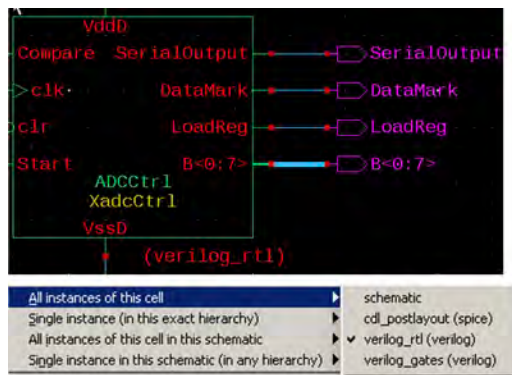


Figure 9: S-Edit cell view selection menu.

Boundary elements

For mixed-signal simulation, the designer will need to tell the simulator how to connect analog and digital signals when crossing a domain boundary. Symphony uses a novel approach to analog-digital boundary crossings known as boundary elements (BEs). In other tools, designers define connect modules with Verilog AMS code, which is tedious and error-prone. Boundary elements serve the same purpose as connect modules but are more powerful and easier to use.

Inside a sub-circuit/module, the connections are generally between same types of ports/nets. However, when sub-circuits/modules in different domains are connected, various combinations of connections may result. These different connection combinations result in the boundary element types, such as Logic (Digital) to Electrical (Analog) and vice versa, which are automatically added by Symphony when a signal crosses a domain boundary.



Figure 10: Boundary elements.

In mixed-signal design, errors most often occur at the interfaces between analog and digital blocks. Frequently, bugs in the interfaces are identifiable only at a higher level of hierarchy, for example at the I/O pins. In Symphony, the designer can display and analyze both the analog and digital results which aid in mixed-signal debug.

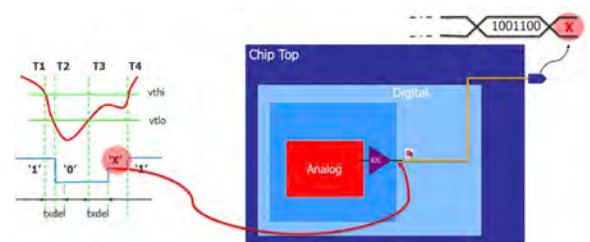


Figure 11: Mixed-signal waveforms.

Custom layout with L-Edit IC

L-Edit IC

L-Edit IC, Siemens's physical layout tool, can accelerate custom layout implementation with some advanced editing and ease-of-use features. L-Edit IC is built on OpenAccess and supports PCells, which are great for building flexible layout blocks for analog and mixed-signal designs. PCells are created for primitive devices and released in foundry PDKs, but can also be built for logic gates. The L-Edit IC environment, menus, and bindkeys are also customizable.

Schematic driven layout

L-Edit supports (SDL) schematic driven layout, which enables the layout designer to create a layout with PCells and a connectivity database from a schematic to save time and ensure layouts are correct by construction. PCells are generated in the layout with the parameters derived from the schematic devices and placed in the order they are arranged in the schematic when the user clicks on Publish to SDL in S-Edit. Connectivity enables the layout designer to graphically see connections between instances using flight lines, which aids in the routing process. Flight lines can be displayed per net or multiple nets from the SDL Navigator, and the colors are configurable by the user through a menu.

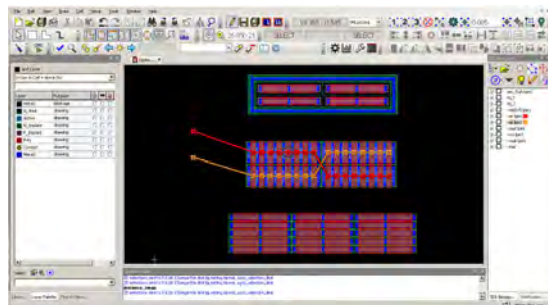


Figure 12: L-Edit layout editor environment.

Cross probing can be performed between S-Edit, Siemens' schematic capture and design entry tool, and L-Edit IC, Siemens' physical layout tool, by clicking on a symbol in the schematic that highlights the instance in the layout and vice versa.

Advanced editing features

In certain circuits, such as operational amplifiers, devices require a common centroid layout. There are significant matching errors when using transistors, or

resistors, or capacitors, if common-centroid layout is not used. The alignment toolbar, base-point, object snapping, swap instances, and duplicate features make placement and routing easier.

- Base-Point enables a user-specific reference point for editing operations using the cursor or specific coordinates
- Object snapping toolbar enables snapping of objects during drawing, moving or editing. You can enable different snap modes such as vertices, midpoints, edges, instances wire centerlines, rectangle center points and pins



Guard ring generators

Siemens L-Edit IC can automatically generate multi-part path structures for the purpose of creating a guard ring. Such guard ring cells can then be placed as guard rings around instantiated cells and selections. Default guard ring templates can use standard vias from the foundry PDK, or the user can configure their own.

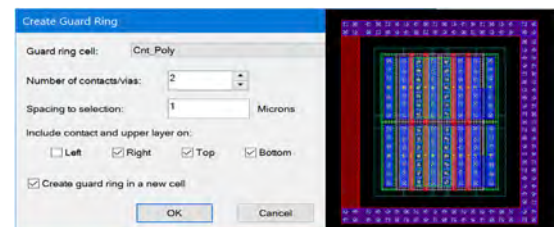
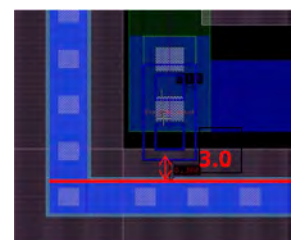


Figure 13: Guard ring generator menu.

Correct layout-as-you-go with Rule-Aware Layout

L-Edit IC Rule-Aware Layout displays violations while you edit your layout, helping you create compact, error-free layouts the first time. This feature simultaneously checks for violations between objects in the same cell and down through the cell hierarchy. You can display the distance between two edges while editing, display violation markers and have Rule-Aware Layout prevent violations by not allowing you to draw or edit a shape that would cause a violation (optional).



Digital implementation with Oasys and Nitro

Mixed-signal design methodologies

Analog/mixed-signal designers are faced with the challenge of implementing an increasing amount of digital content in their mixed-signal designs. An introduction to the digital implementation of these designs and how easily the user can integrate various mixed-signal blocks or IP components will be addressed in this section. Whether you are designing an analog IC with a small amount of digital control or a more complex mixed-signal ASIC, Tanner Digital Implementer (TDI) software from Siemens EDA has an ideal solution to meet the physical implementation.

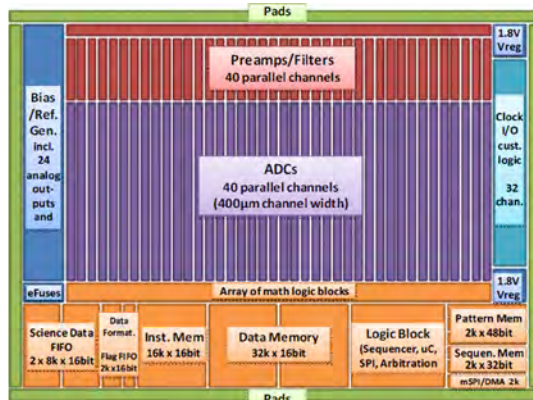


Figure 14: Source: Stargazer Systems, Inc.

Digital implementation with Oasys and Nitro

TDI can support two complementary design flows used for the physical implementation of mixed-signal designs.

- Analog-on-top (AoT) for an analog-centric design where digital control logic is integrated through a schematic driven flow
- Digital-on-top (DoT) for a digital-centric design where the analog/mixed-signal IP is imported through a netlist-driven HDL (Verilog/VHDL) flow

TDI solution

TDI provides an easy-to-use digital synthesis and place and route solution optimized for analog specialty planar nodes at 22nm and above. TDI is powered by Oasys-RTL™ software and Nitro® place and route engines, and can handle 75,000 instances per license and up to four licenses can be stacked. The patented “PlaceFirst” synthesis technology in Oasys improves

RTL optimization by performing placement ahead of synthesis, so high level optimization can be performed at the RTL level instead of the gate level. The high performance timing-driven place and route with patented multi-corner, multi-mode (MCMM) analysis and optimization architecture in Nitro insures design closure on timing, signal integrity, power and area. TDI supports floorplan and power plan functionality, clock tree synthesis, scan chain insertion for DFT and low-power design methodologies

TDI is integrated into L-Edit IC, the Tanner physical layout tool built on OpenAccess (OA), which is an advanced database that provides a comprehensive open standard data model and API for the design of integrated circuits.

Oasys and Nitro are launched from a GUI-driven wizard within L-Edit. This wizard simplifies the complex setup required for a digital place and route tool. Designers new to digital design will find the GUI intuitive and easy to use with a quick learning curve, resulting in less time being invested to become a digital “wizard” and faster turnaround. For experienced mixed-signal designers, Oasys and Nitro can be run from the command line. Both usage models provide access to reference flow scripts for further customization.

Nitro reference flow

TDI runs the Nitro reference flow, which is a unified set of scripts where the IC designer does not require comprehensive knowledge of the commands and options for running Nitro place and route. The Nitro reference flow is shown in figure 15.

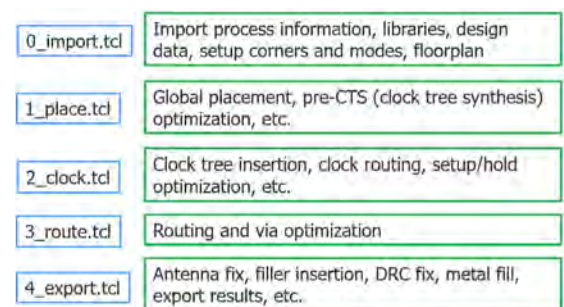


Figure 15: Nitro reference flow.

Physical verification with Calibre

Calibre interactive with L-Edit IC

Designers need tools that accelerate time-to-market. When performing physical verification of analog/mixed-signal (AMS) IC designs, speed is the name of the game. The Calibre verification tool suite is integrated with Tanner L-Edit IC Layout, allowing for precise location of errors, quick turnaround of corrections, and faster debugging. The adoption of Calibre as the sign-off standard at all of the top foundries ensures accurate results for first time success tape-outs. The following Calibre physical verification and extraction tools can be launched directly from L-Edit:

- Calibre nmDRC™ ensures that the physical layout can be manufactured. Using accurate and proven rulesets from the foundry, quickly debug violations for physical verification signoff

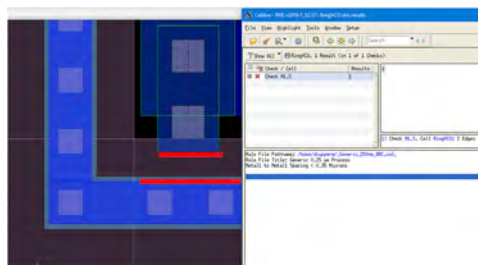


Figure 16: DRC results.

- Calibre nmLVST™ helps check whether physical layout is electrically and topographically the same as the schematic. Calibre nmLVST provides actual device geometry measurement, programmable electrical rule checking, and sophisticated interactive debugging capabilities such as highlight nets and devices with cross-probing to ensure accurate circuit verification

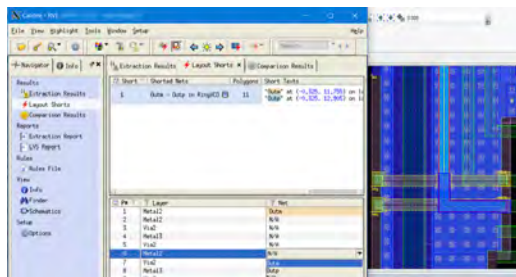


Figure 17: LVS short locator interface.

- Calibre xRC™ helps verify that layout-dependent effects do not affect the electrical performance of the design. It also delivers accurate parasitic data for use in comprehensive post-layout analysis and simulation
- Calibre RVE™ brings the solution together, providing a graphical results viewing environment that reduces debug time by visually identifying design issues instantly and cross-selecting the associated issue in L-Edit and S-Edit

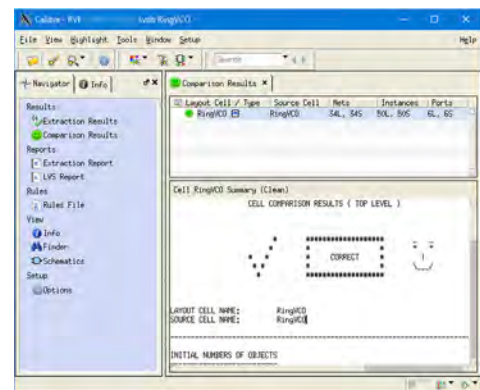


Figure 18: Calibre Results Viewer (RVE)

Calibre RealTime

The Calibre RealTime toolbar enables on-demand Calibre sign-off design rule checking for custom and analog/mixed-signal design flows, improving both design speed and the quality of results by providing immediate feedback on design rule violations and recommended rule compliance. The Calibre RealTime toolbar and options are available automatically when you install the L-Edit tool.



The Calibre RealTime client loads the complete Calibre rule deck, but also allows recipes that give the user control over what checks are executed for each Calibre run. When you run DRC with this integration, the tool only runs DRC on those geometries the user can see on the screen.

| Conclusion

This paper has presented how the Siemens EDA IC full-flow solution portfolio can help you design, verify and integrate various mixed-signal blocks or IP components, each containing a hierarchy of tightly integrated analog and digital circuits, including memories and I/O pads. Whether you're designing an analog IC with a small amount of digital control or a more complex mixed signal ASIC, Siemens EDA has a full-flow solution to meet the challenges mixed-signal engineers encounter designing on mature (planar) nodes at 22nm and above.

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