DIGITAL INDUSTRIES SOFTWARE

Analyzing EM/IR in IC design layouts to ensure reliability and performance

Executive summary

EM and IR drop are two critical design issues that can affect the performance and reliability of IC designs. Understanding the causes of EM and IR drop, and how to modify designs to minimize their impact, is essential to delivering IC designs whose manufactured performance and product reliability match the design intent. To complete these tasks efficiently, with confidence in the results, design teams need EDA tools that can quickly and accurately perform parasitic extraction and EM/IR analysis to enable them to analyze and optimize their designs to minimize EM and IR drop effects while still meeting tapeout schedules.

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Background

Integrated circuit reliability

Integrated circuits (ICs) are found in nearly every facet of our lives today, from the mundane, such as washing machines, televisions, and video games, to critical applications like transportation, communications, medical devices, and military systems and equipment. In all cases, IC reliability is an essential success factor. In the mass market, consumers make buying decisions that include product reliability as a factor. In applications where lives literally depend on the reliability of the system, failure is simply not an option.

Electrical reliability, however, is fundamentally different from mechanical reliability, which is what most people traditionally think of when they hear the term reliability. Electrical circuits don't wear out the same way physical parts do. Mechanical reliability typically means components linearly degrade over time from forces on the device, like friction or other stresses. ICs don't have any moving parts, so their reliability is mainly determined by external factors such as electrostatic discharge (ESD), electromagnetic fields, and variations in voltage and temperature.

As any electronics engineer knows, IC creation is a very intricate process. A typical IC contains billions of transistors, and trying to get those all those transistors to operate correctly for the expected lifecycle of a chip is a monumental task for IC design companies. As we progress to smaller process nodes, we can scale down transistor sizes and fit more on a chip, but that economy of scale also creates more complex device interactions, manufacturing challenges, and reliability concerns to be solved.

IC reliability follows a "bathtub curve" with three main phases: infant mortality, normal life, and end of life (figure 1). This curve is not unique to ICs—it is used widely in all reliability analysis to depict when things will fail [1]. The first phase, infant mortality, occurs in the early life of the chip, and is characterized by a sharply decreasing failure rate over time. Failures in this phase are mainly caused by process defects and manufacturing errors. The second phase, intrinsic failure, is the normal or

useful life of the device. This phase represents the longest period of the IC lifecycle, and is characterized by a low failure rate where the failures are stochastic. The last phase, wear-out, occurs after some period of time and is characterized by an increasing failure rate. This late-stage increase in IC failures occurs primarily due to effects of oxide degradation and interconnect degradation caused by a phenomenon known as electromigration (EM).

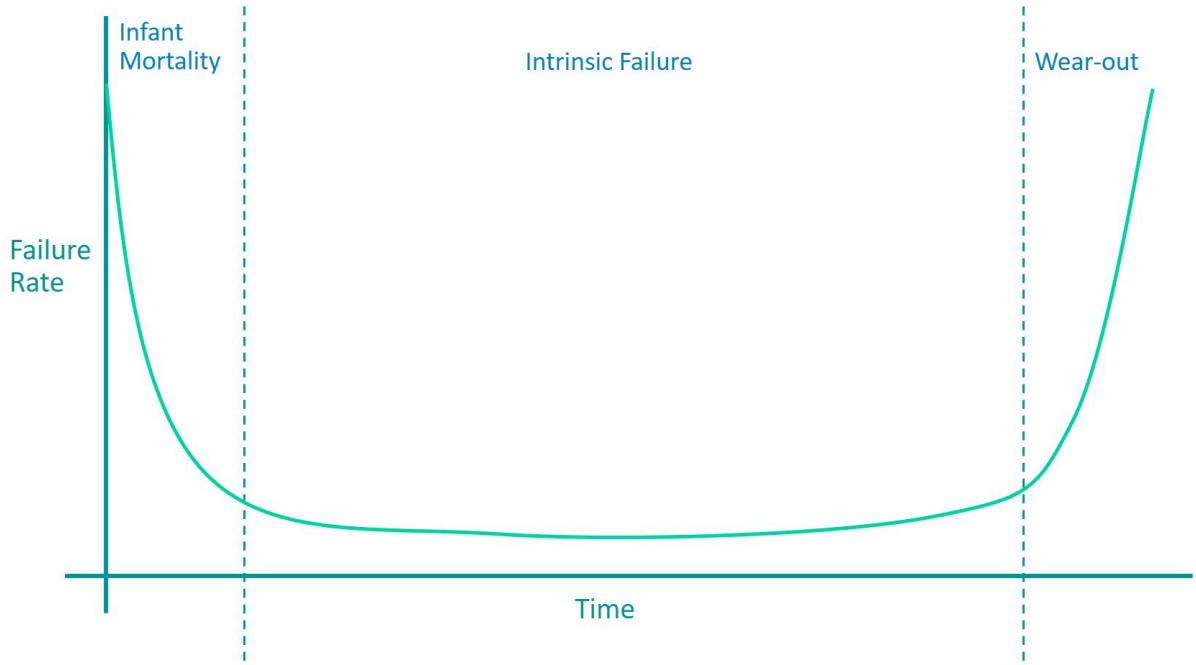

Figure 1. IC reliability curve (bathtub curve) reveals the failure rate of an IC as a function of time.

Electromigration

What is electromigration?

EM is the movement of metal atoms caused by the flow of current through the metal. The electrons flowing through metal move with some velocity, giving them some magnitude of momentum. When these electrons collide with the atoms of metal in the interconnects, they can transfer some of their momentum to the metal atoms, causing the metal atoms to move. Over time, the movement of these metal atoms

creates voids and hillocks in the metal interconnects, as shown in figure 2. Voids can widen and deepen until they create an open circuit in the interconnect, while hillocks can grow high enough to connect to other interconnect wires, creating a short.

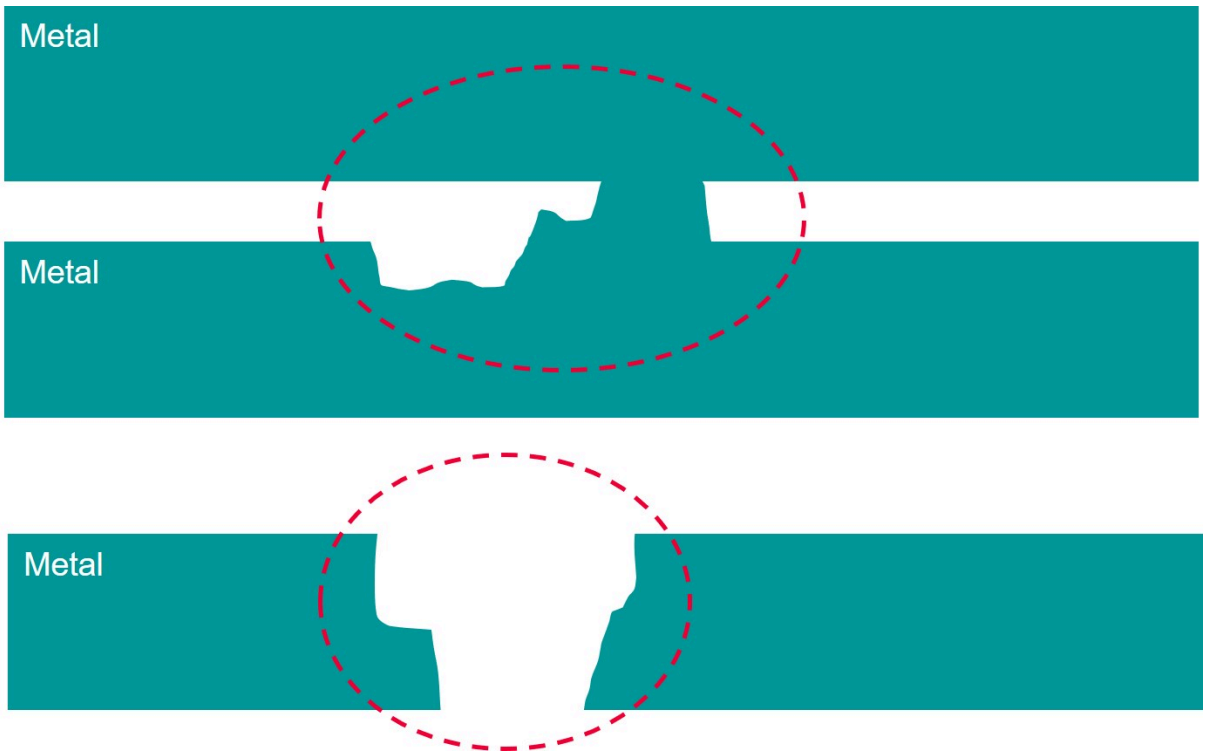

Figure 2. EM can create short circuits between two interconnects through the development of hillocks, or an open circuit through the creation of voids.

The risk of EM is directly correlated to the current density of the interconnects. The higher the current density, the more likely EM will affect the design. One of the primary techniques for predicting failure from electromigration is to simulate currents through the design and analyze the results to find those points where the current densities are beyond design limits. For this reason, one of the main locations of EM failure in ICs is in the vias. Because vias are a point of constriction in the conduction paths, they experience increased current density.

Other factors that influence the occurrence of EM are wire material, wire temperature, and wire size.

Black's equation

Black's equation (figure 3) enables engineers to quantify the variable factors that contribute to the occurrence of EM, providing a method for modeling the mean time to failure (MTTF) of an IC due to EM [4]. Current density is related to wire size—when the wire is wider, the current density is lower. While temperature varies throughout the chip, engineers typically use the worst-case temperature to measure MTTF.

$$MTTF = \frac{A}{j^n} e^{\frac{E_a}{kT}}$$

MTTF: mean time to failure
A: constant
j: current density
n: model parameter
E_a: activation energy
k: Boltzmann's constant
T: temperature

Figure 3. Black's MTTF equation and a description of all the variables.

Why is electromigration a growing issue?

EM has always been present in ICs. However, with the device scaling of today's advanced process node designs, it has become a serious threat to IC reliability. As transistors continue to be scaled down, interconnects and other components must be scaled down as well. Decreasing the size of interconnects increases their resistance and current density, making the interconnect more susceptible to EM.

A related issue of transistor scaling is self-heating, which is the increase in heat trapped in a device due to high current density and poor heat dissipation. Self-heating is especially evident in silicon-on-insulator (SOI) fin field-effect transistor (finFET) and gate-all-around field-effect transistor (GAAFET) technologies. These devices have limited dissipation paths to the thermal ambient, both because of their three-dimensional geometries and because the thick buried oxide layers used in these devices are not very thermally conductive (figure 4). This resistance to heat dissipation results in much of the internal heat in the device being transferred into the metal interconnects, which speeds up the EM effect.

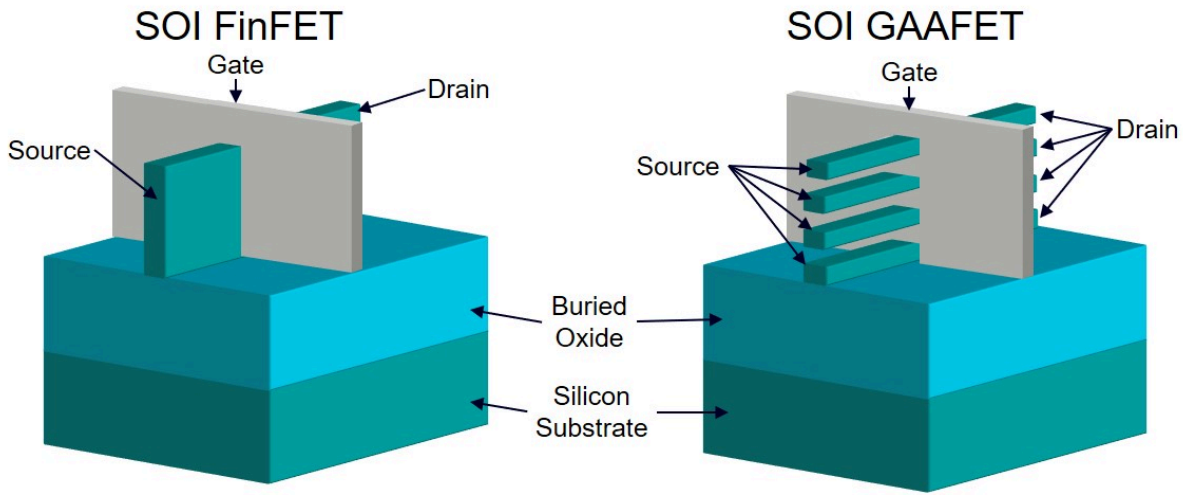

Figure 4. Construction diagrams of SOI finFET and SOI GAAFET devices, showing the buried oxide layer that impairs heat dissipation.

How do IC designers limit electromigration?

Wire width

The easiest way to avoid EM effects is to ensure that the interconnects are sufficiently wide enough to handle the current going through them (figure 5). However, that

solution is at odds with design scaling, especially at advanced nodes, so the semiconductor industry has developed alternative options that include changes in interconnect materials, as well as physical restrictions on interconnect length.

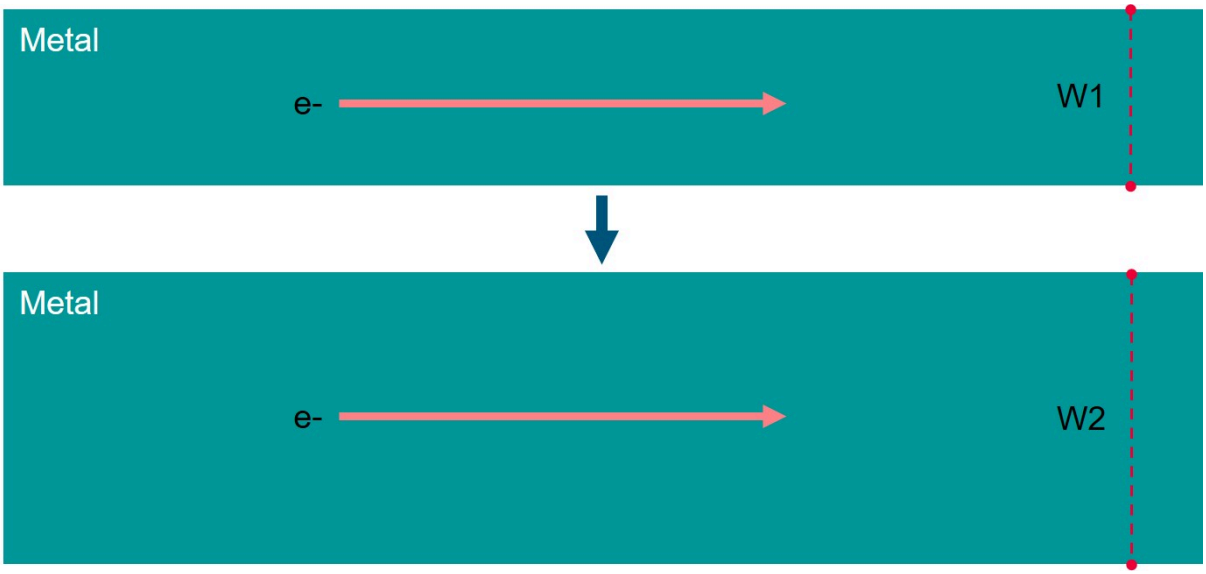

Figure 5. Wider wire widths can reduce EM risk, but are impractical in today's advanced node designs.

Around 25 years ago, the semiconductor industry started to hit a limit with how far aluminum interconnects could be scaled down before EM became a major issue. Copper interconnects, which have a lower resistivity and higher resistance to EM than aluminum, then became the norm (figure 6). Copper interconnects are able to withstand about five times the current density of aluminum, which was a significant improvement. However, as designs keep scaling down, we are now starting to reach the limits of copper. At this time, there is no other material available that is a significantly better conductor than copper.

Figure 6. Changing wire material to a lower resistivity metal, such as the shift from aluminum to copper, can reduce EM.

Barrier/Seed layers

EM primarily occurs on the boundary of a wire because the adhesion between the copper and the dielectric barrier is weak. To increase this adhesion, designers can

introduce a barrier layer between the edge of the copper and the dielectric (figure 7). This barrier, also known as a seed layer, is usually a copper layer doped with another type of metal, such as cadmium, calcium, or zinc.

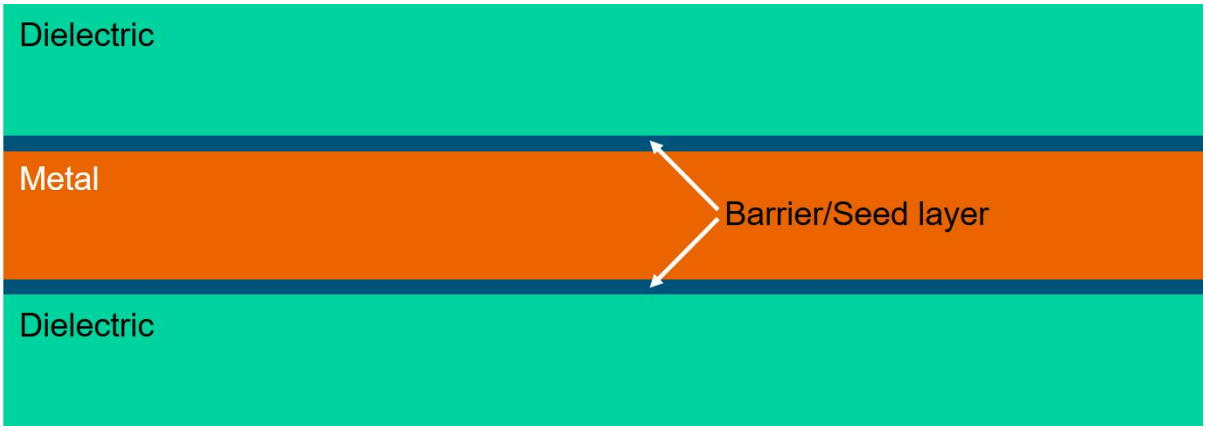

Figure 7. Adding a barrier/seed layer between the metal wire and dielectric can improve adhesion and reduce boundary EM.

Blech effect

Another way to mitigate EM is by utilizing the Blech effect, first described by Ilan Blech in the 1970s [3]. The Blech effect describes how electron migration creates a tensile stress at the upstream end of a wire and a compressive stress at the downstream end (figure 8). These stresses cause the sidewalls of the wire to become more rigid, which creates a backpressure against the stresses, in turn slowing down the migration. Additional research by Blech and others determined there is a certain ratio between line length and current density where no migration will occur, known as the Blech length. The Blech length is typically between 10 and 100 microns. By restricting the length of the interconnect to these dimensions, IC designers can limit EM effects.

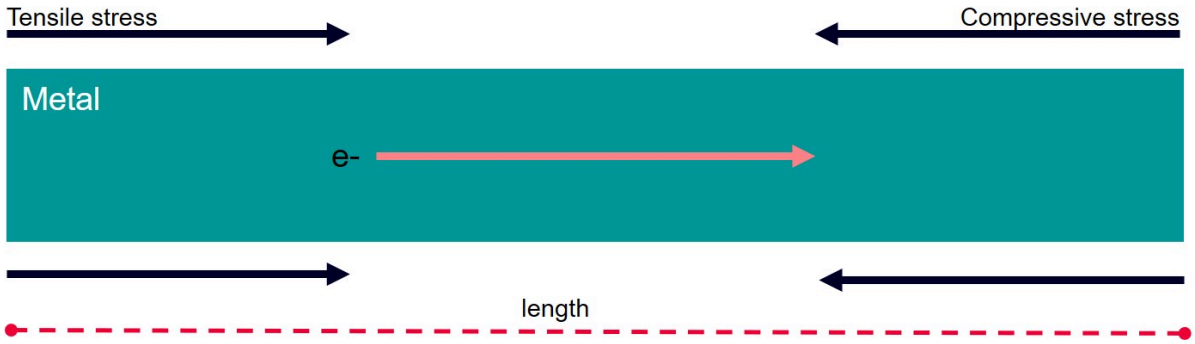

Figure 8. Compressive and tensile stresses caused by electron migration on a wire. There is a certain length where these stresses neutralize each other and no migration occurs, typically between 10 to 100 microns.

IR Drop

What is IR drop?

Ohm's law [5] defines voltage(V) = current(I) * resistance(R). As current flows through a resistor, it creates a reduction in voltage, called a voltage or IR drop.

Electrical power is needed for a chip to function. With device scaling, transistors and wires get smaller, but the chip dimensions remain relatively the same. This dichotomy means wires become narrower, but stay the same length, which increases the parasitic (unintended) resistance of those wires. Due to this increased resistance, the voltage in the path from a supply pin to the input of the cell that it must be used in decreases over that path (figure 9). This resistance continues to get exponentially larger as the industry moves designs to ever-smaller nodes [6]. For example, moving a 28 nm chip design to 7 nm results in approximately a 10x increase in wire resistance.

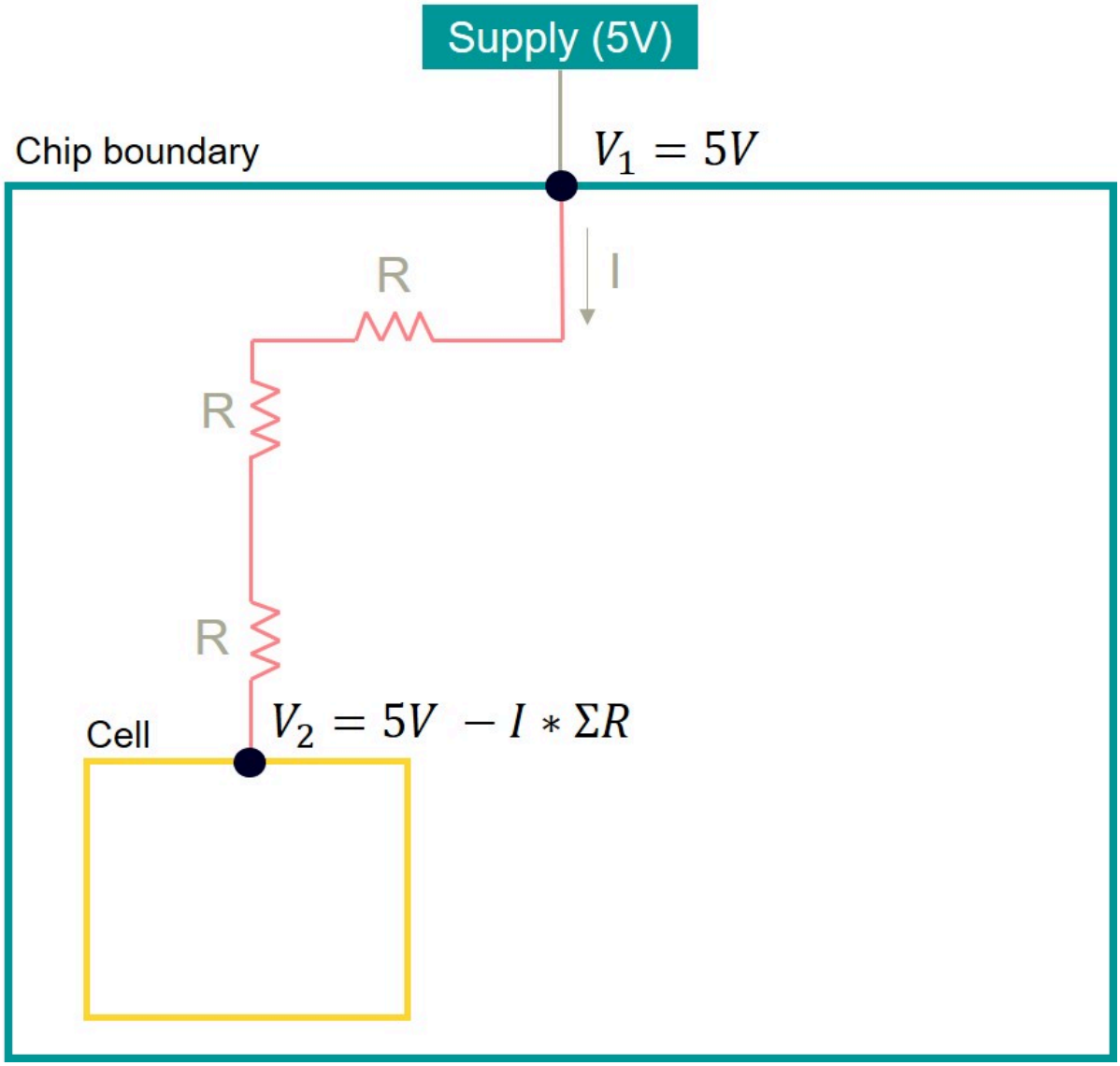

Figure 9. Distributed parasitic resistance in the interconnects between a supply pin and a cell reduces the original supply voltage. The voltage the cell receives is the supply voltage minus the IR drop in the wire.

There are two types of IR drop in a design, static and dynamic. Static IR drop is the voltage drop that occurs in the presence of a constant current draw due to parasitic resistance in the wires. Dynamic IR drop is a voltage drop caused by high switching activity of transistors. When many transistors switch at the same time, it can cause locations of high current on the chip. Dynamic IR drop is a time-based calculation that takes into account both resistance and capacitance effects in both parasitic and

designed devices. Dynamic IR drop, in particular, has been getting worse as power consumption and chip frequency (the frequency of the clock generator on the processor) increase at advanced nodes.

Why is IR drop analysis important?

As voltage drops, transistors operate more slowly, which can create timing violations. In turn, these violations can cause slower performance in the final chip. When manufactured chips don't meet their design specifications, they may have to be sold at a lower price for less-demanding uses, which reduces the anticipated revenue for that design. Timing violations can also cause functional failures of the chip, which can result in entire lots of chips that don't even make it to market. While it can be difficult and time-consuming to find and fix the root causes for IR drop, IR drop analysis is a critical step in the IC verification flow that helps designers achieve the lowest IR drop possible [7].

Static IR drop analysis identifies weaknesses in the power grid due to parasitic resistance impacts. If there are many voltage violations across the design, there may be too much resistance in the grid, and it may need to be re-designed. Dynamic IR drop analysis is more precise and indicative of the actual function of the chip because it simulates device switching as it would occur in normal operation. If there are many devices close together that are switching at the same time, localized areas can experience high currents during this time, resulting in timing violations if the IR drop is severe enough. Static IR drop analysis cannot recognize these device switching conditions because they must be measured over a period of time, not in one moment.

EM is also directly correlated to IR drop, as they both relate to effects that occur in interconnects. Higher resistance in wires not only causes more IR drop, but it also results in a higher current density, which causes EM.

How do IC designers minimize IR drop?

Since static IR drop analysis only evaluates the resistance of the wires, error correction techniques focus on reducing resistance. The primary modification is to increase the width of the metal wires. However, vias are commonly a point of high resistance in

designs because they are generally smaller than the metal wires they connect. If violations are caused by vias, then adding redundant vias along the metal helps reduce that resistance. These methods are very similar to the techniques used to limit EM.

Because dynamic IR drop includes both resistance and capacitance, one way to solve dynamic IR drop violations is to add decoupling capacitor (DCAP) cells. A DCAP cell is essentially a capacitor connected across the power and ground. When no switching is occurring, the DCAP cell is charging. When the device switches, the DCAP cell can discharge into the circuit to help provide more power, keeping the device voltage from dropping too much and going into a metastable state.
Other techniques include reducing the toggle rate of devices or moving cells to enable control of localized current spikes in designs.

Parasitic effects

Parasitic effects occur when an IC design layout creates conditions that allow the formation of unintended (parasitic) electrical activity in a circuit. Parasitics can take the form of resistance, capacitance, or inductance effects. Even though unintended, these parasitics have very real effects on electrical performance.

For example, current density is an important factor in EM mitigation. A simulation tool calculates the amount of current going down each line, based on the voltage, the parasitic resistance, and the operating region of all of the transistors.

In IR drop analysis, when the parasitic resistance is too high, the voltage will drop too much.

Careful design and layout of ICs can help minimize the impact of parasitic resistance, capacitance, and inductance. To ensure the optimal corrections are applied to a layout, designers need accurate parasitic extraction results.

Parasitic resistance

Parasitic resistance is a measure of the difficulty that electrons encounter as they flow through a conductor, which can cause data loss or other problems. In IC design, parasitic resistance is a major source of concern. To mitigate this resistance, designers try to ensure that the current passing through a circuit is as low as possible. They may increase the number of vias, which are areas where the current can pass through metal layers, or use thicker metal traces or widen the wires, to reduce the effects of parasitic resistance.

Parasitic capacitance

Parasitic capacitance is unintended capacitance that exists between the conductors of an electronic circuit. This capacitance can cause signal distortion and reduced performance. The effect of parasitic capacitance is most pronounced at high frequencies, making it a major consideration in the design of high-speed circuits. There are several ways to reduce the effects of parasitic capacitance, including reducing the spacing between conductors, and using special materials that have a low dielectric constant.

Parasitic inductance

Parasitic inductance is the unintended inductance that occurs due to the presence of metal interconnects. This inductance can cause problems such as signal delay and distortion, and can also increase power consumption. Parasitic inductance can be minimized by using shorter and thicker interconnects, and by keeping them as close to the ground plane as possible.

Calibre xACT parasitic extraction

The Calibre® xACT™ platform offers engineers powerful electronic design automation (EDA) functionality to help them quickly and accurately analyze EM-induced resistance drops in copper interconnects, and to predict and prevent device failures caused by EM effects. The Calibre xACT tool evaluates the circuit design using rule-based tables and generates a netlist, which is a list of all the electrical components in a circuit. This netlist includes any parasitic resistance and capacitance that is detected, as well as all of the intentional devices, such as MOS transistors. The netlist is then used as input to a simulator, such as the Analog FastSPICE or ELDO™ tools, to

simulate the circuit performance. Designers use these results to determine if the design meets specifications, even with the parasitics. If not, layout engineers must modify the layout to minimize the parasitics, then re-run the entire extraction and simulation flow until the design meets specifications.

When parasitic inductance begins to affect chip behavior, an RCL netlist is used in place of the RC netlist. Parasitic inductance effects occur most often when the chip runs at a high frequency, for example, in 5G designs. Because the Calibre xACT 3D tool contains a capacitance field solver, it can be used in conjunction with the Calibre xACT tool (for resistance) and the Calibre xL tool (for inductance) to generate a highly accurate RCL netlist that includes parasitic inductance. The increased accuracy comes from the use of a field solver vs. a rule based tool.

Power integrity analysis

EM/IR is a problem that impacts all aspects of semiconductor design and manufacturing. EM/IR effects often lead to device failures during operation. Understanding EM/IR and how it impacts the performance of an IC design is critical to layout optimization. Power integrity analysis software performs EM/IR analysis on IC designs to predict power performance and identify EM/IR hotspots in the circuitry.

Calibre xACT and EM/IR tool integration

To ensure accurate analysis results, EM/IR tools require a parasitic extraction tool that can extract a layout netlist in DSPF format of the parasitic network. The Calibre xACT tool generates parasitic netlist data in DSPF format that contains detailed data about the design parasitics. The Calibre xACT platform is tightly integrated with most power integrity analysis tools to provide design companies with confidence in the parasitic data needed for accurate power analysis.

mPower power integrity analysis

The Siemens mPower™ platform enables customers to perform sign-off analysis of IR-drop, power, and EM for both digital and analog IC designs, from block to full-chip level, to ensure that the as-implemented design will meet performance and reliability targets when manufactured.

The mPower platform can take as its input the netlist of leading parasitic extraction tools, including the Calibre xACT tool. It can then use any SPICE simulator that can write a fast signal database (FSDB), and using the post-layout simulation results, display waveform outputs and graphical color maps to help designers pinpoint areas of the layout containing EM/IR issues. With this information, designers can make layout modifications (for example, lower resistance by widening wires, or lower coupling capacitance by moving two wires further apart), then re-run parasitic extraction, simulation, and EM/IR analysis, to see if the problem areas have been resolved.

Conclusion

EM and IR drop are two critical design issues that can affect the performance and reliability of IC designs. Understanding the causes of EM and IR drop, and how to modify designs to minimize their impact, is essential to delivering IC designs whose manufactured performance and product reliability match the design intent. To complete these tasks efficiently, with confidence in the results, design teams need EDA tools that can quickly and accurately perform parasitic extraction and EM/IR analysis to enable them to analyze and optimize their designs to minimize EM and IR drop effects while still meeting tapeout schedules.

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