DIGITAL INDUSTRIES SOFTWARE

S-Edit Schematic Capture

Benefits

- Handles your most complex, full-custom IC designs
- Native on OpenAccess
- Integration with AFS, Eldo and T-Spice simulators, allowing waveform cross-probing and direct viewing of operating point simulation results in the schematic
- Simulation can also be set up, launched and monitored using the Solido Design Environment
- Inherited connections are supported
- Schematic Compare visually displays differences between any two schematic or symbol views

A Complete IC design capture environment

S-Edit is an easy-to-use design environment for schematic capture and design entry. It gives you the power you need to handle your most complex mixed-signal IC design capture. S-Edit is tightly integrated with Analog FastSPICE™ (AFS), Eldo® or T-Spice simulators, Solido Design Environment, the L-Edit IC layout editor and the Calibre® LVS and PEX tools. S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. A faster design cycle gives you more flexibility in moving to an optimal solution, freeing up more time and resources for process corner validation. The results are less risk downstream, higher yield and quicker time-to-market.

Schematic capture for the most complex mixed-signal IC design

- Bus support speeds the creation of mixed-signal designs
- Advanced array support enables easy creation and editing of memory, imaging or circuits with repetitive blocks
- Rubberband connectivity editing with snap to pin (hotspots) enables faster design modifications

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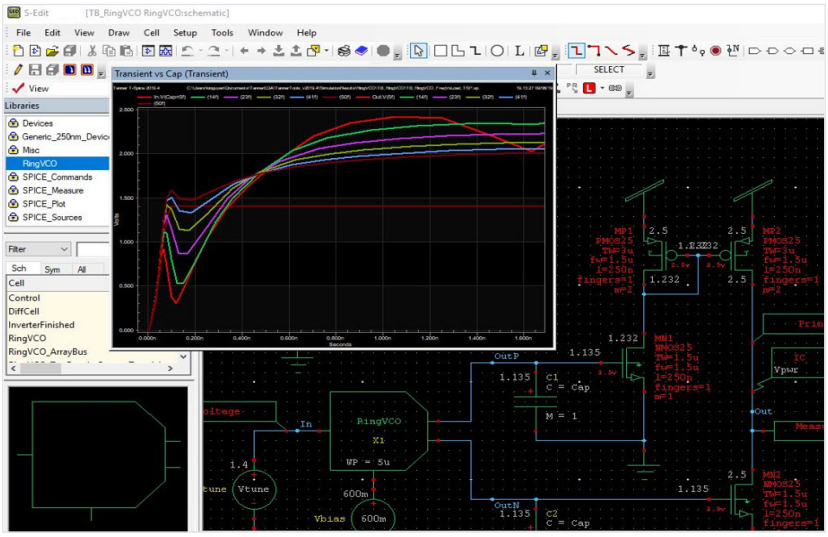
Benefits *continued*

- Cross-probe between schematic, simulation results, layout and Calibre LVS report with net/device highlighting
- Netlist multiple-views per cell including: SPICE, schematic, Verilog, Verilog-A and Verilog-AMS
- Integrated with L-Edit Schematic Driven Layout (SDL) module to speed the layout and ECO process
- Configurable schematic Electrical Rule Checks (ERC)
- Multiple library support with integrated library navigator
- Hierarchy Editor to create and manage configuration views
- Advanced array and bus support
- Integration with third-party revision control tools
- Import and export multiple standard formats



S-Edit schematic capture and simulation cockpit shows schematics, simulation waveforms, model parameters and simulation settings. The tool is easy to use and has the power to handle complex mixed-signal IC design capture.

- S-Edit displays evaluated parameters in real time over the course of the design process; parameters with formulas based on other circuit parameters can be displayed or evaluated
- Using an imported netlist, S-Edit can generate a schematic view of that netlist. All of the connections on the schematic are implicit, with no wires visible. This generated schematic visualization is useful for LVS and simulation
- Auto symbol generation enables you to easily create symbols from schematics and synchronize any changes
- All actions are fully scriptable through the TCL/Tk command language
- Recordable scripts enable you to automate tasks or expand the tool for application-specific needs
- Replayable logs permit recovery if there is an unexpected network or hardware failure
- S-Edit performs net highlighting and keeps the net highlighted as you move through the hierarchy
- Calibre RVE cross-probing between schematic, layout and LVS report to highlight nets or devices
- Schematic ERC enables you to check your design for common errors such as undriven nets, unconnected pins and nets driven by multiple outputs; the design checks are fully configurable, including custom validation scripts

Tight integration with simulation

- Drive the simulator from within the schematic capture environment. This allows for viewing operating point results directly on the schematic, viewing small signal parameter of devices, viewing model parameters, and performing waveform cross-probing to view node voltages and device terminal currents or charges
- S-Edit creates an efficient flow for the iterative loop of design, simulation, analysis and tweaking of circuit parameters. Focus on the design and not on data processing, thereby speeding up the design process
- Easy interoperability with third-party tools and legacy data
- S-Edit reads in native OpenAccess or EDIF from third-party tools, with automatic conversion of schematics and properties for seamless integration of legacy data
- Netlists can be exported in flexible, user-configurable formats, including Spectre, SPICE and CDL variants, EDIF, structural Verilog and structural VHDL
- Library support in S-Edit maximizes the reuse of IP developed in previous projects, or imported from third-party vendors

Powerful and easy-to-use interface

- S-Edit makes front-end design capture easier and more productive
- A fully user-programmable design environment allows you to remap hotkeys, create new toolbars and customize the view to your preference – all in a streamlined GUI
- The complete user interface is available in multiple languages, including English, Japanese, and Simplified and Traditional Chinese
- S-Edit provides Unicode support; all user data can be entered in international character sets
- Cost-effective
- S-Edit provides an ideal performance-to-cost ratio, allowing you to maximize the number of designers on a project
- Since S-Edit runs on Windows® and Linux platforms, designers can work on cost-effective workstations or laptops; this means you can take your work with you anywhere, even home and continue working to meet time-to-market pressures
- Available in two configurations: full schematic editor and schematic viewer

Siemens Digital Industries Software

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For additional numbers, click here.

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