

DIGITAL INDUSTRIES SOFTWARE

STMicroelectronics: IP validation and analysis with Solido Crosscheck and Solido Analytics

Solido methodology helps STMicroelectronics ensure IP release quality and improve QA efficiency

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Introduction

Modern system-on-chip (SoC) designs benefit from the integration of design IP as a method of modularizing design workflows, leveraging re-usability of components, and improving design quality as well as time-to-market. IP production teams provide standard cells, I/Os, and many other types of digital and analog IP, including interface blocks, power management units, data conversion IP, etc., to be integrated at the chip-level or higher block levels.

For all of these IP types, effective validation that anticipates SoC integration challenges is important to ensure the final design meets power, performance and area metrics while staying within production schedules and budgets. A strong IP QA methodology achieves this by detecting issues early and improving the quality of the IP used.

Challenges in IP production and validation

Due to the growing complexity of IP, production and validation teams face several new challenges during the IP release cycle. These challenges include:

Handling multiple design views

One reason why IP view generation requires a proper QA methodology is the multitude of views and formats used in the IP production and SoC design process.

STMicroelectronics' IP view generation process includes the production of multiple design views, such as functional, electrical, physical, test and other models. The input data required for view generation may originate from different sources.

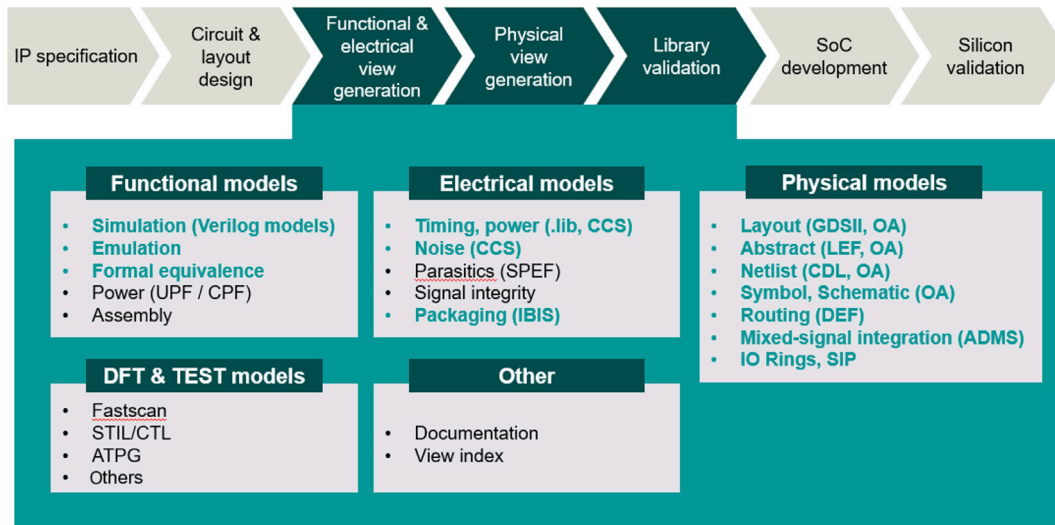


Figure 1: Design views used in the IP production and integration flow.

Different design views are often produced from different tools or processes and contain different information that is equally crucial for a successful SoC design tape-out. For example:

- SPICE netlists are produced from circuit design and written out from schematic editor tools. Information stored here includes device netlist interconnectivity and transistor types/sizes.
- LEF abstract views are created by extracting information from GDS2 layout of IPs. They are created and written out from layout editors. These views provide physical layout information (i.e., metal interconnect, blockages, pin locations and other information).
- Liberty (.lib) models, including CCS and Liberty Variation Format (LVF), are produced from the characterization process using SPICE netlists and other inputs. The resulting .lib models are used by static timing analysis (STA) tools to measure timing, power, noise and variation at a digital SoC level.

As shown in figure 1, a successful IP production and integration flow requires all inter-related views to be correct and contain consistent information. Inconsistencies between views and formats must be identified and resolved during the IP release process; otherwise, SoC development schedules and quality of results will be at risk.

Increasing size and complexity of IP data

Production processes and IP data have steadily increased in size and complexity. For example, due to increasing requirements for accuracy, .lib characterization methodologies today consider many more factors and are run on more process, voltage and temperature (PVT) corners than ever before. The result is libraries with tens or hundreds of gigabytes of data, including timing, power, noise and statistical modeling information.

Larger data sets and more complex production processes increase the risk of incorrect or inaccurate IP data. For .libs, SPICE input, circuit issues, or incorrect characterization settings are just a few of the factors that can lead to incorrect results, such as unexpected zero value results, “noisy” data, or per-PVT .libs that have systemic outliers when compared to other PVTs.

Non-uniformity among production environment components

One of the challenges IP release teams face in their day-to-day operations is non-uniformity among different components. Different IPs, technology process nodes, foundry design kits (PDKs) and design methodologies each introduce additional compatibility layers or corner cases that need to be handled correctly.

IP qualification or validation tools must be robust enough to handle most, if not all, of these differences. However, new design requirements and increased specialization such as new categories of IP, or divergences in process technology for different applications, continuously drive the need for more flexibility at the IP design stage. Because of this, IP QA flows must keep up with frequently evolving input specifications.

STMicroelectronics' requirements for an effective, comprehensive IP QA methodology

To be an effective solution, an IP QA framework must deliver on multiple metrics, including: breadth and depth of validation coverage to meet validation requirements, usability of the solution and effectiveness of analysis/debugging, and finally, extensibility and the ability to integrate into larger production and validation systems, if needed.

In addition, to sign off an IP release as production-ready, STMicroelectronics' IP team requires an IP

QA flow that can detect consistency issues between views (i.e., inconsistencies between LEF versus .lib views), as well as perform view modeling checks, IP integrity checks, and package checks.

Furthermore, for .libs, due to the complexity in .lib data structures and volume of data, the IP QA methodology needs to be able to automatically check for outliers and potential systemic issues, such as issues that affect an entire PVT .lib.

STMicroelectronics' IP and library view validation methodology with Solido

The Solido software tools used in STMicroelectronics' IP QA flow include Solido Crosscheck and Solido Analytics.

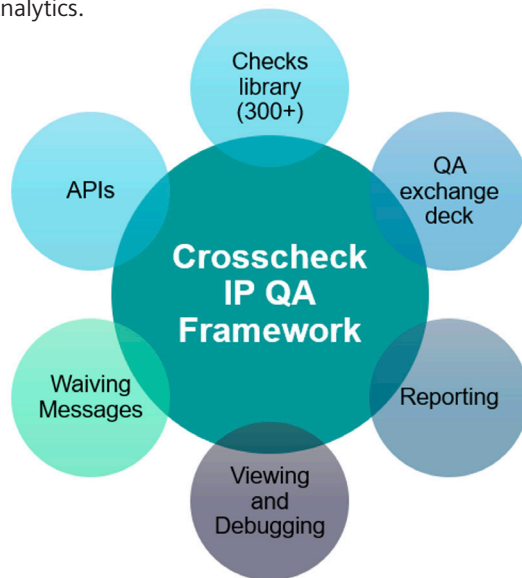


Figure 2: Solido Crosscheck IP QA framework.

Solido Crosscheck is used for broad design view QA coverage across all formats and views, including functional, electrical, physical, test views and others.

For advanced .lib verification and analysis, STMicroelectronics uses Solido Analytics, which provides an additional layer of machine learning-enabled sign-off verification, as well as analysis and insight into .lib data.

Solido Crosscheck: IP QA framework with broad design view coverage

Solido Crosscheck provides IP validation covering many design views and formats, including functional, electrical/timing, physical and other views.

Solido Crosscheck includes a complete IP validation framework around its validation checks. This includes a reporting system, ability to view and debug errors or violations, and validation results classified into pass/fail/wave categories.

Breadth of coverage: Ensuring all target IP, technology, views, checks and usage models can be validated

STMicroelectronics utilized Solido Crosscheck to validate a broad range of IPs across multiple

process technology nodes from 40nm to 16nm. Figure 3 shows a sample of the design views and formats validated by Solido Crosscheck in STMicroelectronics’ IP QA flow:

Design types validated: I/O cells, Analog Macros, Flash, RF IP, SERDES/PHY, Voltage Regulators, etc.			
Functional models <ul style="list-style-type: none"> Simulation (Verilog) Emulation Formal equivalence Power (UPF / CPF) Assembly 	Electrical models <ul style="list-style-type: none"> Timing (.lib, CCS) Power (.lib, CCS) Noise (CCS) Parasitics (SPEF) Signal integrity Packaging (IBIS) 	Physical models <ul style="list-style-type: none"> Layout (GDSII, OA) Abstract (LEF, OA) Netlist (CDL, OA) Symbol, Schematic (OA) Routing (DEF) Mixed-signal integration (ADMS) IO Rings, SIP 	DFT and test models <ul style="list-style-type: none"> Fastscan STIL/CTL ATPG

Figure 3: Design types and views validated by Solido Crosscheck.

Usability: Reducing engineering time and effort, as well as shorten IP validation cycles

A key metric to the effectiveness of the tool was the ease-of-use and practical utility that would help shorten IP validation schedules. Solido Crosscheck

provides a dashboard to summarize and classify validation results into pass/fail/waive categories, providing users the ability to quickly evaluate whether IP was “golden” and ready to release, or if more work was required.

Check name	Description	Duration	waive	setup_warning	warning	error	fatal
61.Liberty-Arcs-power	Liberty Timing arcs check (rule: 61)	2.394 sec	0	0	0	0	0
61.Liberty-Arcs-timing	Liberty Timing arcs check (rule: 61)	0.319 sec	0	0	0	0	0
67	Liberty vs Verilog or VHDL timing arc check with SDF back-annotation (rule: 67)	0.065 sec	0	0	0	0	0
711	NLDM delay tables accompanied by NLDM transition tables (rule: 711)	11.256 sec	0	0	0	0	0
712	Ascending capacitance and transition index values (rule: 712)	13.257 sec	0	0	0	0	0
714	Transition indices are identical for all tables of a single cell (rule: 714)	13.247 sec	0	0	0	448	0
715	Check number of indices (rule: 715)	13.471 sec	0	0	0	0	0
7201	Range check for cell_rise and cell_fall delay values (rule: 7201)	13.244 sec	0	0	0	0	0
7202	Range check for rise_transition and fall_transition values (rule: 7202)	12.580 sec	0	0	0	0	0
7203	Checks whether delay values rise or fall proportionally (rule: 7203)	12.350 sec	0	0	0	138	0
7204	Compare rise and fall values within a cell (rule: 7204)	17.114 sec	0	0	0	0	0
7205	Checks whether delay values for the same arcs but different conditions do not vary too much (rule: 7205)	12.998 sec	0	0	0	0	0
7206	Range check on setup and hold values (rule: 7206)	13.161 sec	0	0	0	0	0
7207	Range check on min_pulse_width values (rule: 7207)	13.227 sec	0	0	0	0	0
7208	Range check on min_period values (rule: 7208)	12.997 sec	0	0	0	0	0
7209	Delays increase with increasing output capacitance (rule: 7209)	13.533 sec	0	0	448	0	0
7210	Delays increase with increasing input transition times (rule: 7210)	12.431 sec	0	0	0	0	0
7211	Setup and hold tables are defined in matching pairs (rule: 7211)	12.324 sec	0	0	0	0	0
7212	Matching setup and hold tables have equal indices (rule: 7212)	14.154 sec	0	0	0	0	0
7213	Sum of setup and hold values must be larger than 0 (rule: 7213)	13.495 sec	0	0	0	0	0
7215	Check for non changing delay or transition values (rule: 7215)	15.541 sec	0	0	0	40	0
7217	Checks for any zero value in any table (rule: 7217)	14.316 sec	0	0	0	503	0
7306.Delays-increase-with-decreasing-supply-voltage_voltageLiberty12	Delays increase with decreasing supply-voltage (rule: 7306)	5.757 sec	0	0	0	8	0
7306.Delays-increase-with-decreasing-supply-voltage_voltageLiberty15	Delays increase with decreasing supply-voltage (rule: 7306)	5.774 sec	0	0	0	10	0
7306.Delays-increase-with-decreasing-supply-voltage_voltageLiberty18	Delays increase with decreasing supply-voltage (rule: 7306)	5.779 sec	0	0	0	8	0

Figure 4: Solido Crosscheck built-in HTML reporting.

Extensibility and integration into STMicroelectronics’ IP production and validation flow

A key requirement of a QA framework is the extensibility of the tool to cover custom use cases, provide custom functionality to interact with, or even be integrated, as part of a larger QA solution.

Solido Crosscheck provides extensibility with APIs that enable reading in custom formats, performs custom checks, and writes out custom reports.

STMicroelectronics developed infrastructure around Solido Crosscheck using these APIs so that user intervention for configuration and setting parameters for checks could be minimized by reading metadata from IP views, and using that information to handle different technology data.

Solido Analytics: Machine learning-enabled .lib verification and analysis

Solido Analytics is a Liberty model (.lib) verification and analysis tool. Aside from rule-based methods, Solido Analytics also provides an additional layer of validation by using machine learning (ML) to automatically detect outliers and other issues in .lib data. Solido Analytics also includes a library visualizer that enables users to plot, analyze and debug .lib data. By plotting table data

across different PVTs, the tool can help users understand how their Liberty models behave across different PVT corners.

Machine learning-enabled validation, analysis and debugging for .libs

STMicroelectronics uses Solido Analytics to identify outliers across table data and different PVT corners. One of the main applications of this tool was for characterization or .lib verification teams to check for unexpected outliers caused either by design or characterization settings. In many cases, after detecting an issue the characterization or .lib verification team needed to analyze the .lib data further to trace the issue back to the root cause and determine what to fix.

For this use case, the machine learning engine in Solido Analytics identified .lib errors by comparing actual .lib data with expected values obtained from an ML model of the .lib, and provided the visualization required for analysis.

The following example illustrates this use case. Typically, we would expect cell fall time to decrease as operating voltage increases. In this case, Solido Analytics detected an incorrect trend where cell fall times increased as operating voltage increased past 0.95V (figure 6).

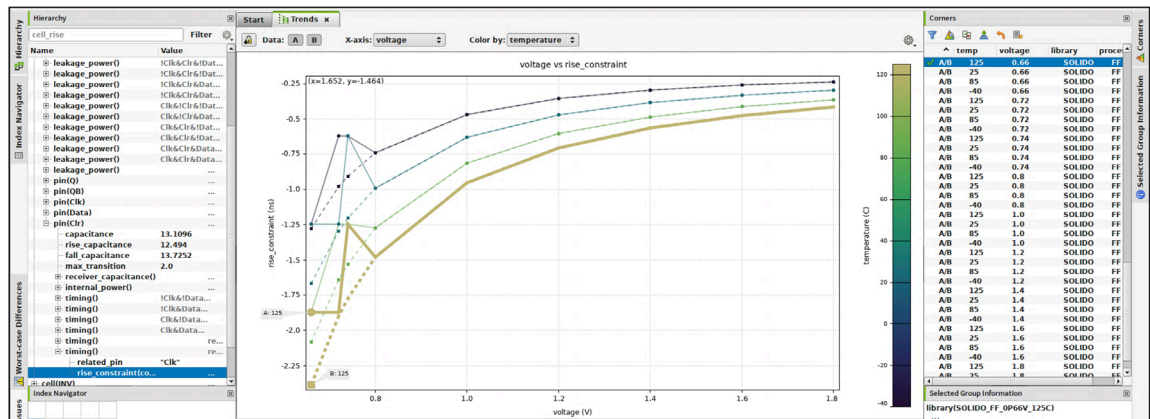


Figure 5: Solido Analytics machine learning outlier detection and .lib visualization.

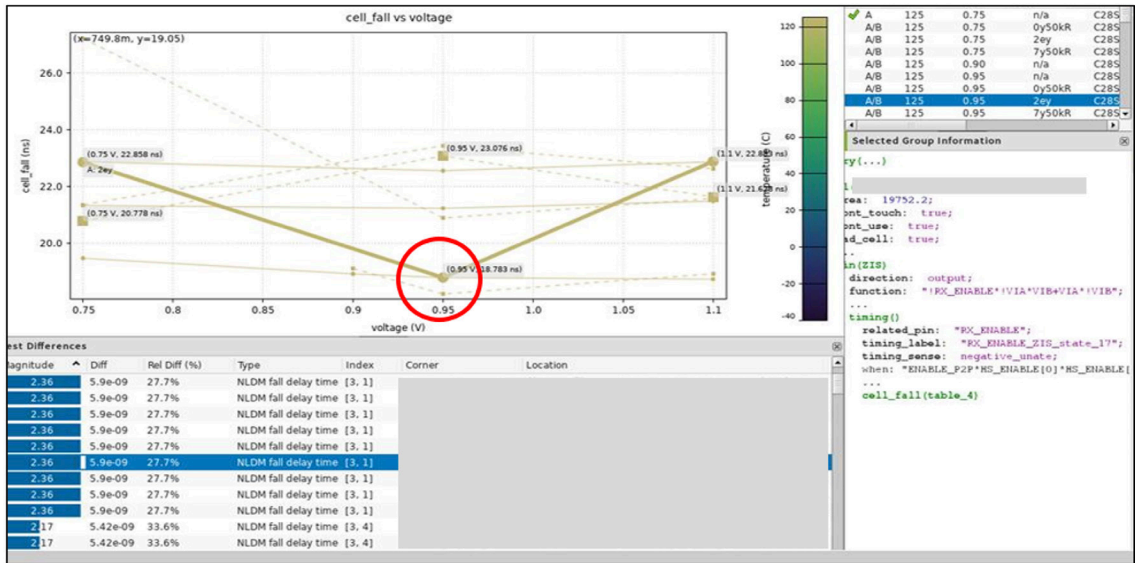


Figure 6: Cell fall outlier identified by Solido Analytics.

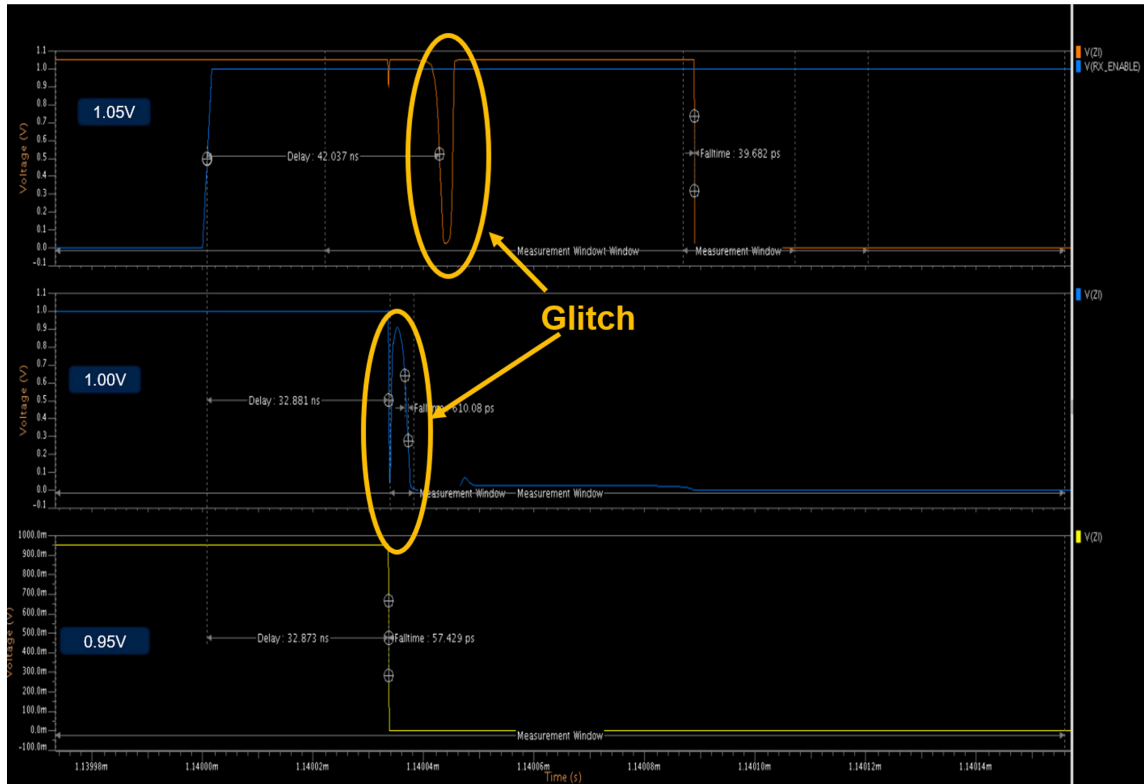


Figure 7: Incorrect circuit behavior detected by Solido Analytics is confirmed by a waveform viewer.

Further investigation with a waveform viewer (outside of Solido Analytics) confirmed that SPICE-simulated cell behavior shows glitches occurring at operating voltages 1.0V and above. Therefore, in this case, characterization results correctly reflected a problem with the circuit, which was identified by Solido Analytics.

The example above shows a case where the identified issue was traced back to a circuit issue, which was fixed.

The machine learning outlier detection in Solido Analytics also identified cases where .lib issues were caused by incorrect characterization setup, or issues with inputs during alternate .lib creation methods. Examples include:

1. Analog block characterization: An electronic circuit called the “compensation block” provides a digital compensating code to the target I/O driver to slow down output signals during “best case” conditions and speed up output signals during “worst case” conditions (thereby “compensating” the output signal speed based on best-case/worst-case conditions). If the digital compensating code is incorrectly applied during characterization, this will result in incorrect characterization results, which were caught by Solido Analytics.

2. Digital block characterization: Some digital block characterization is done with STA tools, using a gate-level netlist, SPEF for resistance and capacitance (RC) parasitics, and standard cell library information for internal components of the block. In this case, Solido Analytics detected digital block characterization errors caused by incorrect or missing SPEF information.

3. Semi-automated appending of .lib data: In some cases, .libs are appended with additional data using scripted methods, such as leakage table value insertion with data translated from other tools or sources. In this case, Solido Analytics identified cases where appended leakage numbers were impacted by incorrect inputs or translation.

The three previous examples show how machine learning is used to detect issues that are not easily identifiable by other methods.

| Summary

With an IP QA framework that utilizes Solido Crosscheck and Solido Analytics, STMicroelectronics can:

- Improve schedule time and release quality of IP with a fully integrated QA solution customizable for the user’s needs using built-in functionality and API extensions.
- Focus on product design and CAD strengths while leveraging industry experience from a commercial EDA tool provider for software and checks.
- Benchmark and compare the team’s own IP validation with industry standards. Built-in checks and recommended settings provide insight into industry-wide IP validation care-about, and proactively identify any “blind spots” in the team’s IP validation process.

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