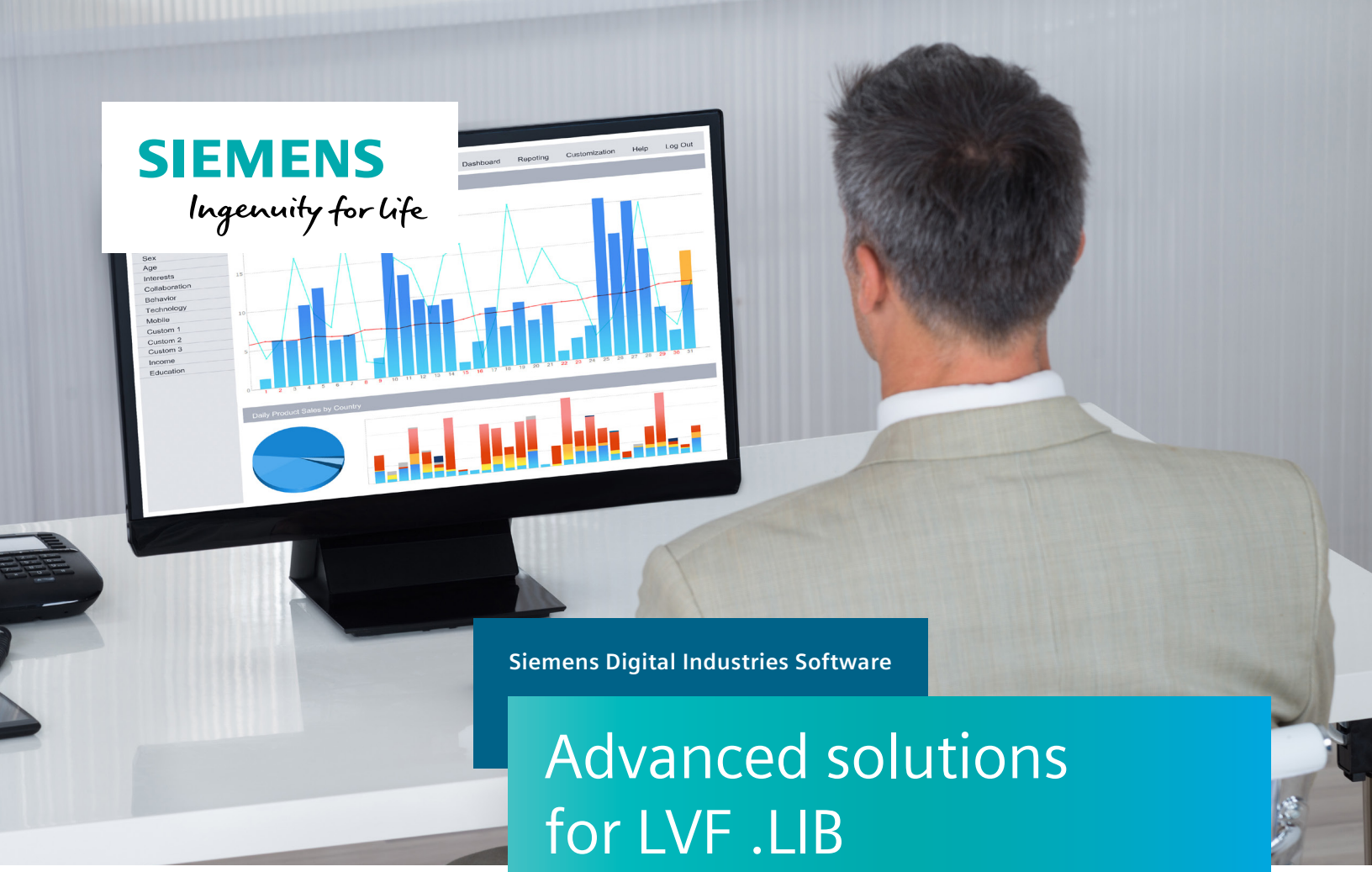

Siemens Digital Industries Software

Advanced solutions for LVF .LIB

Variation modelling using LVF allows chip designers to encapsulate statistical variation data to supplement nominal timing values, and is required for advanced process nodes 22nm and below. Many approximations are used during the characterization process for LVF data, due to long runtimes required to run Monte Carlo analysis. This leads to incorrect/inaccurate LVF data that may lead to timing closure issues and silicon failure. Therefore, LVF validation is a crucial step in design flows that use LVF.

Siemens Digital Industries Software Solido products provide comprehensive, closed-loop verification for LVF data. Solido Analytics uses machine learning to automatically identify outliers and potential issues across the entire data set. Then, Solido Variation Designer runs full Monte Carlo-equivalent deep analysis and re-validation on problem areas identified by Analytics, identifying the correct sigma and moments values for those data points.

Wei-Lii Tan and Jeff Dyck

Introduction

On-chip variation (OCV) is a significant factor affecting timing sign-off for digital designs at 20nm and below. At 7nm, timing measurements such as propagation delay, setup time, and hold time may change by 50%-100% due to statistical variation. In order to capture these variation effects accurately, timing .libs for 20nm and smaller process nodes include variation modeling information defined by the Liberty® Variation Format (LVF).

LVF requires that each timing data point must also perform a Monte Carlo analysis in order to capture the full distribution of behavior. Since each brute-force Monte Carlo analysis requires thousands of additional simulations (across all timing measurements defined in the .libs), characterization tools use various methods to make runtime feasible. These methods introduce approximations and inaccuracies that may invalidate library timing data, resulting in chip tapeout delays or silicon failure. Therefore, verifying LVF data is a critical step for chip tapeout success.

Solido provides a sign-off solution for verifying LVF data in .libs using advanced Machine Learning (ML)-enabled technology. Using Solido's Analytics and Variation Designer tools results in a workflow that correctly and automatically identifies all LVF problem areas, and accurately re-simulates any points that do not meet production targets. The end result is sign-off verified LVF .libs that can be confidently used in production.

On-chip variation and liberty variation format

Liberty Variation Format (LVF) is the leading format that models on-chip variation (OCV) for libraries at 22/20nm and smaller process technology nodes. Before going into the details of LVF, let's recap what OCV is, and why LVF is important in design flows at 22/20nm and smaller.

On-chip variation (OCV)

OCV refers to localized differences in semiconductor and interconnect behavior within the same chip, due to factors such as transistor properties or manufacturing irregularities. Since there is no feasible way to model these effects deterministically today, OCV effects are either modelled as global derate factors for larger process nodes, or statistically modelled as sigma values for smaller process nodes, and are stored in timing .libs. These adjustments are used by static timing analysis (STA) tools to add pessimism to chip-level timing.

On-chip variation modeling methods

Global derate OCV factors

For 90nm and larger process nodes, it may be adequate to model OCV as global derating factors for each PVT .lib. A global derating factor is applied on all timing paths in the design. Among other options, the user can define different global derating factors for rise and fall timing measurements, and specify whether the derating factor applies to cells, interconnect or both.

Advanced OCV (AOCV)

For process nodes from 65nm and below (to about 22nm), there is an increasing impact of OCV on timing and power, making it no longer feasible to model OCV as global derating factors while achieving design closure for power, performance and area metrics. A single derating factor applied uniformly across all nets and cell instances is too pessimistic, since it is unrealistic to assume all instances in a logic path will be affected by the maximum variation.

AOCV provides different OCV derating factors based on logic stage, instead of a single derating factor. The derating factor for instances/nets at later logic stages are reduced compared to the initial stages. This is why AOCV is also called SBOCV, short for "stage-based OCV".

Some AOCV implementations take into account physical distance of cell instances. In this case, the derating factor used is chosen based on distance between cell instances, or from a 2D table with both logic stage and distance as the table indices.

Liberty variation format (LVF)

LVF extends the Liberty format to add statistical variation to timing information. Compared to using global OCV derate factors or AOCV, LVF provides the most granularity and accuracy for modeling statistical variation in timing libraries. Today, LVF is the leading standard for modeling variation for timing libraries at 22/20nm and smaller process nodes.

Nominal timing libraries contain numerous lookup tables that include timing information such as cell delays, transition times, and setup and hold constraints for all cells in the library. LVF extends that information with additional tables for early and late statistical variation (sigma) values of each measurement.

With LVF, the STA tool obtains sigma information per timing arc and per slew-load combination, for each cell in the library. This level of granularity is required for 22/20nm libraries and smaller, due to the large impact of variation on timing measurements. For example, at 7nm and 5nm, timing attributes such as delays, transition times and constraints may change by up to 50%-100% of the nominal timing, due to OCV.

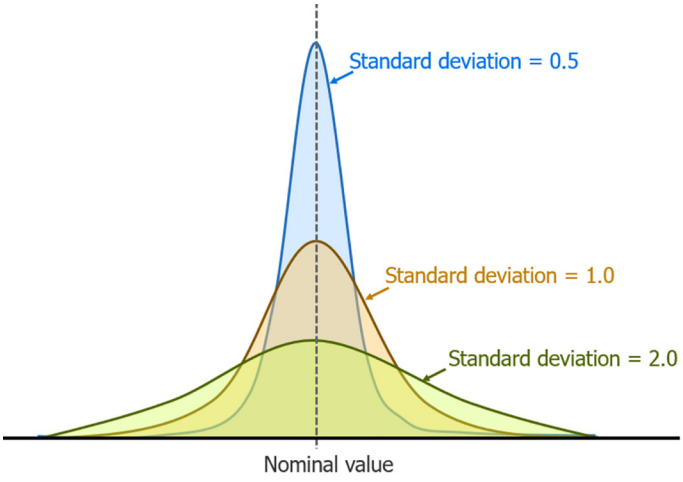

Figure 1: LVF .libs with Moments contain the standard deviation values for each measured entry.

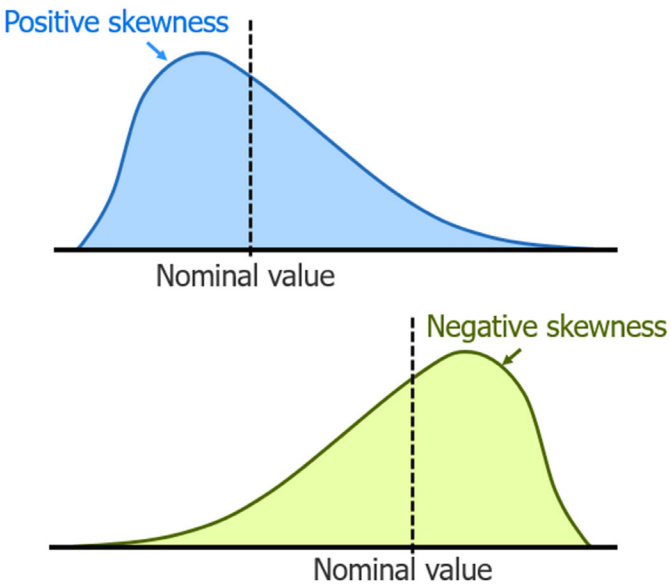

Figure 2: LVF .libs with Moments also include higher-order statistical moments (e.g., skewness) for each measured entry.

In addition to sigma values, the LVF syntax also includes support for moments (figure 1), which contain additional information about the statistical distribution, including the difference between nominal and the mean (mean shift), the standard deviation, and the skewness (figure 2).

How LVF information is used for static timing analysis

During static timing analysis (STA) of digital designs, the timing tool uses sigma values in the LVF .libs to add pessimism to the timing path. LVF .libs include several different sigma tables that describe variation for timing properties such as for transition time, delays, and constraints (for sequential cells). The sigma values in these tables are obtained through Monte Carlo, or Monte Carlo-equivalent analysis, and are described at the cell timing arclevel. During STA, the timing tool will interpret these per-instance timing arc variations from the LVF .libs, to determine the 3-sigma variation delays and constraints at the timing path level. An example is shown in figure 3.

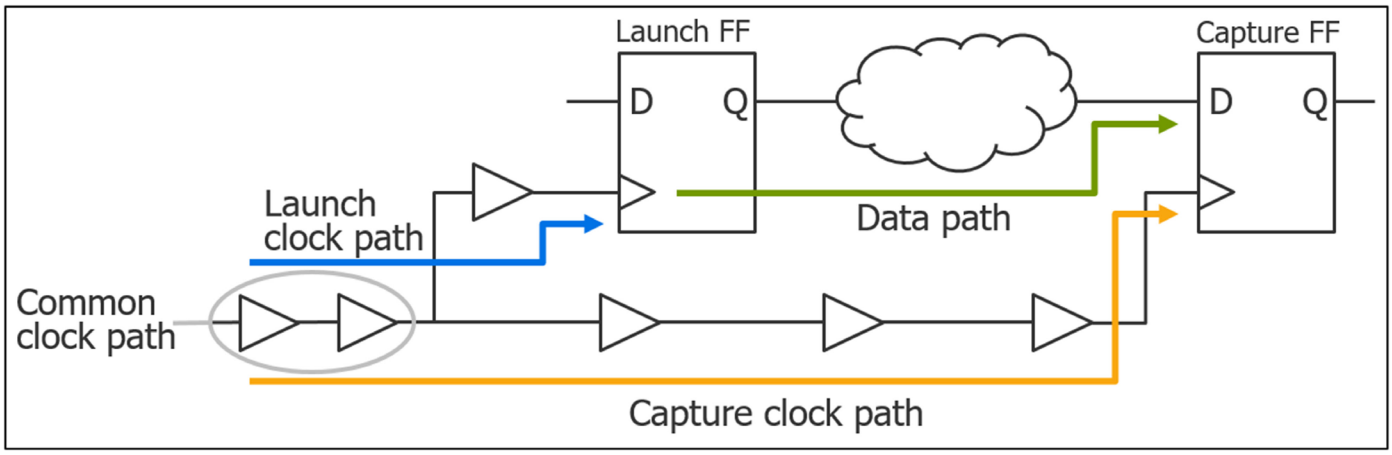

Figure 3: Simple logic timing path.

The diagram illustrates a simple timing path, consisting of two registers (flip-flops) with combinational logic in between. In this example, both registers use branches from the same clock tree.

During setup timing mode in STA, late LVF sigma values are applied to the launch clock path and the data path, to model the data arriving at the capture flip-flop later than the mean arrival time. At the same time, early LVF sigma values are applied to the capture clock path, to model the capture clock edge arriving earlier than the mean arrival time. In addition, a constraints sigma value is applied to the capture flip-flop to model a more pessimistic setup time requirement.

For hold timing mode, the early/late conditions are reversed (i.e, using early LVF sigma values for launch clock and data path, and late LVF sigma values for capture clock path). STA accuracy for hold timing is especially important, since a digital IC/SoC that does not meet setup timing can still run with a lower clock frequency, but one that does not meet hold timing has no such remedy.

This additional modeling of the launch clock path, capture clock path, and data path results in a sufficiently accurate representation of added pessimism to the timing of the path, based on statistical values characterized in the LVF timing .libs. However, since all the sigma values mentioned above come from LVF .lib tables, the viability of this model is entirely dependent on the accuracy and correctness of LVF .lib table data.

Challenges to LVF characterization

The additional information contained in LVF .libs is useful for modeling cell-level timing and power variation at a very granular level. However, it also presents unique challenges for characterization.

We can take a 12x12 cell_rise delay table (12 input slews and 12 output delays as table indices) that describes propagation delay for rising output timing arc as an example. In this example, we would need 12x12=144 values obtained via SPICE simulation, to characterize nominal values for all data points in the table. However, in order to obtain 3-sigma values for the OCV_sigma_cell_rise table that describes delay variation for that same timing arc, thousands of brute-force Monte Carlo simulations would be required for each of the values in the table. In practice, this is not feasible because the run-time would increase by at least 1000X.

Instead, today's library characterization tools utilize a number of methods to reduce the amount of simulations needed to characterize LVF data. Some examples of simplifications used to reduce runtime include sensitivitybased approximations and netlist reduction.

These runtime reduction methods may introduce inaccuracies that impact characterization results. Although some methods are less risky than others, these methods all add uncertainty to the accuracy of characterized .libs, which means proper verification of the resulting LVF data is a critical factor to ensure a successful chip tape-out using these timing libraries.

LVF verification challenges

As mentioned earlier, LVF sigma values may impact final timing and power numbers by as much as 50%-100% for 7nm and smaller process node libraries. This means inaccurate LVF data will invalidate accurate nominal data if it is not caught and fixed.

Unfortunately, issues in LVF data such as "noisy" data and outliers are a common occurrence (figure 4). This puts many smaller process node designs at risk of inaccurate STA, which may lead to design tapeout delays, or in more severe cases, chip failure and re-spins.

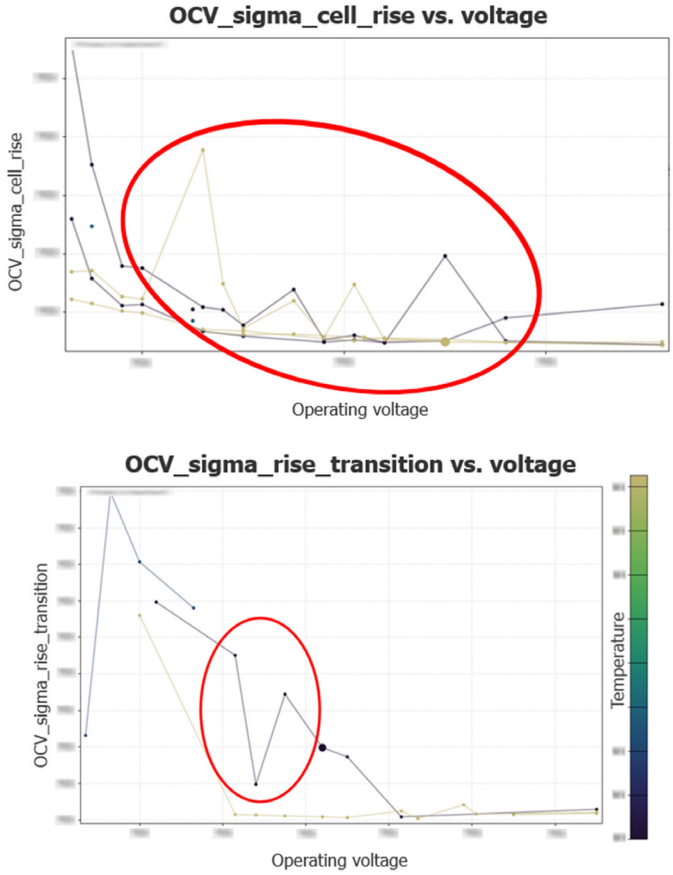

Figure 4: Example issues in LVF sigma results for rise delay and rise transition.

Moments data in LVF .libs are also susceptible to characterized inaccuracies, as shown in figure 5.

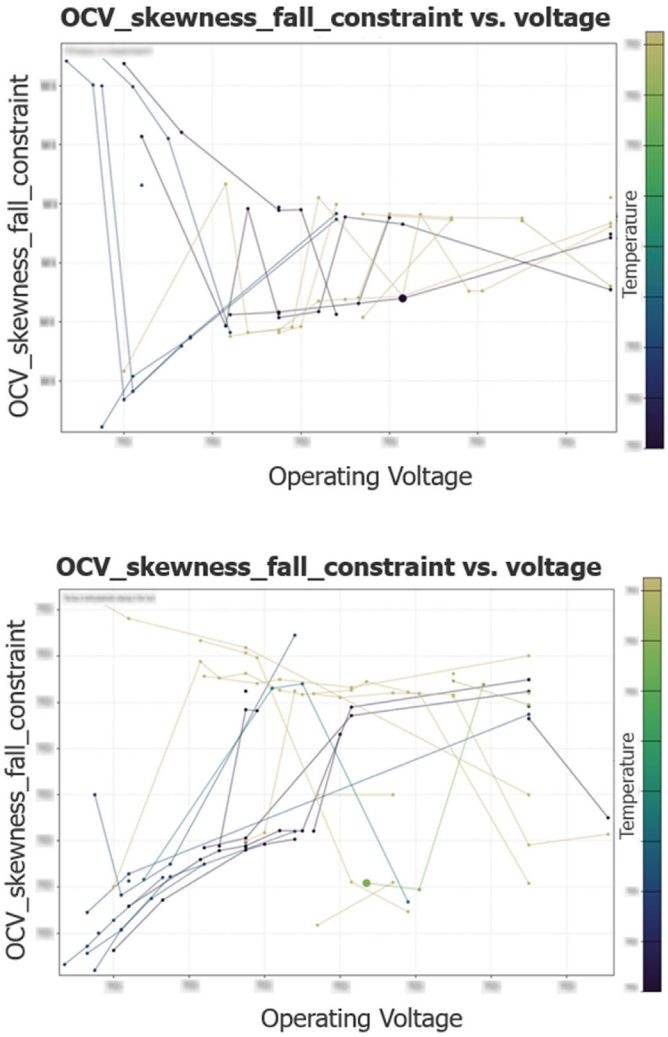

Figure 5: Example issues in LVF moments results for fall constraints.

Another common source of inaccuracy in LVF data is differences between brute-force Monte Carlo simulations and approximated Monte Carlo simulations for the long-tail of distributions (Figure 6). LVF data is typically measured at 3 sigma (3σ). For long-tail distributions, even with a brute-force Monte Carlo approach, there is a larger difference in output value (e.g., variation of delays and constraints) for a given sigma difference. Therefore, any inaccuracy added by approximation during characterization would amplify these differences in output value, resulting in much more inaccuracy in the resulting LVF data.

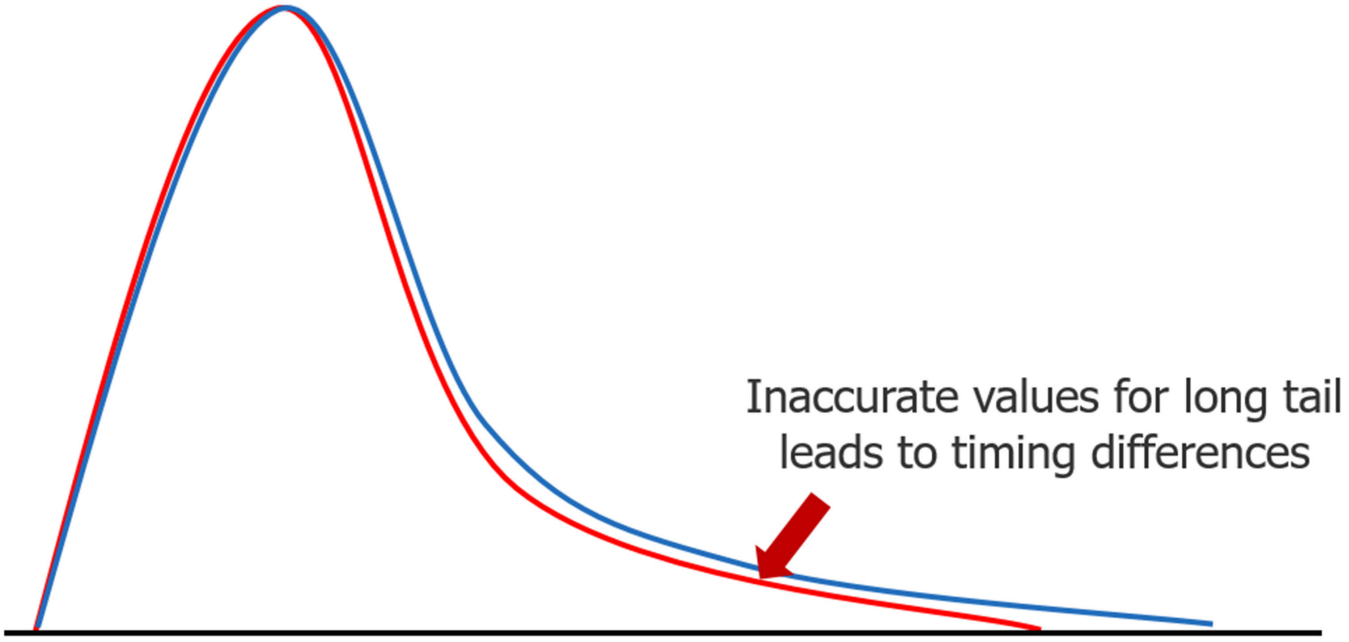

Figure 6: Inaccuracies in long tail values used for LVF data can lead to timing differences and potential silicon failure.

Given these examples, it is clear that a reliable method for identifying LVF data issues is a critical step in any design flow that uses LVF data. However, actually implementing a reliable method for verifying LVF data is almost impossible without the right tools.

The main challenges associated with LVF .lib verification are: Identifying problematic data in a "sea" of hundreds of millions of values, and knowing what the correct value is.

Scale and reliability

LVF data is not just a single additional table per timing arc. For each timing arc and nominal measurement (e.g. propagation delay), there are up to 5 additional measurements used for statistical analysis (early and late 3-sigma values, mean shift, standard deviation, and skewness). In order to achieve the accuracy and granularity required for smaller process nodes, a significant amount of additional characterized data has to be produced and verified.

For modern libraries that consist of 1000+ cells and 100+ PVT corners, the task of LVF data verification spans across hundreds of millions of values and gigabytes of additional data, and requires correct handling of many (and often unpredictable) ways that the characterized LVF data may fail to meet accuracy standards. This means that a user cannot visually inspect the data to make sure the LVF data is valid. A reliable, automated method is required.

Knowing the correct LVF value

On the surface, finding the "correct" LVF value seems straightforward: running brute-force Monte Carlo analysis yields the golden result for comparison. However, since 3-sigma values are used for LVF, thousands of brute-force Monte Carlo SPICE simulations are required to produce each table value. Given the large number of LVF results to verify, running brute-force Monte Carlo to produce the golden reference value is not a feasible solution.

Brute-force Monte Carlo is still sometimes used to produce golden values, but only for a small number of randomly selected LVF data points. The "spot-check" coverage achievable with this method falls short, by a large margin, to be sufficient for a reliable LVF verification methodology.

Solido analytics and solido variation designer: sign-off verification for LVF .Libs using machine learning

Given the requirements stated above, an effective verification flow for LVF data has to include full coverage of the LVF results, i.e., be able to identify problem areas across the entire dataset, as well as the ability to obtain the correct variation modeling value for all problem areas, within feasible runtimes. Siemens Digital Industries Software Solido products achieve this with Solido Analytics and Variation Designer.

Solido analytics

Solido Analytics is a timing library signoff verification tool. It uses a comprehensive set of built-in or user-defined rules, as well as machine learning to automatically identify all issues and outliers in the library. Analytics comes with a library visualizer GUI that helps users explore and debug timing libraries quickly, and produces automated QA reports (figure 7). This helps library teams ensure correctness and accuracy of their .libs, and helps digital teams save valuable engineering time on timing closure iterations.

For variation modeling, Analytics performs a full-coverage check for potential issues using rule-based checks and machine learning-enabled analysis in LVF data including moments. Rule-based checks can identify LVF .lib structural issues such as non-matching table indices compared to nominal data, missing cells or timing arcs across different PVTs, negative sigma values, and other potential issues. More importantly, machine-learning analysis will check for issues in the .lib content data, such as incorrect or inaccurate LVF sigma values, standard deviation, or skewness values. These checks are done automatically, and run in batch mode. The results are collected and summarized for the user in easy-to-read PDF reports and text-based summaries.

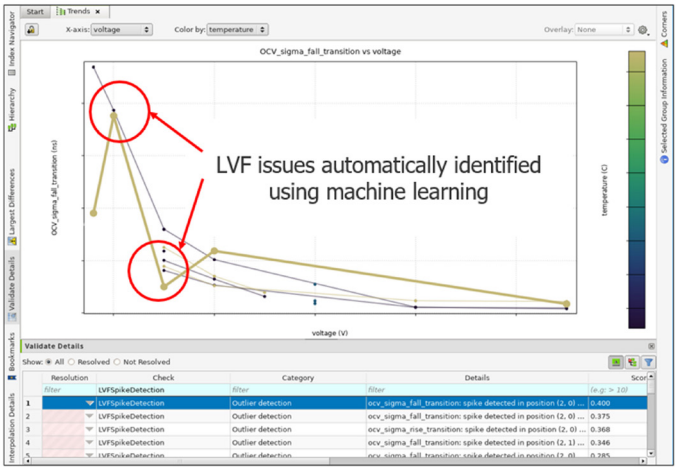

Figure 7: Automatic identification of LVF issue “hotspots” using machine learning in Solido Analytics.

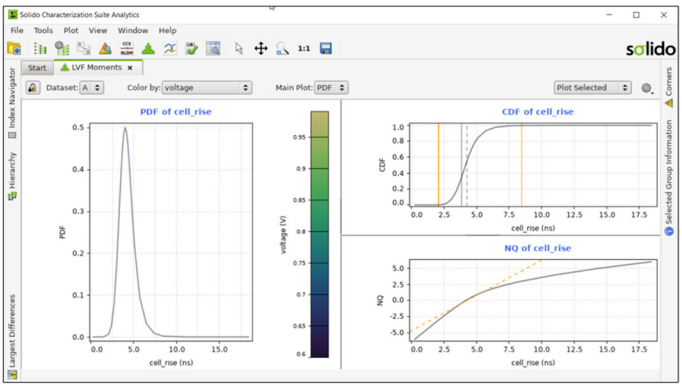

Figure 8: LVF moments data plotting and analysis in Solido Analytics.

In addition to automatic error identification and analysis methods, Analytics also includes a powerful library visualizer GUI (figure 8) that can show any plot-able result to the user. LVF data, especially moments, can be difficult to analyze without the correct tools. With Analytics’ library visualizer GUI, users can readily visualize LVF-related information such as probability density function plots and normal quantile plots. This provides users a muchneeded way to understand the data they have in LVF and moments tables.

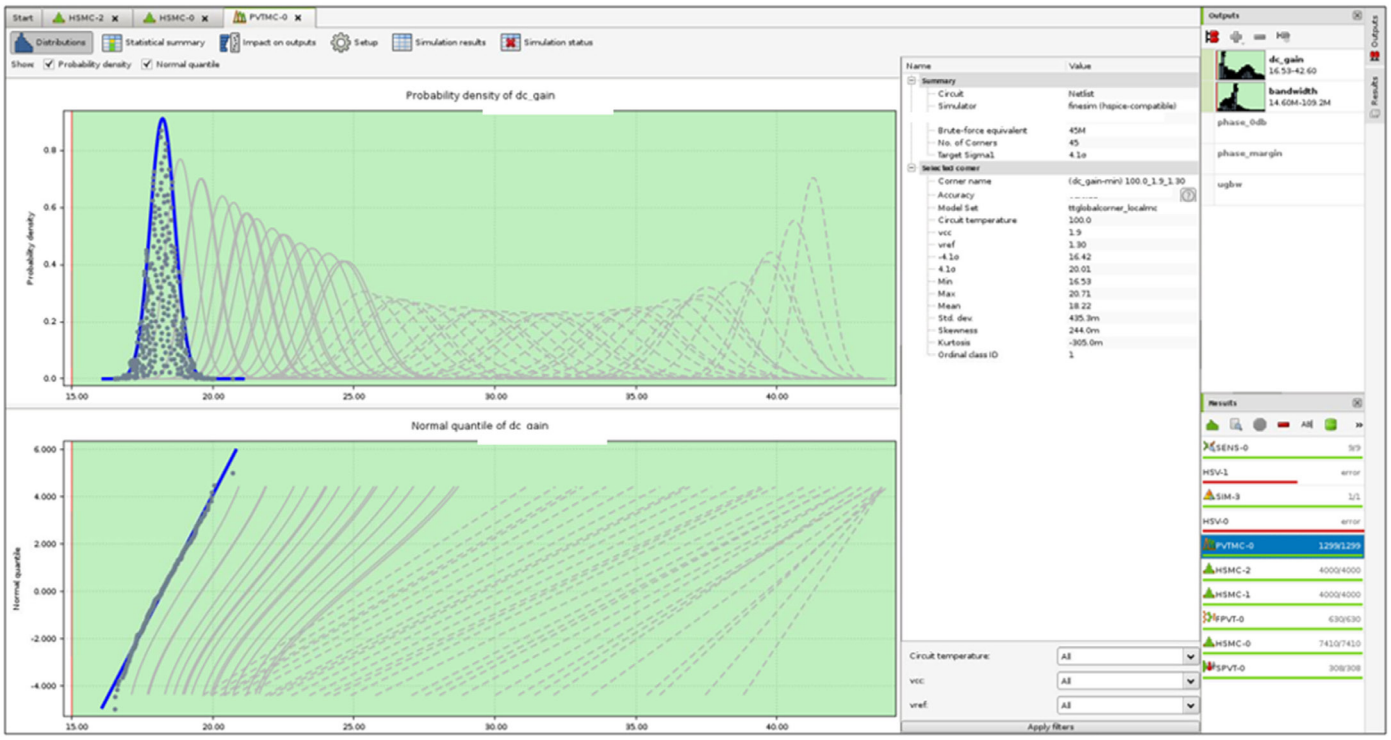

Figure 9: LVF data deep analysis and re-validation in Solido Variation Designer.

Solido variation designer

Solido Variation Designer is the world's most advanced variation-aware design solution that utilizes machine learning to deliver unprecedented speed, accuracy, and variation coverage. Solido Variation Designer provides deep analysis and full re-validation of problem areas identified by Solido Analytics, identifying the correct "golden" value LVF table values at 3 sigma and higher (figure 9). Using machine learning methods, Variation Designer is able to provide the correct reference sigma values (e.g., LVF cell transition/delay/constraints sigma values, as well as moments table data) with brute-force Monte Carlo accuracy, using 1000X+ less SPICE simulations and runtime.

Here, the user can either run PVTMC Verifier to obtain LVF golden reference results for problem areas identified by Analytics across a wide range of PVT corners, or High-Sigma Verifier to obtain LVF reference values for 4 sigma and higher, such as 6.5+ sigma. Both PVTMC Verifier and High-Sigma Verifier are part of Solido Variation Designer.

Conclusion

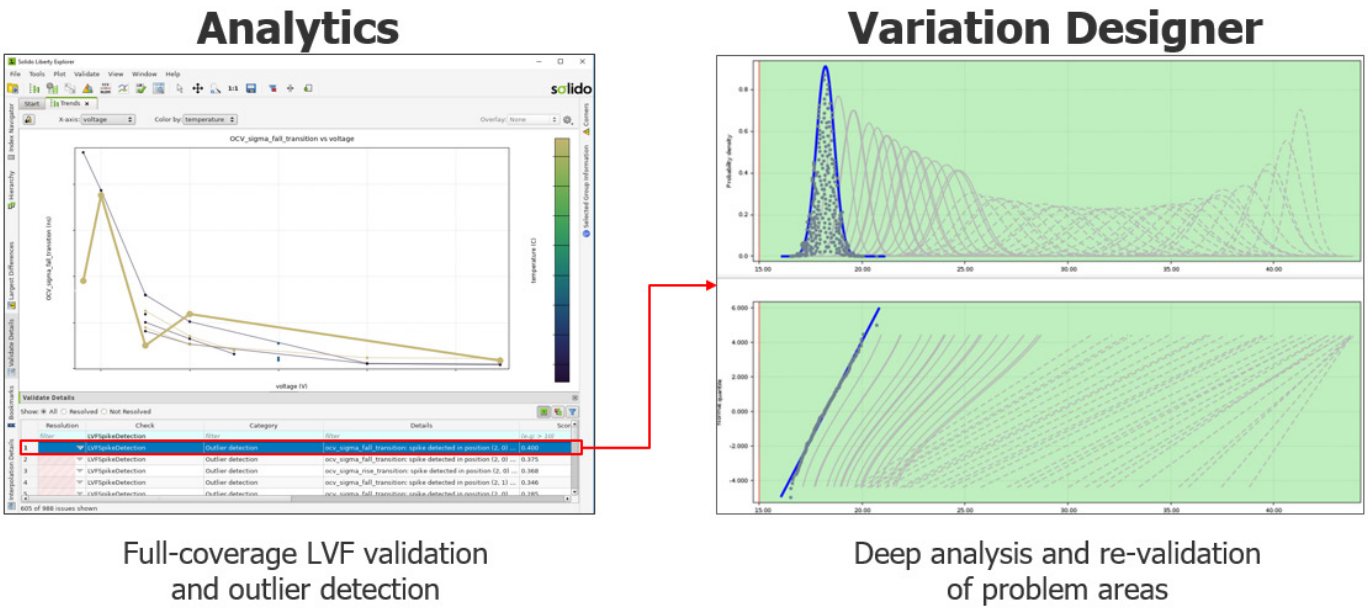

Figure 10: Closed-loop LVF validation: Analytics for full-coverage analysis, finding outliers in a “sea” of billions of values; Variation Designer provides Monte Carlo + SPICE-accurate results across full PVTs.

Closed-loop sign-off verification for LVF

Using Solido Analytics to identify problem areas and Solido Variation Designer for deep dive analysis and re-validation of data points identified by Analytics, results in a complete, closed-loop verification and re-validation flow for LVF data including moments (figure 10).

Siemens Digital Industries Software

Headquarters
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 972 987 3000

Americas
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 314 264 8499

Europe
Stephenson House
Sir William Siemens Square
Frimley, Camberley
Surrey, GU16 8QD
+44 (0) 1276 413200

Asia-Pacific
Unit 901-902, 9/F
Tower B, Manulife Financial Centre
223-231 Wai Yip Street, Kwun Tong
Kowloon, Hong Kong
+852 2230 3333

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