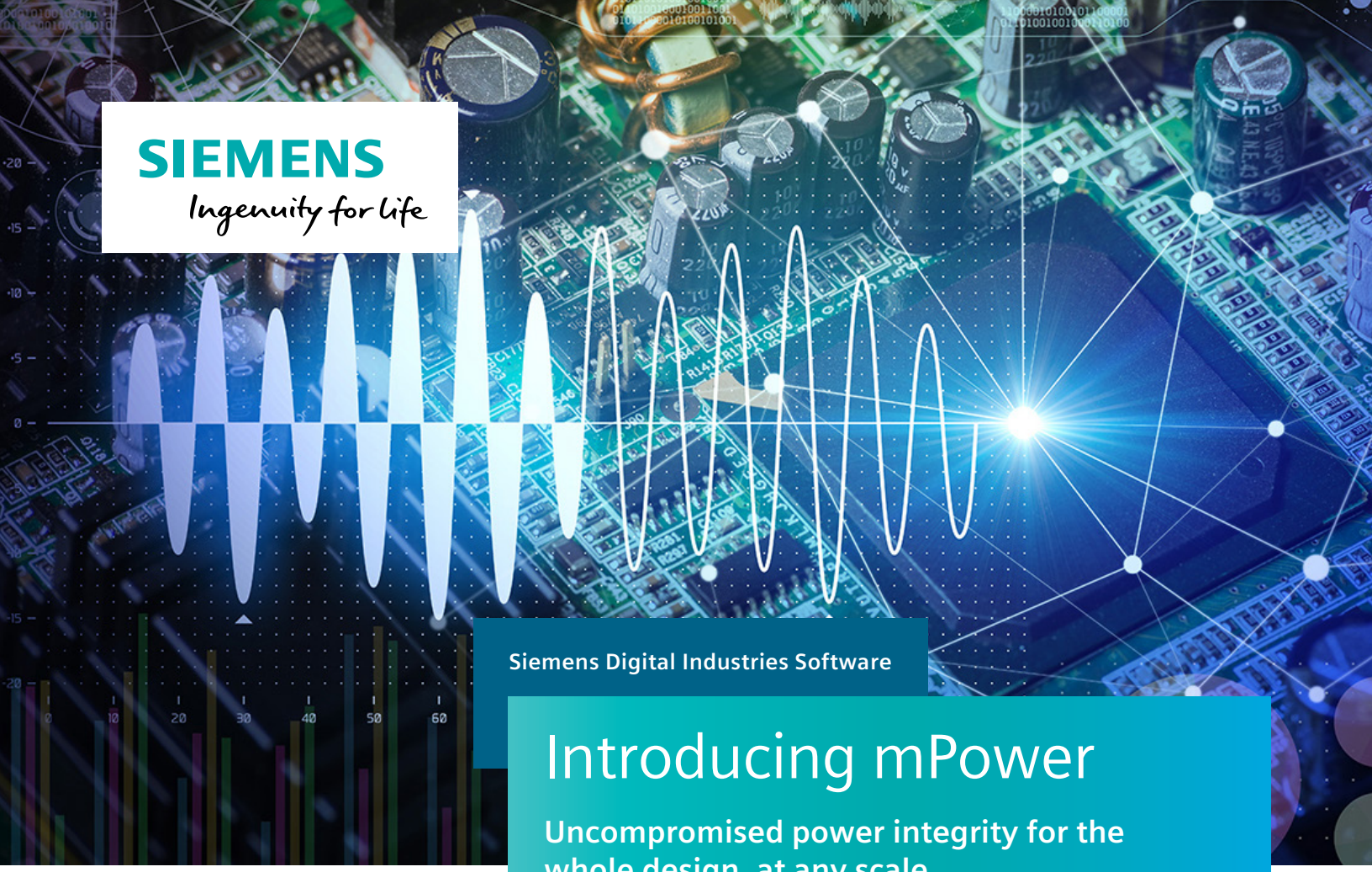

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Siemens Digital Industries Software

Introducing mPower

Uncompromised power integrity for the whole design, at any scale

Executive summary

Power integrity analysis evaluates circuits to determine if they will provide their designed/intended performance and reliability as-implemented. Designers must be able to verify analog and digital power integrity from the RTL/gate level through die-level integrations up to the package and board system-level. The mPower toolset is an innovative automated power integrity verification solution that brings analog and digital EM, IR drop, and power analysis together in a complete, scalable solution, enabling high-confidence power analysis tape-outs for all technologies and across all design types.

Joe Davis
Siemens Digital Industries Software

Background

Analog is a ubiquitous presence in our lives. The sound of a human voice, the hum of nature around us—we are born into an analog world. The digital age, in which computational power resigns supreme, is still relatively new to us, Babbage notwithstanding.

While our need for digital computation power seems insatiable and un-ending, we are moving into an era where the integration of analog and digital has become the enabler that puts a computer, a phone, a GPS, a media player, and a camera in the palm of your hand. Products and systems are differentiated not merely by their processing power, but by their assimilation into our everyday lives. Activity trackers report our heart rates, exertion levels, and even sleep patterns. Diabetics track glucose levels with stick-on patches or implants that interact with phone applications. Farmers use sensors and satellites to monitor crop and soil conditions and optimize yields. These activities are all enabled by analog sensors combined with high-speed digital computation operating at low power—this is the cross-domain synergy that the market is looking for, and the integration that is driving the need for the next generation of design enablement tools.

Figure 1 shows the expected increase in the number of CPU cores and power domains across four process technologies for the next five years, with the most advanced technologies growing the fastest. This trend is the result of design teams adding more and more capabilities to new chips, and having to add more processing bandwidth and power-management to support those capabilities while keeping the power of the chips within a given system power envelope. The last trend shown, often overlooked, is the growth in the number of analog blocks, which is driven by the need to connect that processing power in the chip to the real world. The number of analog/mixed signal blocks is growing at a compound annual growth rate of 10-15% across technology nodes from 5 nm to 28 nm. In addition, those blocks are getting bigger and more complex, as they connect to ever more powerful sensors in the system.

The integrated circuit (IC) industry collectively put a huge amount of investment into digital scaling. As the explosion in edge computing drives similar exponential growth in analog and sensor components, as well as functional integration, integrated circuit (IC) designers are finding that they simply don't have the electronic design automation (EDA) power analysis tools and methodologies they need when they get to the confluence of physical and electrical signoff. Abstraction is just fine for digital flows, but analog design flows don't lend themselves to such clean interfaces. Chip designers need a fast, effective, accurate, and integrated means of scaling their power analysis to the full analog system level, then to the combined digital/analog chip, and finally to multi-chip designs.

What is power integrity analysis and verification?

Power integrity analysis evaluates circuits to determine if they will provide their designed/intended performance and reliability as-implemented. For chip-level power integrity signoff, IC design companies must run

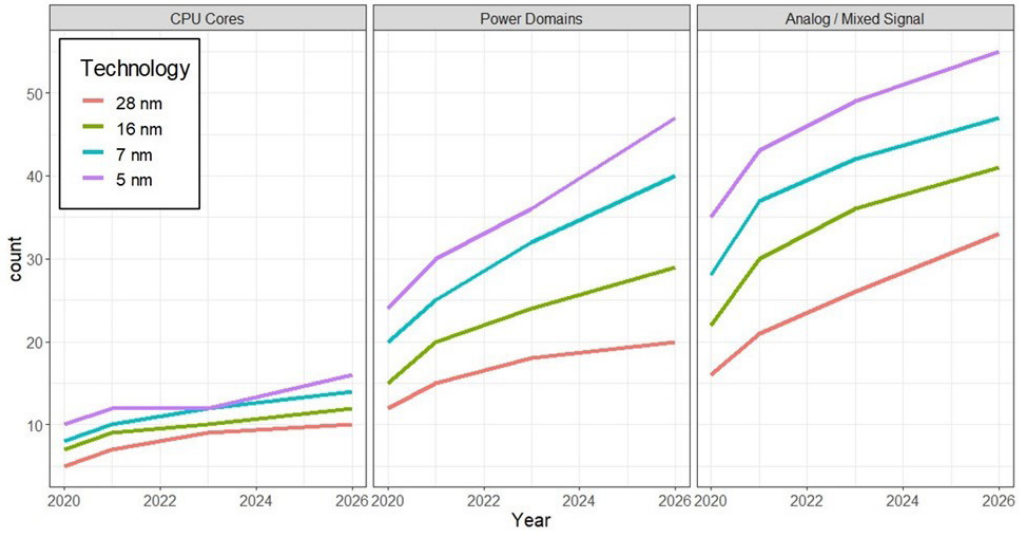

Figure 1. Growth in both digital and analog is putting pressure on existing power analysis solutions.

full-chip electromigration (EM) and voltage (IR) drop analysis to ensure that the power grid can deliver the necessary current to the devices to function as designed, and to ensure that the wires will not fail prematurely due to EM. A complete power integrity analysis solution comprises three main components:

- **Power:** Verify the chip design as implemented will provide the total predicted power under different operating modes.
- **Performance:** Find and eliminate performance issues affected by layout, such as at-speed fall-out, functional failures, etc.
- **Reliability:** Find and eliminate layout implementation issues that may impair performance and product life, such as EM, self-heating, etc.

Power integrity design flow

Now entering its 3rd generation, the system-on-chip (SoC) is becoming more and more a system-of-chips. Designers must be able to analyze and verify analog and digital power integrity from the RTL/gate level through die-level integrations up to the package and board system-level (figure 2).

Two primary factors currently inhibit full-scale power integrity analysis—the lack of automated analog EM/IR analysis, and combined analog/digital analysis scalability from the same EDA tool supplier.

EM/IR analysis on large analog circuits is where designers face the greatest challenges and operational pain. Existing tools are often difficult to use, especially for large analog layouts. Not only can the collection of all required inputs be difficult and time-consuming, but existing tools also lack robust interfaces for all design types and sizes, which impedes the process further. In addition, EM/IR verification typically requires additional setup from the base process design kit (PDK). Many foundries don't provide everything the design companies need, so they must expend additional time and resources to create their own.

Because large analog layouts are difficult to analyze with existing tools, the largest, most complex analog systems are often sent to manufacturing without a complete, detailed EM/IR analysis. Existing tools cannot simulate large netlists, only blocks, and don't provide designers with the necessary flexibility on the extracted netlists. These restrictions mean traditional simulation-based dynamic analysis is generally limited to designs with fewer than ~1-2M transistors. Beyond this size, the typical approach is to force analog designers into a digital-like hierarchical formalism that isn't well-suited for analog designs and design flows.

Super-block and chip-level analysis is typically performed manually, using simplifications, such as subsetting of the design, using less accurate simulators, and other ad hoc methods and approximations, which consume large amounts of engineering time to make up for the lack of automated tool support (figure 3). Neither static analysis or hand calculations provide the full coverage or confidence of simulation-based signoff. In addition, existing tools tend to create large

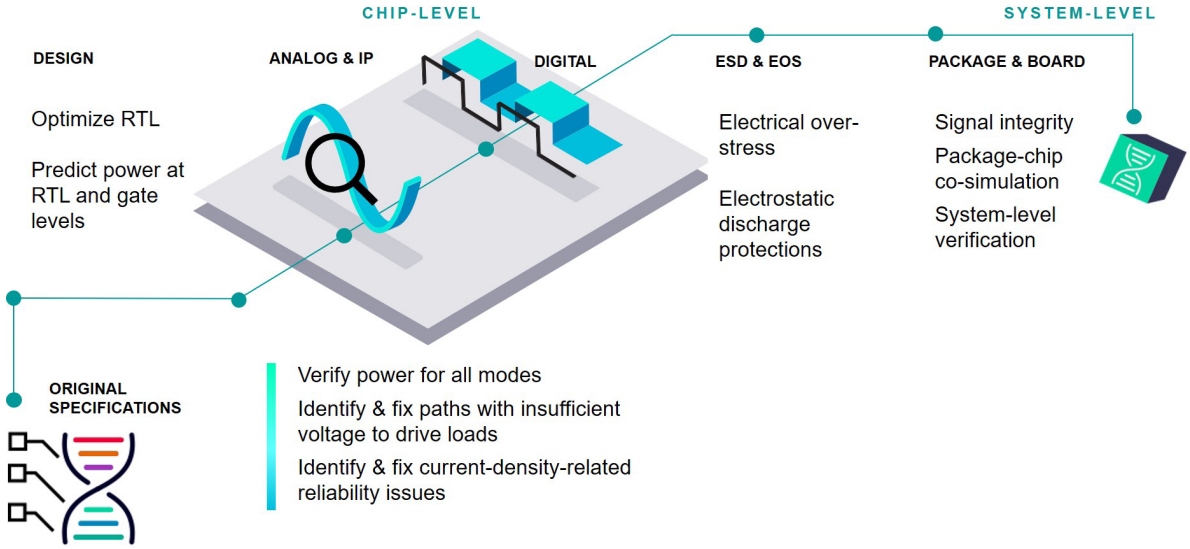

Figure 2. The power integrity design flow.

numbers of false errors for typical analog layouts, requiring even more time and resources for debugging. This lack of detailed automated EM/IR analysis for large-scale analog circuits puts the whole system at risk.

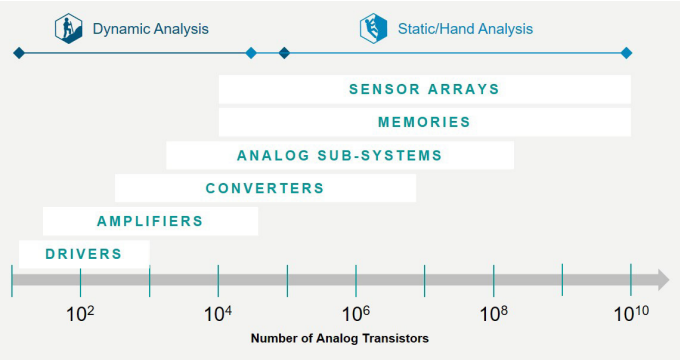

Figure 3. Static and manual analysis don't provide the coverage or accuracy needed for today's applications.

While there are credible solutions for large digital designs, existing digital power analysis options often have poor correlation to silicon, putting silicon delivery at risk. In addition, there is little to no integration with analog solutions, making full-chip analysis difficult, if not impossible.

High-profile, bet-the-company designs have significant engineering cost and risk. When full chip automated EM/IR analysis is impossible, and existing EM/IR tools fail, analysis must be done by hand with SPICE and manual calculations. Chips get out the door, but with no confident validation of power integrity. Design teams find themselves constantly chasing PI problems.

The increasing size and complexity of today's integrated IC designs demands an integrated analog and digital power integrity solution at scale to deliver full-chip designs with full confidence in the power implementation across all domains.

mPower power integrity solution

The mPower toolset is an innovative automated power integrity verification solution that brings analog and digital EM, IR drop, and power analysis together in a complete, scalable solution (figure 4). The mPower toolset provides efficient, easy to use power integrity analysis for digital, analog, and 3D IC chip designs across all design flows, at any scale, to verify that the design meets power-related design goals and performance. Analog and digital power analysis can be readily integrated into existing design flows while scaling to circuits and chips of any size. mPower enables high-confidence power analysis tape-out for all technologies and across all design types.

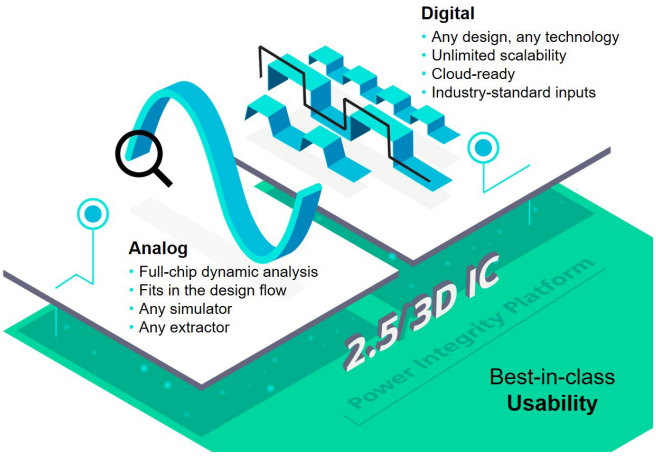

Figure 4. The mPower solution is the only power analysis solution that provides power integrity analysis for digital, analog, and 3D IC across all design flows, at any scale.

The mPower software enables design teams to perform power integrity analysis from the smallest blocks to the largest full-chip layouts to verify that the design meets power-related design goals and performance:

- Verify power for all modes
- Identify and fix paths with insufficient voltage to drive loads
- Identify and fix reliability issues related to current density

The mPower power integrity verification solution provides uncompromised power integrity analysis for the whole design, at any scale.

Performance

Designed from the ground up to scale on heterogeneous networks, the mPower solution delivers highly accurate results in the best turnaround time with the least cost. All mPower engines are optimized for maximum parallelism on heterogeneous networks. While other tools require large amounts of memory on a primary machine, the mPower tool distributes its memory needs across all remotes to minimize the overall burden on the grid.

Ease of deployment

The mPower solution is easy to adopt, in large part because it uses industry-standard formats and a simple and understandable TCL command language. The use of industry-standard inputs throughout the flow help minimize costs and increase reuse, while the TCL command language shortens and simplifies the learning curve.

When in use, the mPower solution automatically reports results during the run, enabling designers to get critical information while the run is still in progress. Results can then be highlighted back into all major design tools.

mPower GUI

The mPower solution include a fast, stable, and easy-to-use GUI for invocation and results debugging (figure 5). Designers can use the mPower GUI to identify root cause, then highlight results into design tools through the Calibre RVE interface for fixing. Features include:

- Fast, high-capacity for full-chip viewing
- Single or multiple page views
- Filter layout by net or instance name
- Browse ASCII report file and highlight wire/device in Report browser
- Trace Worst IR Drop pin to source pad
- Plot current/voltage waveforms

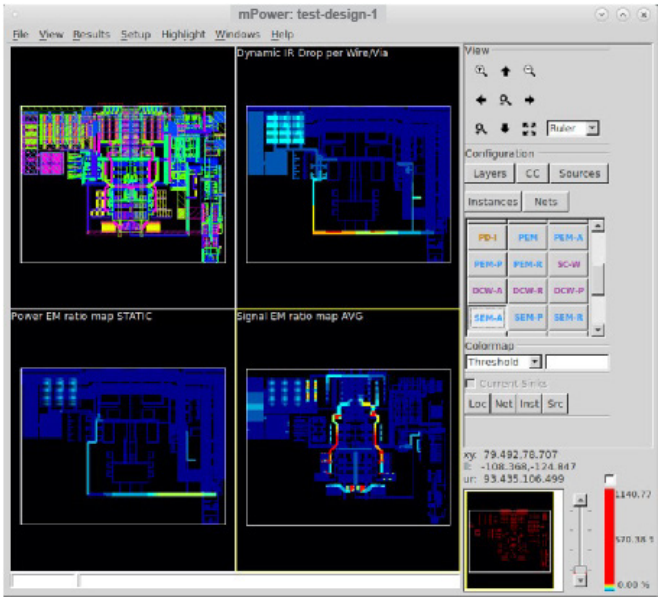

Figure 5. The mPower GUI enables engineers to quickly and easily run an mPower power integrity analysis, then debug the results.

mPower Analog

The mPower Analog software performs EM/IR analysis on transistor designs of any size—from the smallest bandgap reference to large analog systems and sensors. The mPower Analog tool brings scalability to transistor-level designs that was previously only available in the digital domain, to enable static and dynamic analysis on large circuits that no other tool can handle.

The key to mPower Analog scalability is its innovative high-capacity (HC) dynamic analysis functionality—a simulation-based EM/IR analysis that can run on the largest, most complex blocks and chips to enable fast, accurate power integrity analysis of 5G sensors and other large, complex IC systems.

High-capacity dynamic analysis

mPower HC dynamic analysis provides full coverage of and confidence in simulation-based signoff of large analog circuits across scale (figure 6). HC dynamic analysis provides the detailed analysis designers need to confidently sign-off designs for manufacturing, while enabling faster overall turnaround times by providing full-chip and array analyses from block-level SPICE simulations. It can also enable faster iterations early in the design cycle by using pre-layout SPICE simulations.

mPower Analog HC dynamic analysis provides a top-level EM/IR analysis that easily fits within existing design flows to enable designers to analyze blocks and chips that they simply couldn't with existing tools.

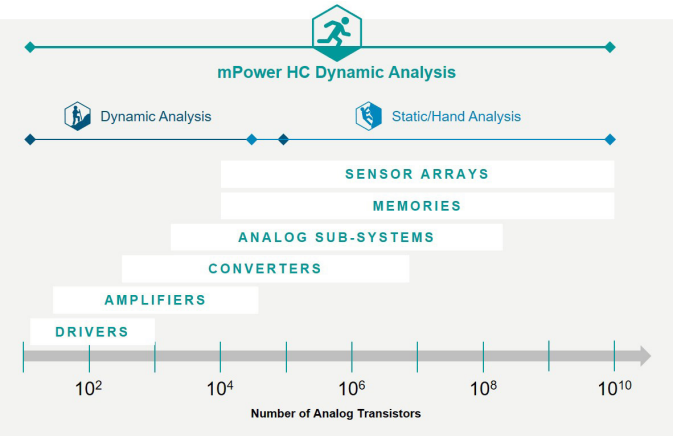

Figure 6. HC dynamic analysis provides simulation-based EM/IR analysis on the largest, most complex blocks and chips.

Fast and flexible

mPower Analog provides faster overall turnaround times by providing full-chip and array analyses from block-level SPICE simulations. It speeds up iterations by using pre-layout SPICE simulations. Equally important, it provides unparalleled flexibility on simulation and extraction:

- Use any extractor to drive post-layout SPICE simulation
- Use any SPICE simulator that can write a fast signal database (FSDB)
- Additional benefits, such as automatic probe insertion and simplified setup, are available when using Calibre® parasitic extraction tools and the Analog FastSPICE platform from Siemens

mPower Digital

The mPower Digital solution provides digital power integrity analysis with massive scalability to enable design teams to analyze the largest designs quickly and accurately.

Accurate

The mPower Digital tool provides accurate results with standard Liberty models. At advanced nodes, industry-standard CCSP extensions to the standard Liberty models can be used for enhanced accuracy.

For memories, the mPower Digital tool supports multiple levels of modeling to provide a rich tradeoff between performance and accuracy. The mPower Digital software supports models from the simple LEF + Liberty to GDSII views to fully-embedded transistor-level models.

Scalable to any size

Large chips require fast turn-around for confident tapeout. The mPower Digital tool delivers rapid full-chip signoff EM/IR runs to enable multiple iterations and minimize over-design.

High coverage vectorless analysis

The mPower Digital software employs a vectorless algorithm that selects a subset of instances based on switching power, load, and other parameters. Even though all instances aren't sampled in a single run, the high-coverage algorithm ensures that all instances are sampled over multiple iterations, enabling the mPower Digital tool to find new violations (figure 7).

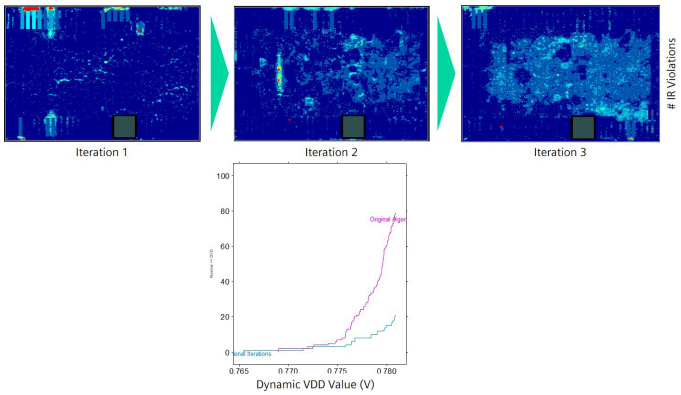

Figure 7. Multiple iterations ensure full coverage for fast, accurate analysis.

In-rush analysis for power-gated designs

The mPower Digital software simulates the turn-on of power-gated designs for peak current and turn-on time, and automatically calculates the required simulation time, which eliminates guesswork and minimizes over-simulation (figure 8).

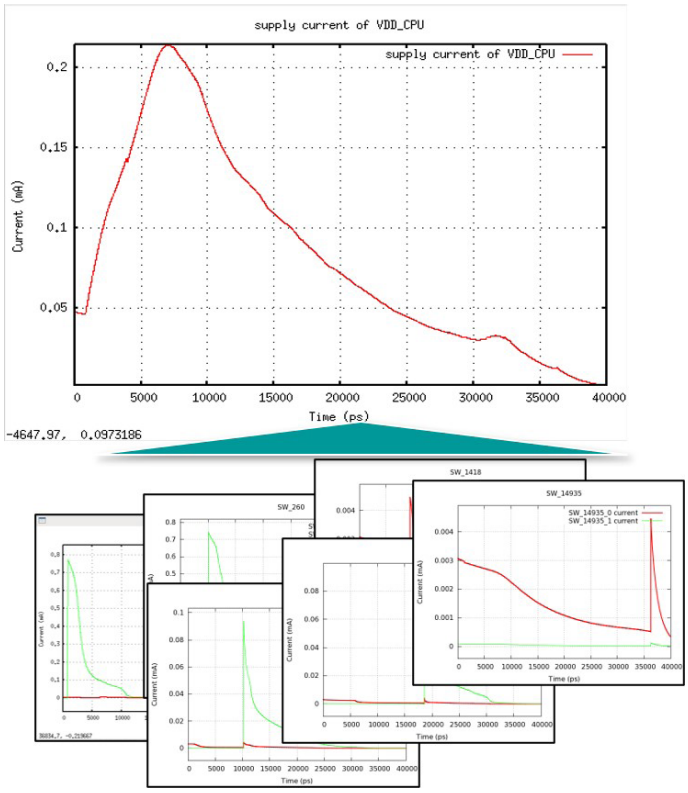

Figure 8. Turn-on/turn-off simulation provides fast, efficient analysis of power-gated designs.

RTL profiling and vectored analysis

The mPower Digital tool can use either gate-level or RTL-levels vectors for vectored simulation (figure 9). Using RTL-level vectored EM/IR analysis shortens the analysis timeline and saves compute resources. The event-based propagation captures glitches using an accurate stage delay. RTL profiling quickly identifies high-power frames, and is intended for large VCDs early in design cycles. Memory instance power profiling can be used to drive power aware MEMBIST insertion.

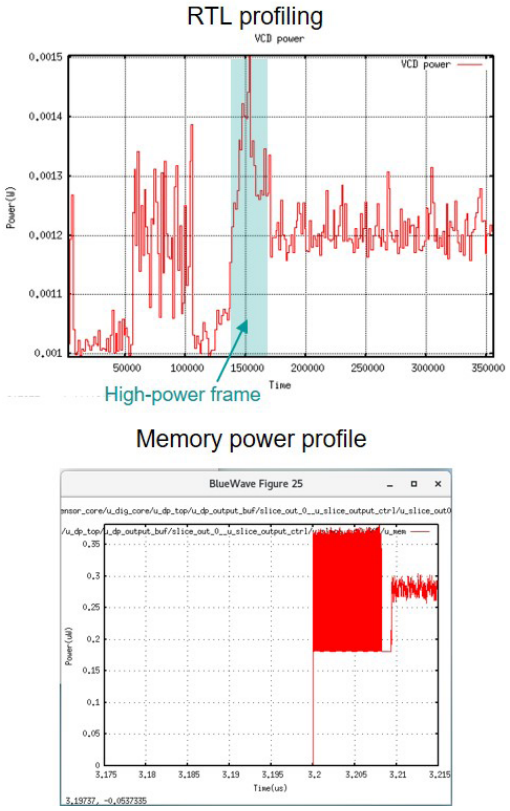

Figure 9. RTL and memory power profiling provide fast, accurate vectored simulation.

Integrated power integrity solution

Design companies need accurate, automated power/EM/IR analysis for both analog and digital layouts, as well as full-chip verification. The mPower solution delivers accurate, easy-to-use power integrity verification that can be readily integrated into existing analog and digital design and verification flows. mPower functionality handles all designs at all nodes, encompassing a wide range of foundries and technologies. The mPower GUI simplifies invocation, while tight Calibre integration provides full-featured root cause analysis and debugging. With the mPower solution, design companies now have no-compromise power integrity for the whole design, at any scale.

Complete electro-physical signoff suite

The mPower power integrity solution also completes the Siemens overall electro-physical signoff suite addressing power, performance, and reliability analysis. Other offerings in this suite include the PowerPro platform, Analog FastSPICE (AFS platform), Calibre PERC reliability platform, Calibre YieldEnhancer with SmartFill technology, and the HyperLynx toolsuite.

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