What’s New?
Release Highlights
Tanner Tools v2023.2

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Operating system support

- Windows:
  - Tanner Tools currently supports both Microsoft Windows 10 and Windows 11
- Linux:
  - Tanner Tools currently supports both RHEL 7.9 and RHEL 8

Enhancements

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Across the flow

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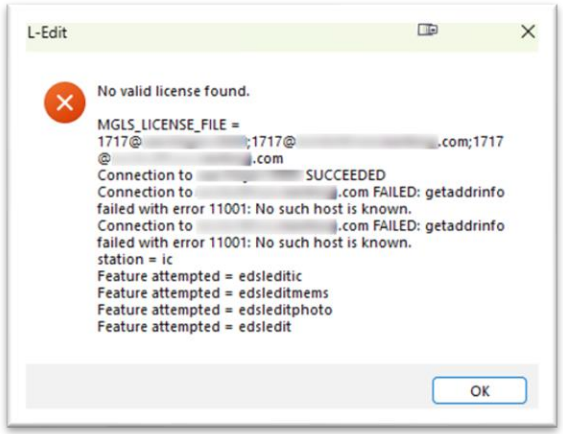
Installer changes

- Default install path is changed to *C:\SiemensEDA*
  - To enable the installer to see older Mentor Graphics installations so they can be uninstalled:
    - Go to **Tools > Installation Preferences**
    - Select the **Target List** tab and select **Add**
    - Browse to the *C:/MentorGraphics* folder and press **Select Target**

Licensing Changes

- Tanner suite of tools has been upgraded to use Siemens Advanced Licensing Technology (SALT) licensing version 2.1.0
  - Clients using SALT 2.0 or greater require upgrading to Siemens License Server 2.x or greater (available on Support Center)
  - ***saltd*** Common Vendor Daemon replaces ***mgcld*** Daemon but does not require a new license file
  - Defaults ports have changed from 1717 to 29000
  - **SALT_LICENSE_SERVER** Environment Variable now required (instead of **MGLS_LICENSE_FILE**)
  - See https://support.sw.siemens.com/en-US/product/1586485382/knowledge-base/MG612613 for more information
- The licensing failure dialog now has information about license servers defined, and if they could be connected



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Linux Performance Improvements

- Performance of log windows is improved for large amounts of data logged
  - Improved performance on any operation that logs many messages to the log window
  - In particular, performance of small AFS simulations where logging would take more time than simulation is greatly improved
- Memory allocation enhancements improved overall performance on Linux

Multi-threaded Design Loading

- Performance opening a lib.defs has been improved by multi-threaded reading of the list of views to populate the Library Navigator in both S-Edit and L-Edit
- Performance improvements up to 10x have been accomplished, especially improved for slow environments such as reading from a drive over a network

Library Manager

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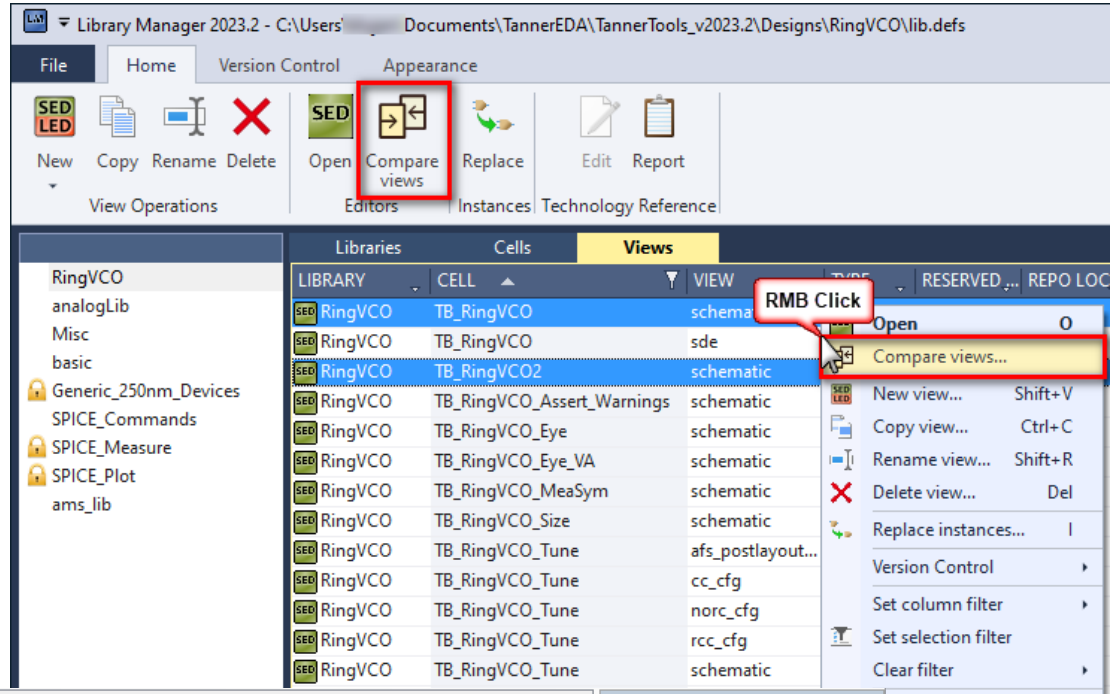
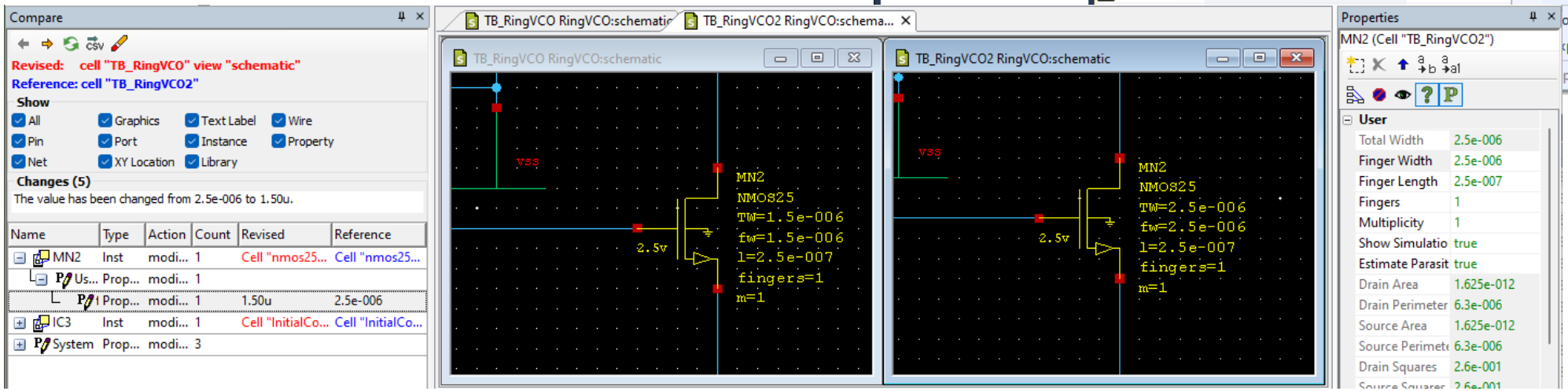
Launch Schematic Compare from Library Manager

- New option to select two schematic or symbol views and launch S-Edit Compare for the two views two display the differences between them





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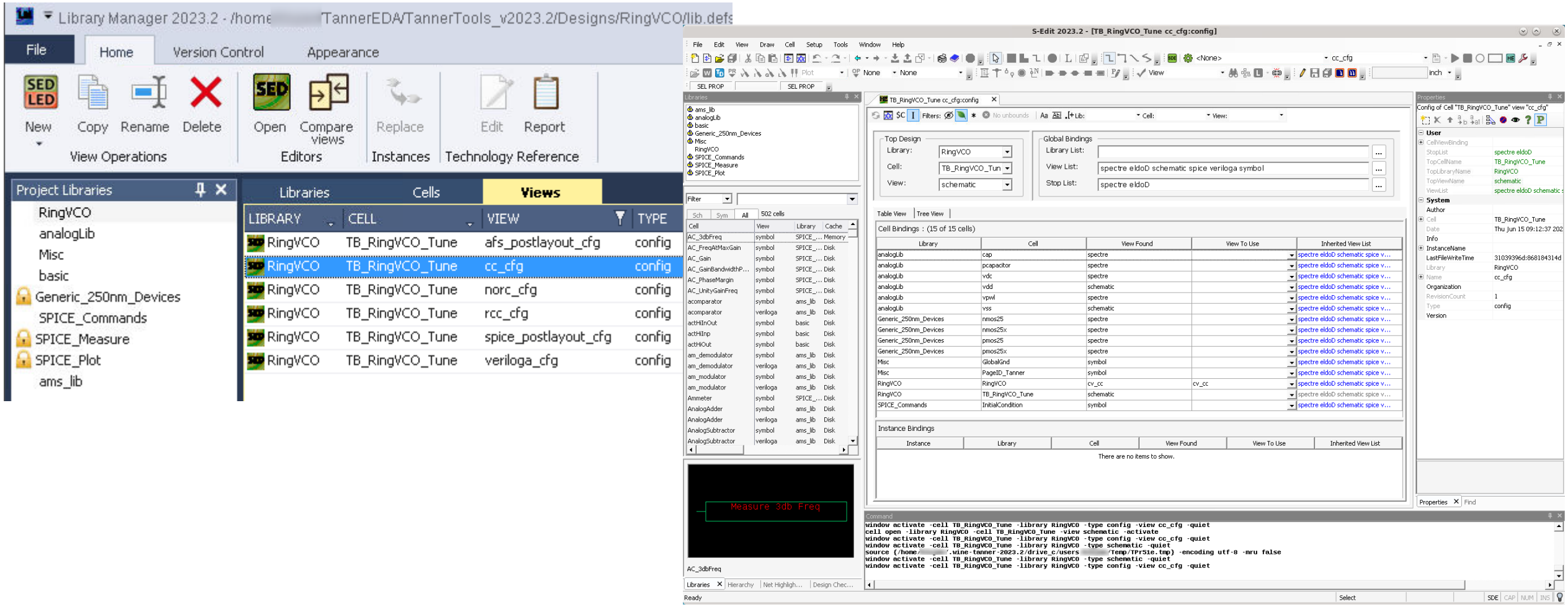
Library Manager - SDE Integration (Linux Only)

- Open any config view to launch S-Edit with SDE



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S-Edit

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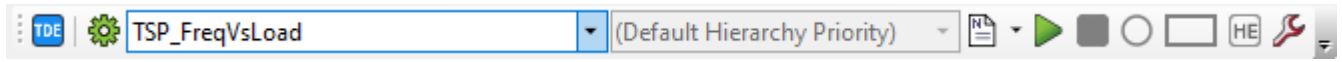
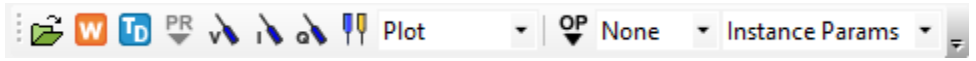
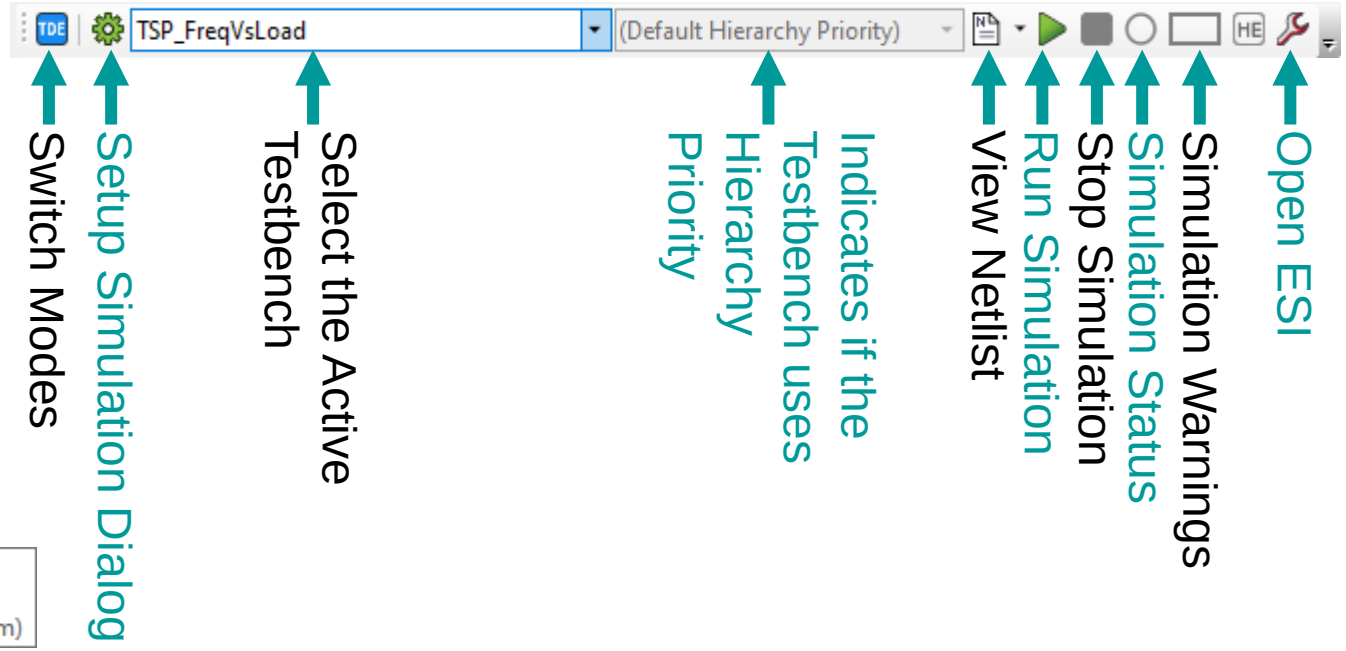
TDE vs SDE

- With the Integration of SDE into S-Edit as an alternative simulation environment or a way to access Solido Variation Designer, we have made it easy to switch between Tanner Design Environment (TDE) for simulation environment (Setup Simulation dialog) and Solido Design Environment (SDE) for simulation environment and Variation Designer (external program)
- SDE integration is only allowed when running S-Edit on Linux
- To support the integration of SDE, the simulation toolbar was split into two toolbars
  - Run Simulation toolbar 

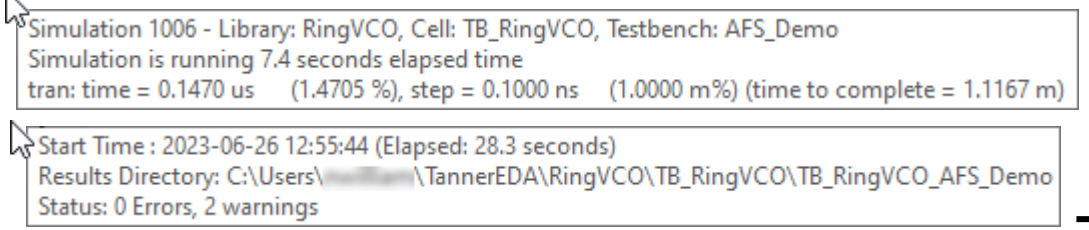
  - Simulation Results toolbar 

- Button on Run Simulation toolbar switches between TDE and SDE mode

Run Simulation Toolbar – TDE Mode



- New field on the toolbar to indicate if the selected testbench uses Hierarchy Priority
- View Netlist – Exports netlist and opens it in S-Edit regardless of Simulator
- Simulation Status
  - Tooltip shows more information



- Simulation Warnings
  - Shows the number of warnings from the last simulation 
  - Red outline indicates warnings increased from the last simulation 

Icon	Simulation Status
	Simulation results were not found
	Simulation in progress – Tooltip will show progress
	Last simulation did not complete or failed.
	Last simulation completed.

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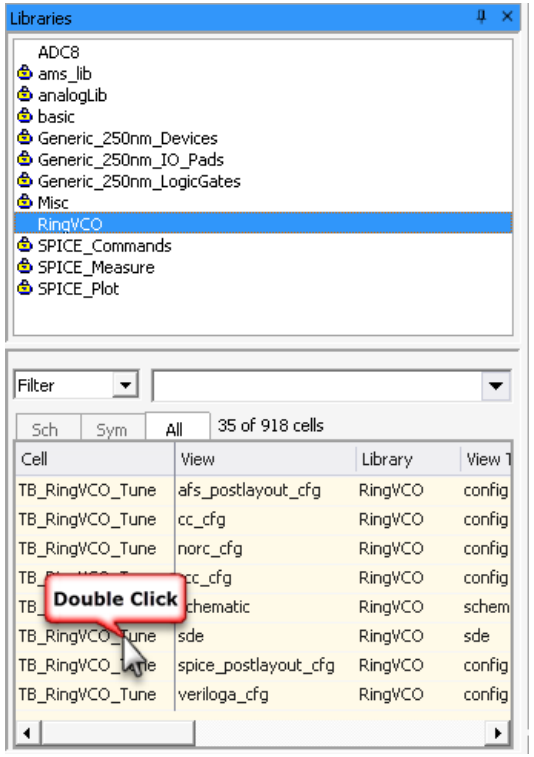
Run Simulation Toolbar – SDE Mode

- First dropdown shows all SDE states of the active view
  - Select the SDE state and press Open SDE button  to start SDE and open that state
  - Users can additionally open the SDE state by double-clicking the SDE state in the Library Navigator
- Second dropdown shows the Config View associated with the active view
  - This will affect traversing the hierarchy
- Clicking the Hierarchy Editor button HE will open the hierarchy editor on the selected config view in the second dropdown
  - Users can additionally open a config view by double-clicking it in the Library Navigator



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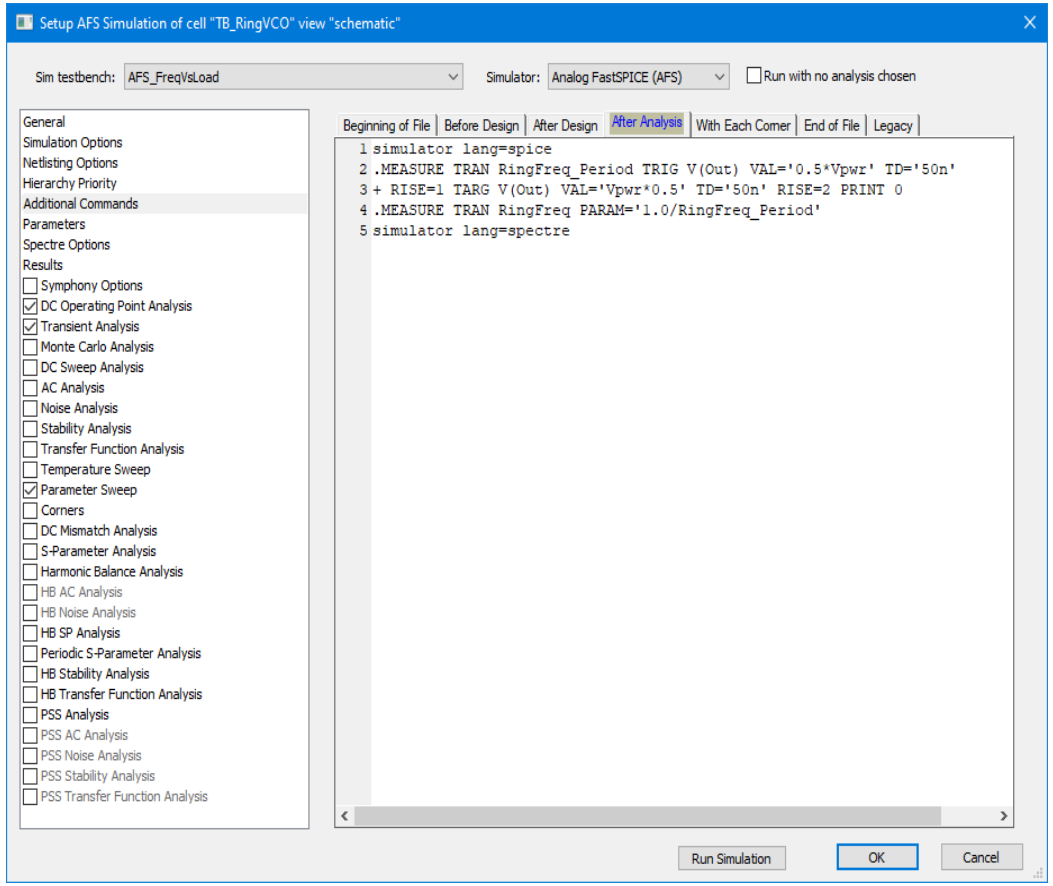
Tanner Design Environment (TDE)



- RF Analysis Pane improvements
  - Updated all RF related analysis panes
  - Added Jitter Measurements to PNoise
  - Added Harmonic Balance S-Parameter Analysis
  - Added Harmonic Balance Stability Analysis
  - Added Harmonic Balance Transfer Function Analysis
  - Added PSS S-Parameter Analysis
- Symphony now exports empty .SUBCKT for Verilog block so you can use the connect pin by name functionality
- More control over where Additional Commands are added to the netlist
- Many enhancements and improvements have been made to various Setup Simulation, including Simulation Options, DC Operating Points analysis, DC Sweep, Monte Carlo, AC Analysis, Noise Analysis, Stability analysis, Temperature Sweep, DC Mismatch analysis, and Corner Analysis

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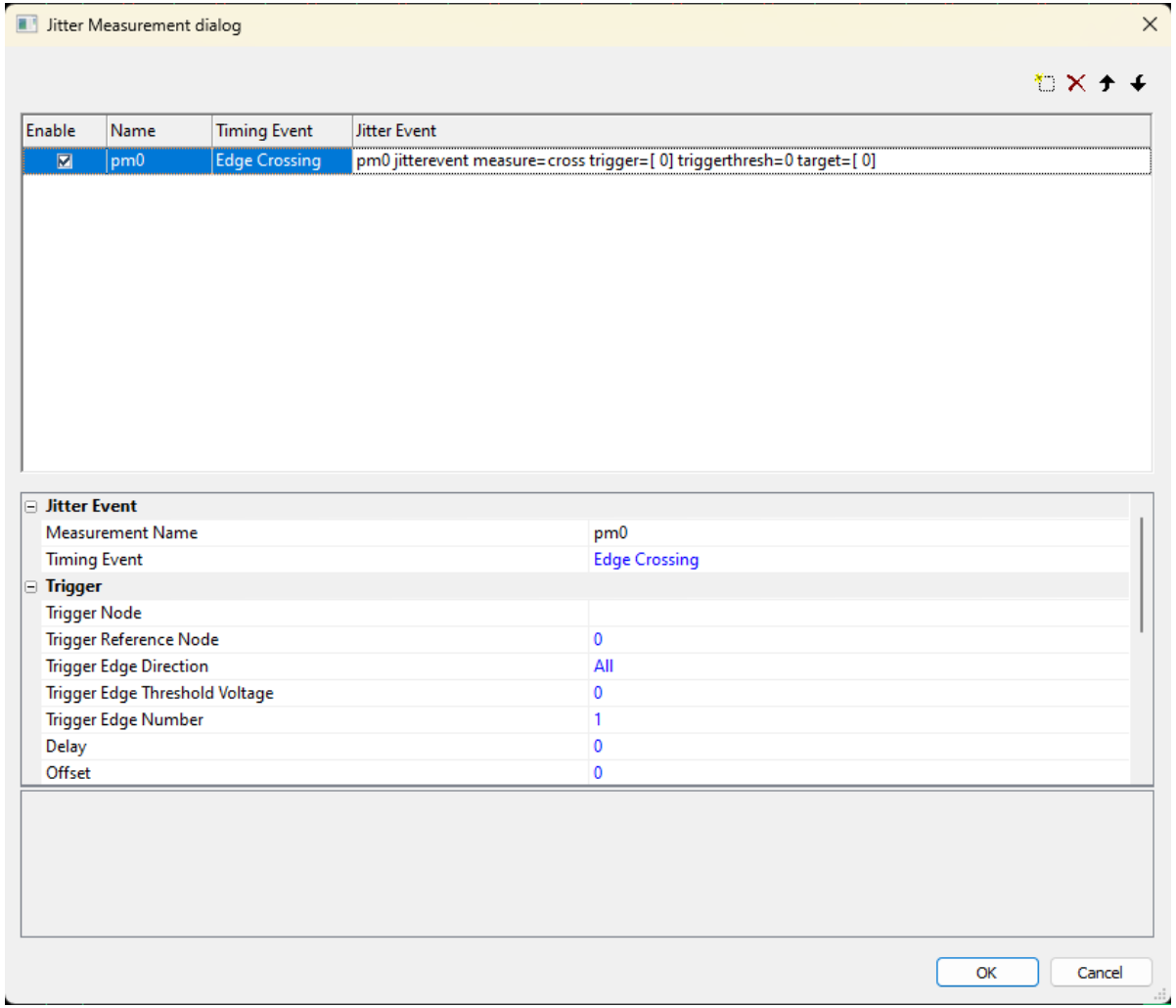
New AMS PSS Noise Analysis Jitter Measurement Dialog

- A new dialog box has been added to AFS PSS Noise Analysis for setup of Jitter Measurements



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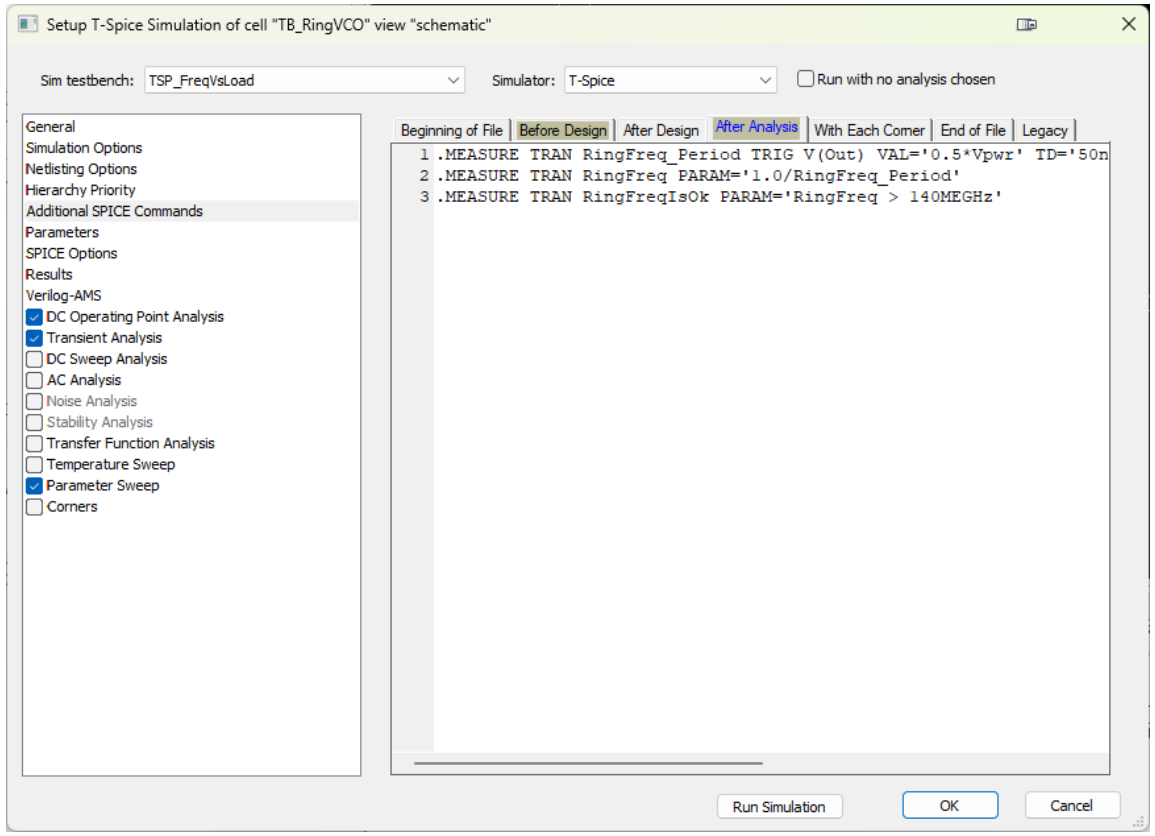
S-Edit Testbench Additional Commands

- Testbench setup enhanced to give greater control over where additional commands can be placed in the netlist
- Lines are numbered
- Tab indicates if data is entered in tab
- Additional commands can be placed in in a tab corresponding to any of the following places:
  - Beginning of file
  - Before Design
  - After Design
  - After Analysis
  - With Each Corner
  - End of File
- Additional Commands from prior releases will be placed in a tab called **Legacy**



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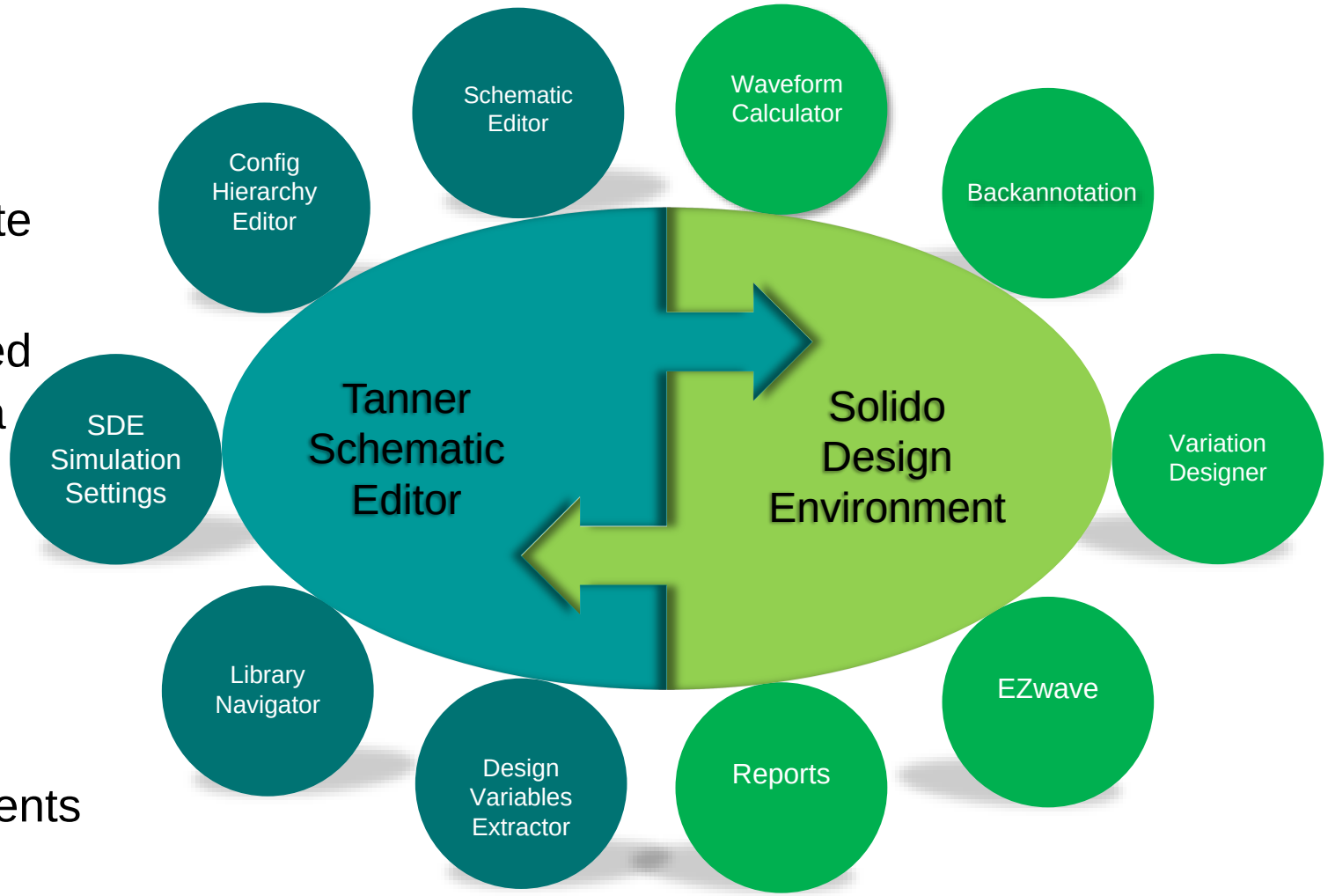
S-Edit AFS Simulation Command Line Argument Change

- AFS simulations now use the `--ovd` command line argument for all simulations
  - Results in a different representation of the data in the simulation database if doing an DC OP analysis (not a DC sweep) and doing either Monte Carlo, corner, or parameter sweep
- Default command line arguments can be overridden in ESI
- In the previous version, when doing a DC OP with AFS with either Monte Carlo, Corners, or Parameter Sweep, it would allow you to reference the results as a waveform using the `wf("<sim/Folder>Wavename")` format
  - The expression `wf("<sim/Folder>Wavename")` will not longer work and will result in a **cannot be found error** in EZwave
- In v2023.2, you can refer to the results in an expression in two different ways:
  - `DATA("Wavename","Folder")` – This will return a list of values
  - `var("<sim>Folder:Wavename", option="WF")` – This will return a waveform of the results but with the X axis as the either Monte Carlo iteration number or the parameter sweep iteration (a number from 1 to the total number of sweep points)
- See Tech Note online for more details

Tanner/SDE Integration Features

- SDE fully Integrated into Tanner Schematic Editor tool
- New Hierarchy Editor tool to create and manage config views
- Common simulation settings saved along with S-Edit preferences in a central location
- Automatic extraction of Design Variables from the design
- Interactive selection of design objects
- Back-annotation of Voltages/Currents and Operating Point Results
- Waveform cross probing



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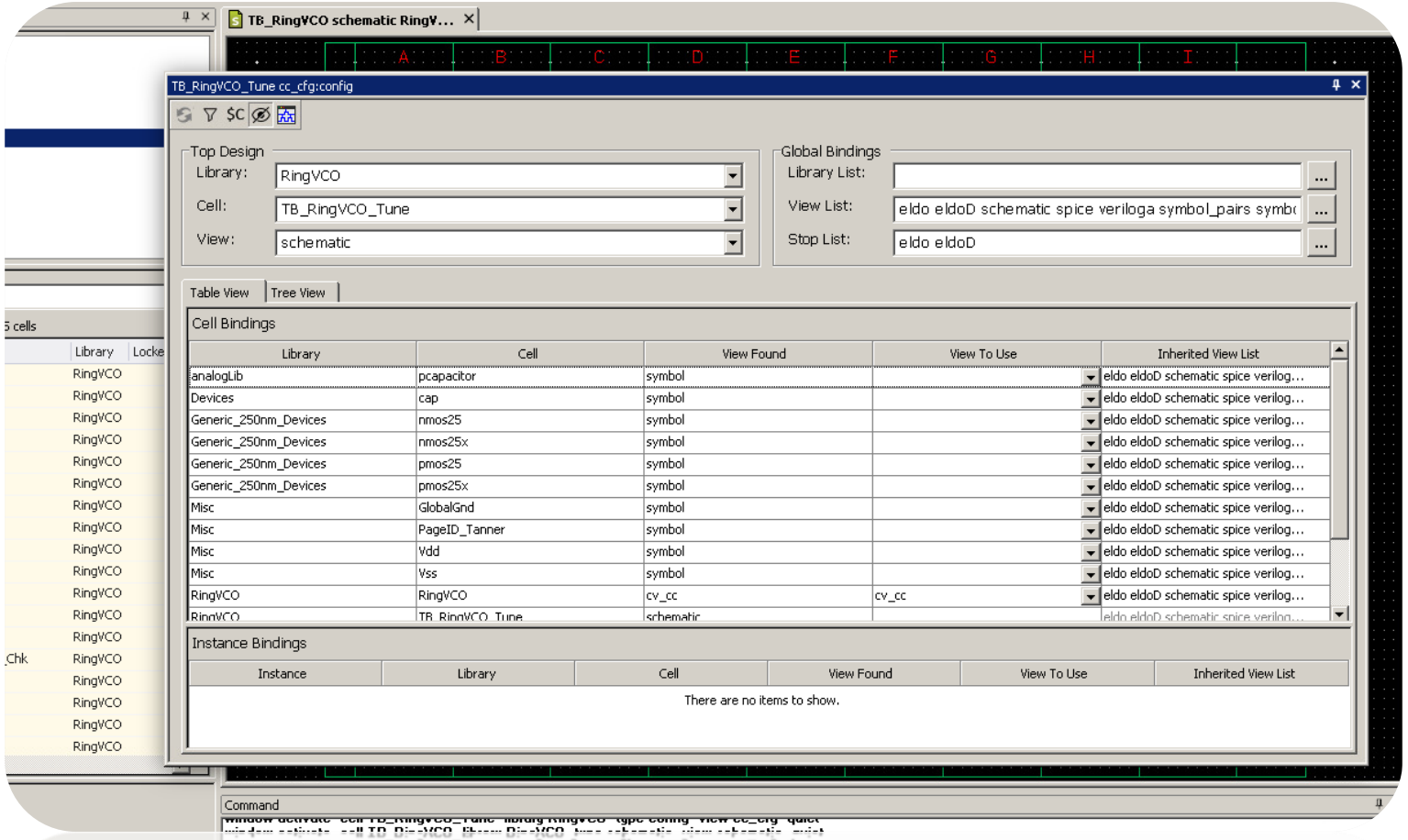
Solido Design Environment (SDE)

- Comprehensive variation-aware design
  - Supports analog, RF, mixed-signal, memory and standard cell design
  - Identifies design weaknesses undetectable by other methods
  - Improves design quality and time-to-market
  - Uses machine learning to accelerate simulation
- Trusted by top semiconductor companies and foundries
  - Fast, accurate and thorough
  - 1000X+ faster than brute force simulation
  - Full coverage verification across PVT and Monte Carlo
- Easy to use and deploy
  - Intuitive GUI for interactive design and analysis
  - GUI or batch mode
  - Works with all process technologies

Config Hierarchy Editor

- Brand new tool to create and manage config views
- Creates industry-standard OpenAccess (OA) based views
- View editor implemented using Multiple Document Interface (MDI) in S-Edit framework so the config views can be managed just like any other views
- Intuitive and customizable user interface
- Uses config views created in third-party tools without translation/migration



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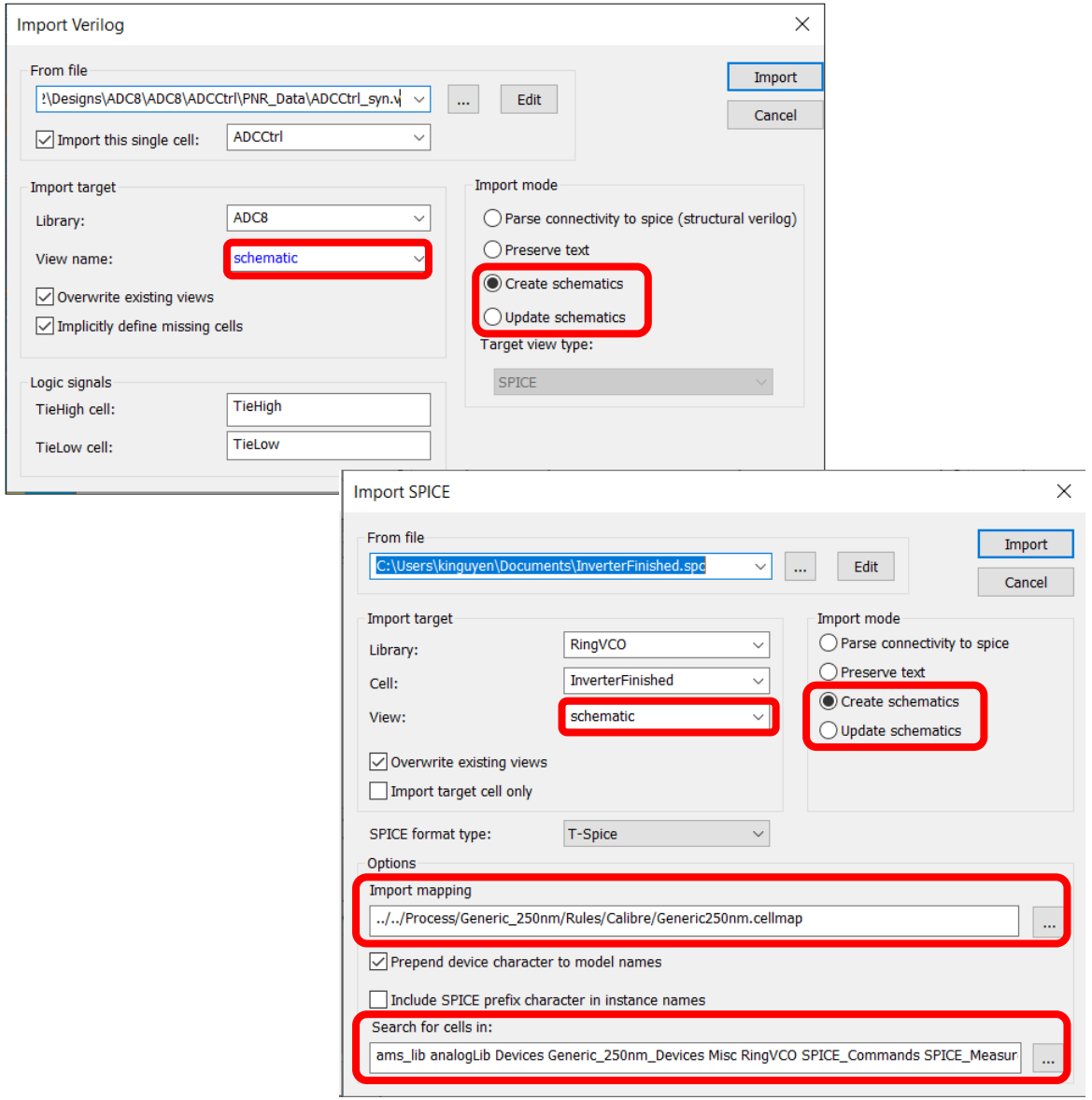
Netlist to Schematic Generation

- Generates a schematic from a netlist
  - Creates an array of instances with netlabels on the pins for connectivity (no wires)
  - Schematic can be used for simulation or LVS netlisting
  - Generates any missing symbols not present in the design library
  - Netlists supported:
    - Structural Verilog netlist (typically from synthesis)
    - SPICE/CDL digital netlist (typically from place and route)
    - Analog SPICE netlist (partially supported)



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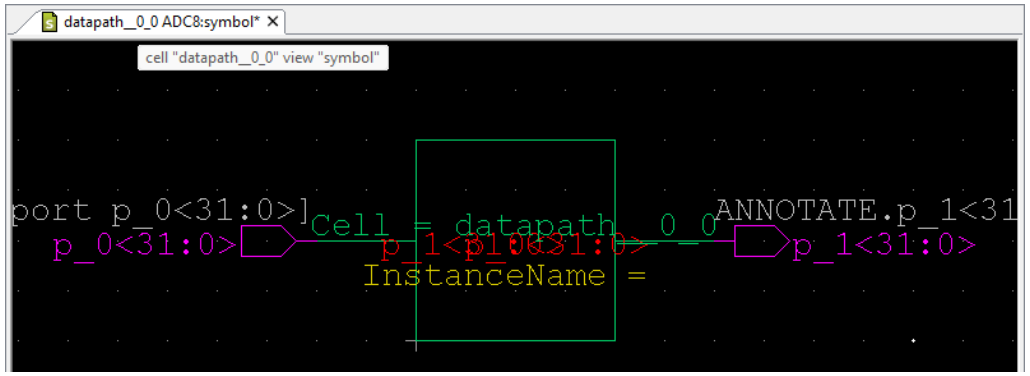
Netlist to Schematic Generation Example – Structural Verilog

Modified

Sch | Sym | All | 3 of 643 cells

Cell	View	View Type	Instances	Library	DM Reserv...
ADCCtrl	schematic	schematic		ADC8	
datapath__0_0	schematic	schematic		ADC8	
datapath__0_0	symbol	symbol	1 instance	ADC8	



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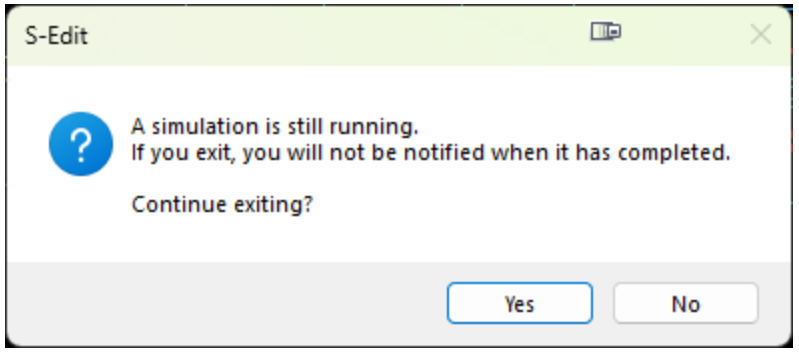
S-Edit Close Warning when External Simulator is Running

- Warn if trying to close S-Edit while an Eldo, AFS, or Symphony simulation is running
  - Gives users a chance to proceed or cancel



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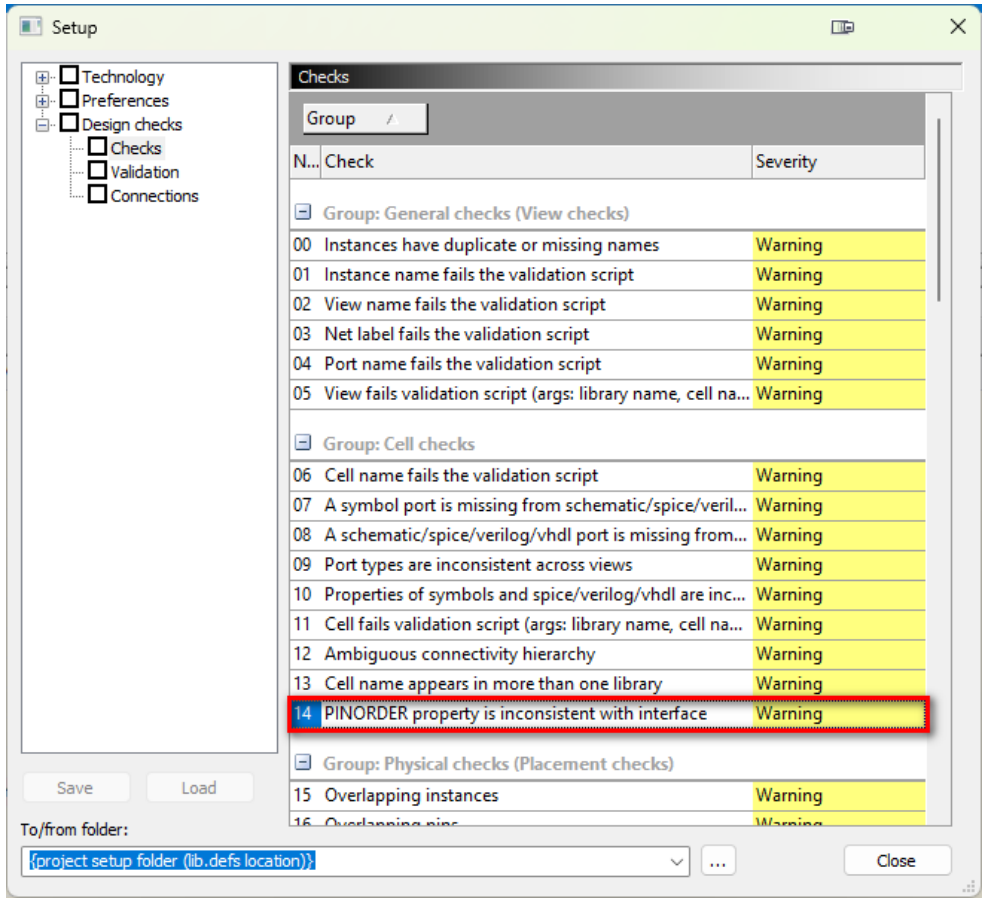
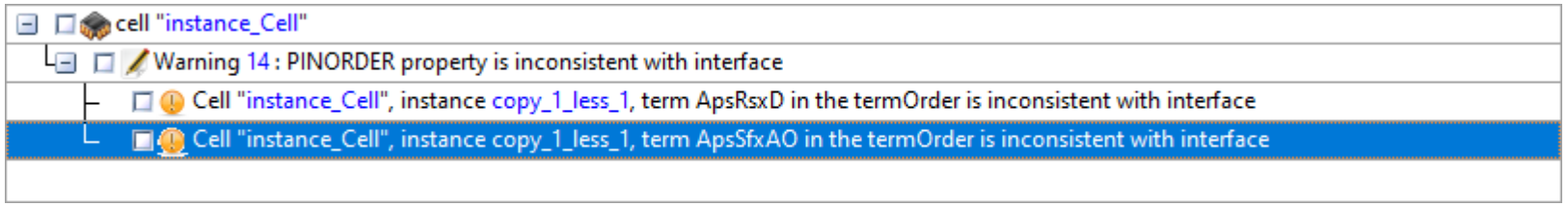
Added Additional Check to Design Check #14

- Warn user when CDF or other term order is inconsistent with an interface





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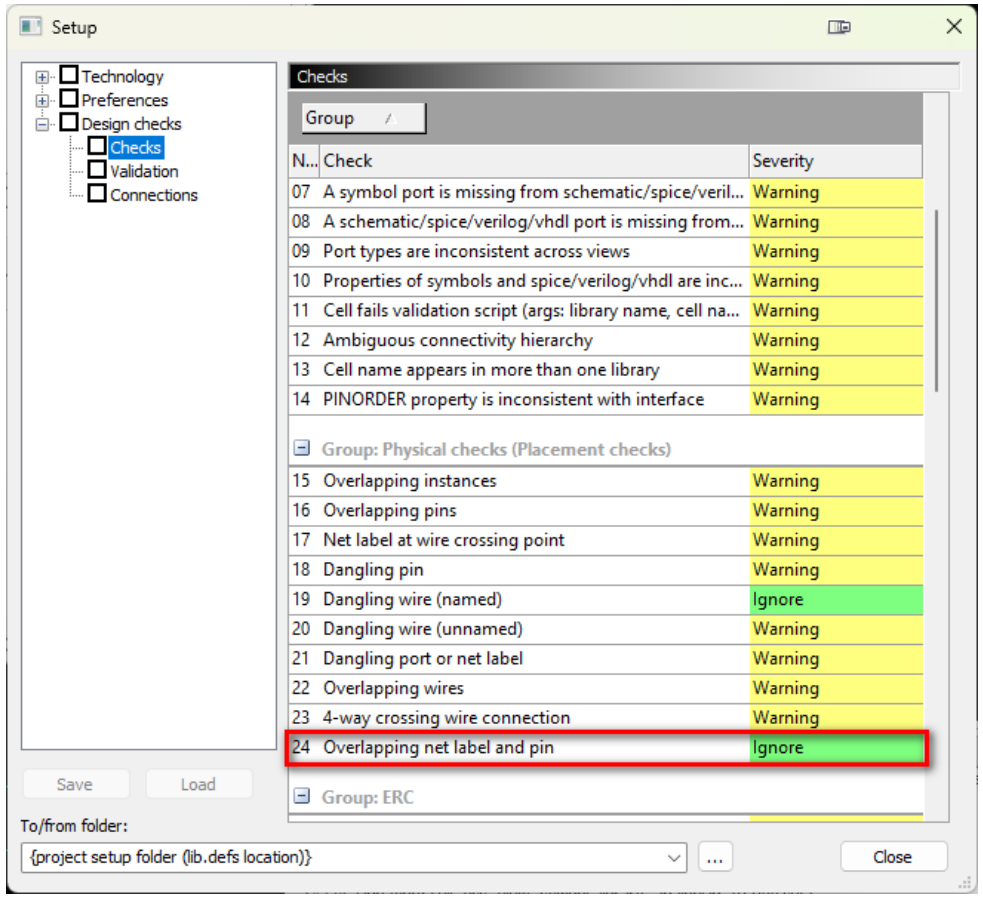
Modified Default Value of Design Check #24

- Default value of Design Check #24 – **Overlapping netlabel and pin** changed from **Warning** to **Ignore**
- Importing a netlist to Schematic, as well as importing a Calibre View, will create symbols with netlabels on the pins, and these should not generate a warning



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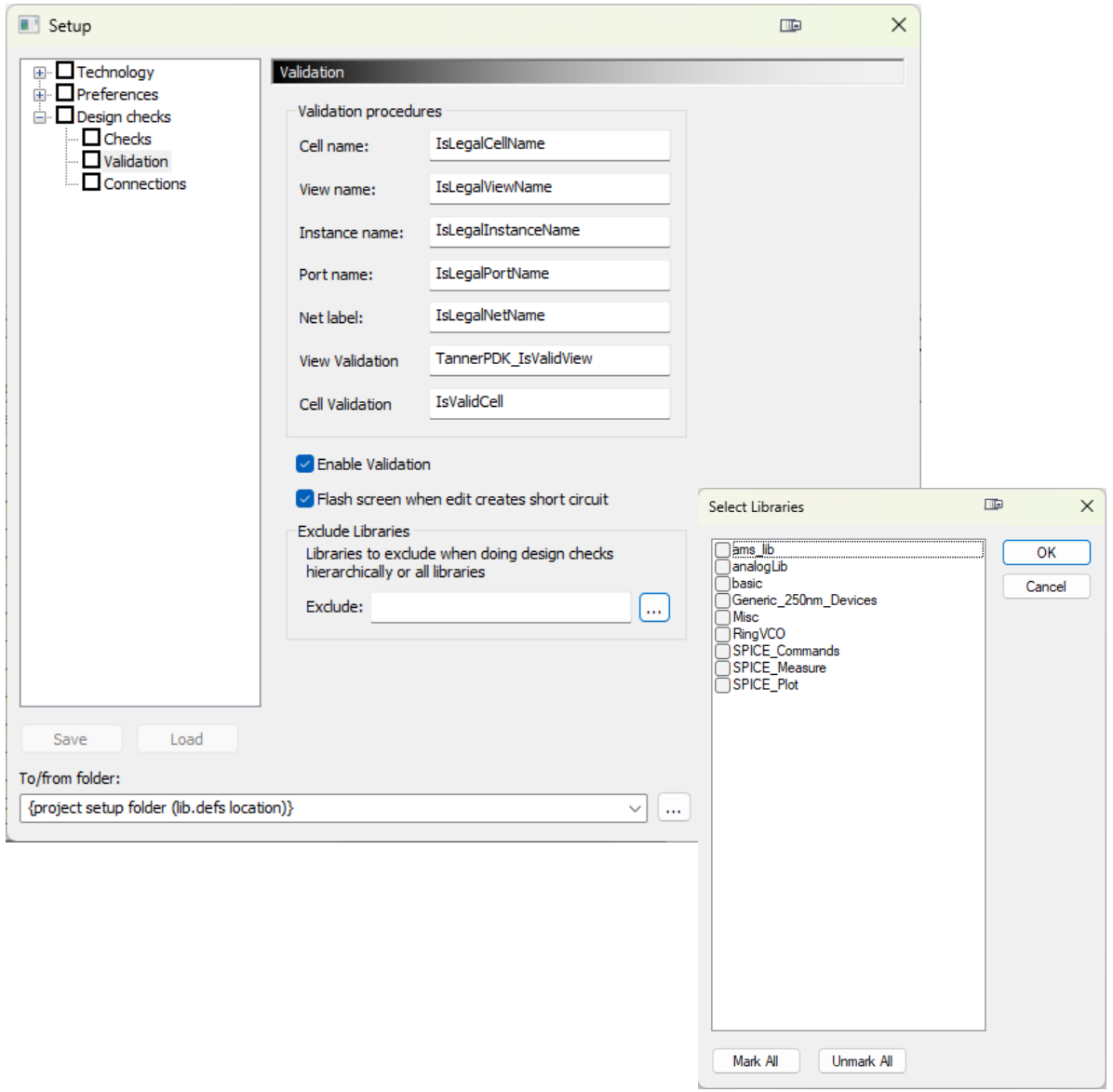
Added Libraries to Exclude for Design Checks

- Added a field to provide a list of libraries to exclude from validation to **Setup>Design Checks>Validation**



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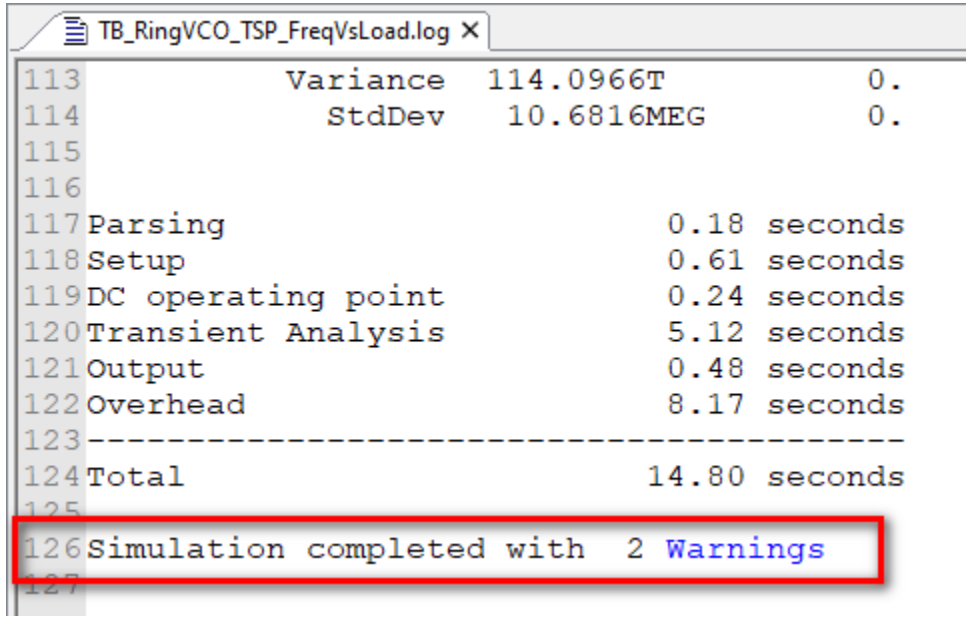
S-Edit TSP Simulation Log Always Contains Warning/Error Summary

- 'Simulation completed with <n> warnings ...' message is now always displayed in the S-Edit log
- TCL command command displays the summary information for the simulation:
  - `tsp log -log {path/filename} -summary`



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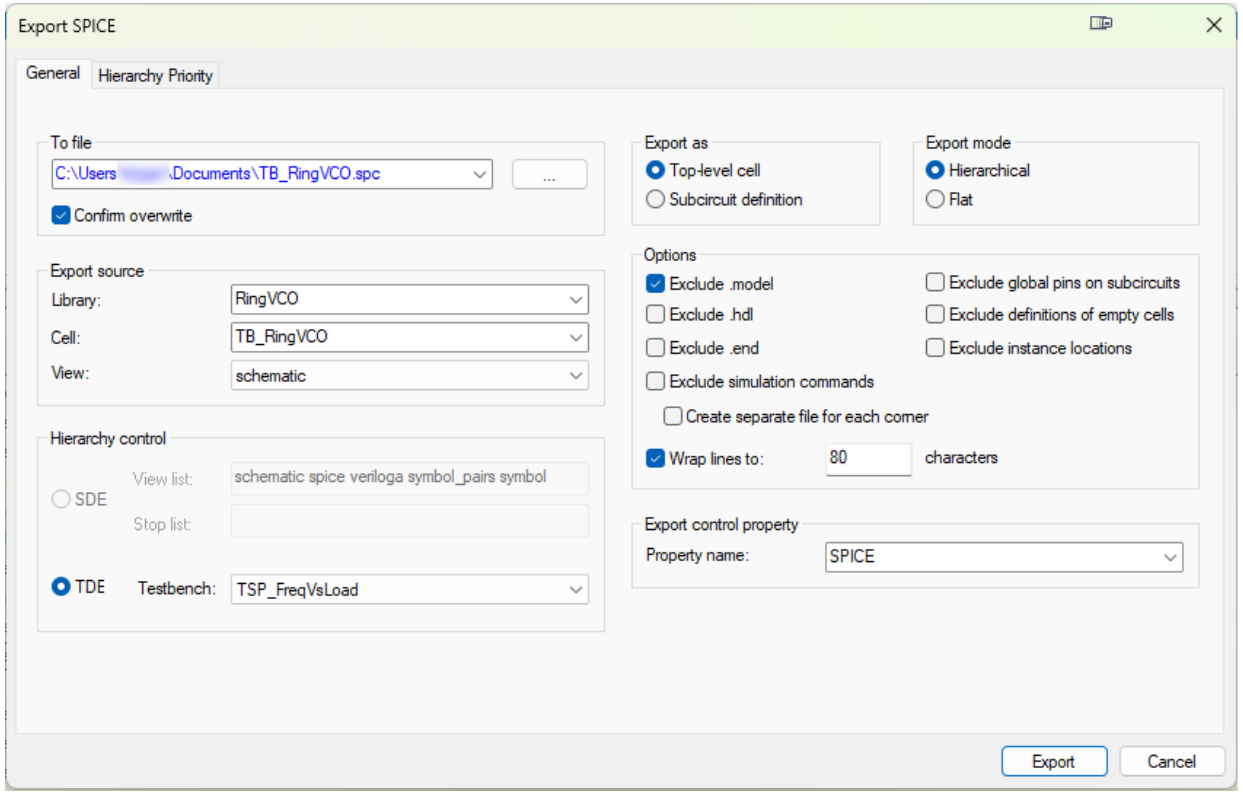
S-Edit Export SPICE/Spectre Dialogs Modified

- Changed aspect ratio of **File > Export > SPICE/Spectre** dialog to better fit on small displays



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S-Edit CDL Import

- CDL Import now supports the $PINS comment syntax for specifying pin assignment

```
Xyyy < n1 n2 … > < / > <subname> < parnam = pval > … <M=m>
+ <$[mname] | $.MODEL=mname> <$T=tx ty r a>
+ <$X=x> <$Y=y> <$D=d> <$PINS <pin=node> … >
```

- Example:

```
XNOR2_1 NOR2 $PINS Z=N_7 B=N_2 A=N_1 vss!=VssD vdd!=VddD
```

ESI

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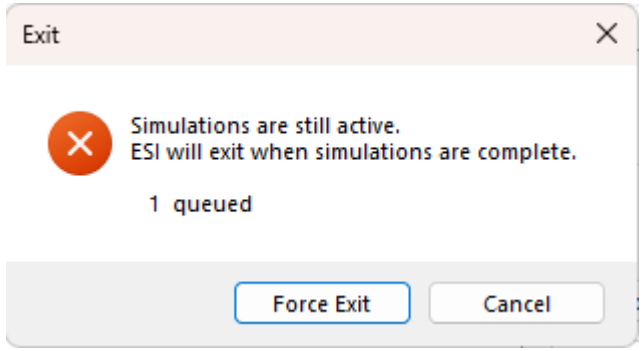
ESI Close Warning when External Simulator is Running

- When ESI <Exit> is performed, if there are any running, stopping, or post-processing simulations, then a dialog box is displayed providing the opportunity to continue with exit, cancel exit, or wait for ESI to automatically terminate when the simulations complete
- Gives user a chance to proceed or cancel



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T-Spice

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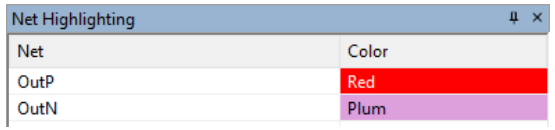
Linux Performance Improvements

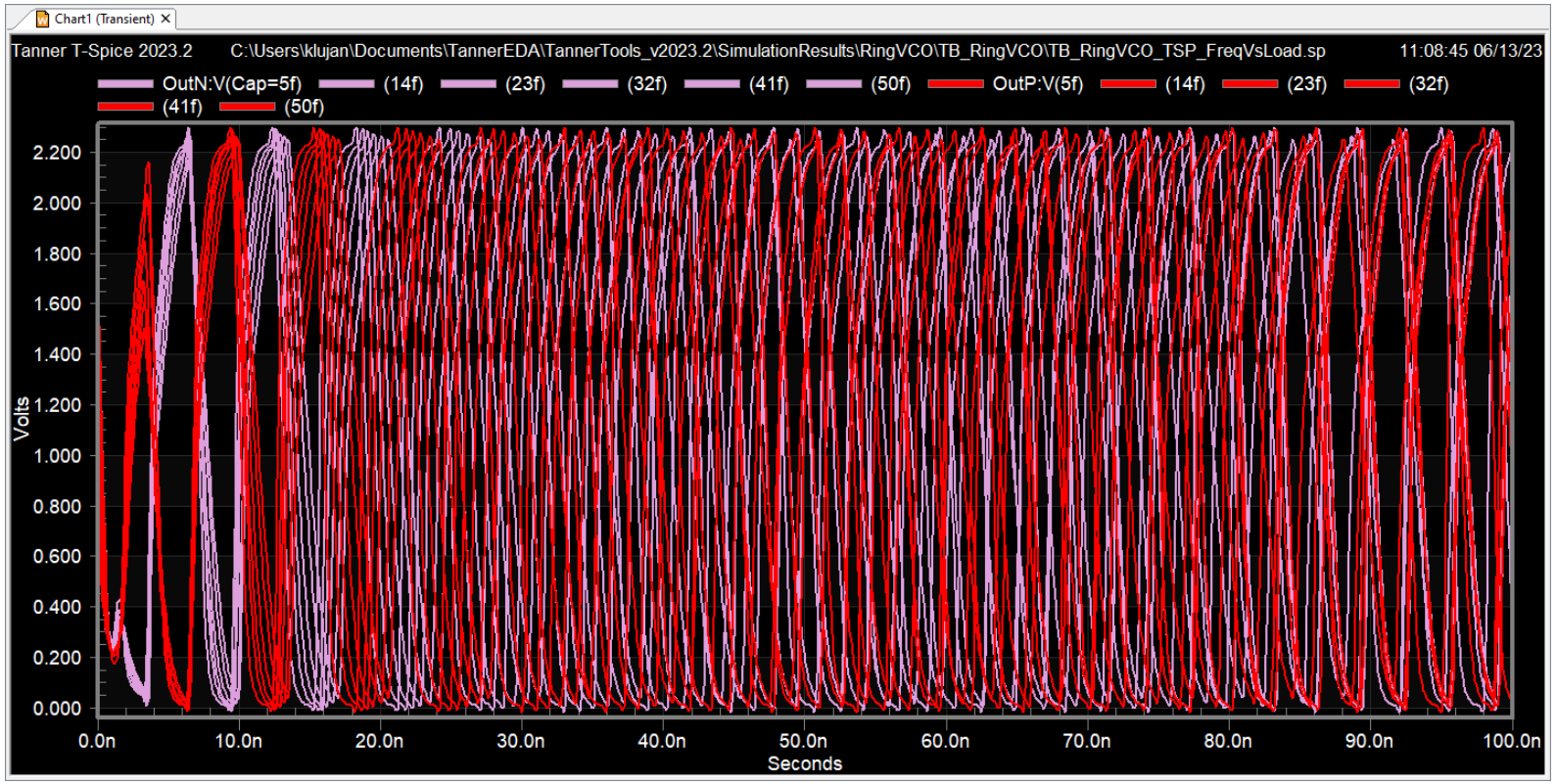
- T-Spice simulation performance has been improved on Linux, especially for temperature and parameter sweeps
- T-Spice has improved multi-threaded performance on Linux up to 1.4x faster

Waveform Viewer

Colored Voltage Probing

- Voltage probing from S-Edit to either Waveform Viewer or EZWave will now color the Net in S-Edit and the waveform the same color
  - Changing the color of the Net will also subsequently change the color of the waveform





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L-Edit

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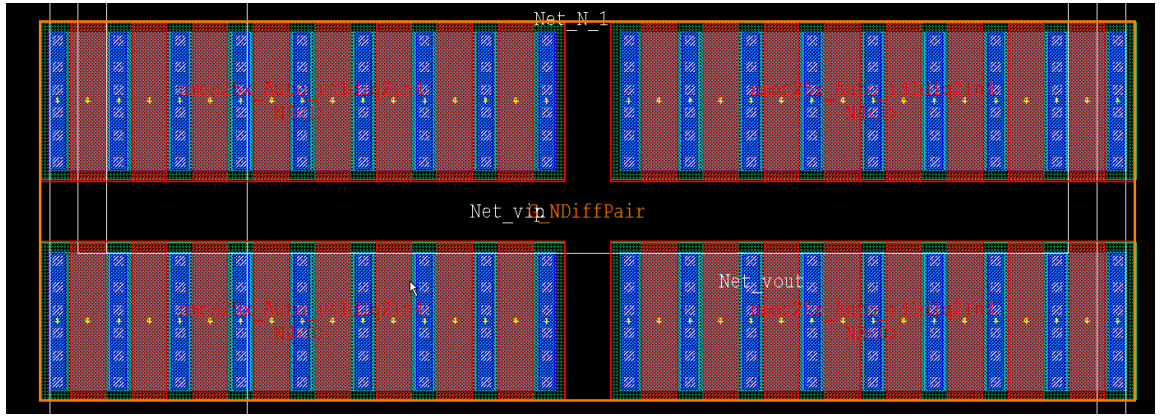
L-Edit Groups

- Designed to keep related objects bound together and organized in the layout cell view
  - Similar to instance grouping but without creating any hierarchy or links
  - No “references” can be made to groups
- Does not affect GDS export (objects in groups are exported to GDS without their group association)
- When moved (copied, deleted, etc.), all the objects in the group are moved (copied, deleted, etc.)
- Groups can contain any type of object: drawn shapes, labels, rulers, electrical ports, instances, and vias
- Groups make selection and replication of multiple objects easier

Selection Manager

Check	Type	Object	Instance of	Group	Layer	Net	#
☐	**G_NDiffPair**	**Group**		**G_NDiffPair**			**1**
☐	Dev_N3	Group		G_NDiffPair\Dev_N3			1
☐	**Instan...**	**N3<1>**	**OpAmp/nmos25x_Auto...**	**G_NDiffPair\Dev_N3**			**1**
☐	Instance	N3<0>	OpAmp/nmos25x_Auto...	G_NDiffPair\Dev_N3			1
☐	Dev_N4	Group		G_NDiffPair\Dev_N4			1
☐	Instance	N4<1>	OpAmp/nmos25x_Auto...	G_NDiffPair\Dev_N4			1
☐	Instance	N4<0>	OpAmp/nmos25x_Auto...	G_NDiffPair\Dev_N4			1



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Updated Terminology

2022.2 and Earlier

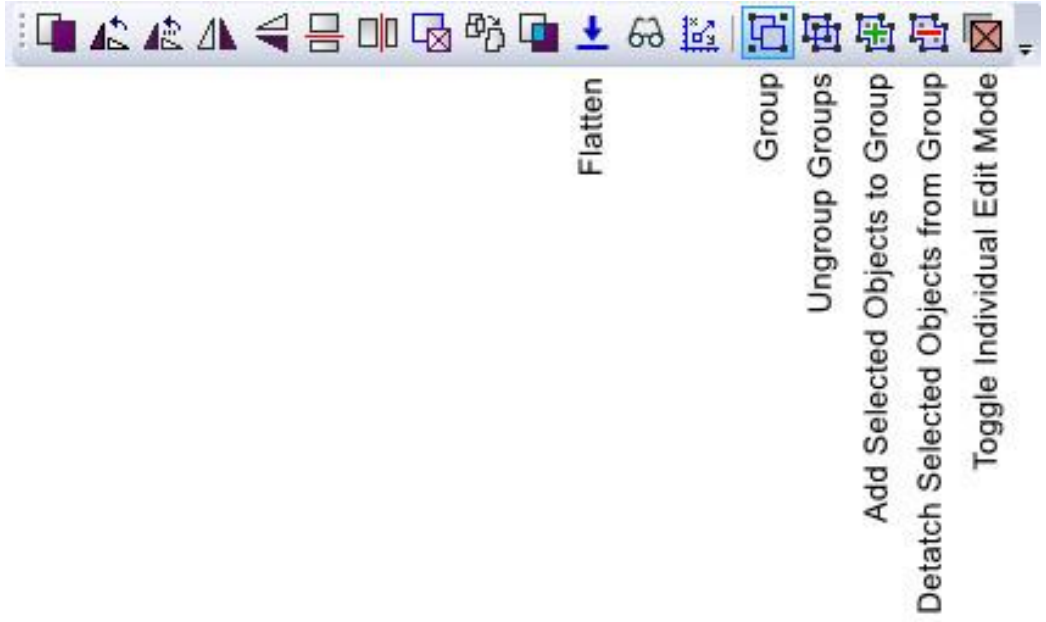
Term	Definition
Group	Created a new cell view from selected objects and instanced cell view in location in replacement of objects selected
Ungroup	Flattened selected instances one level at a time
Flatten	Flattened all levels of entire cell view

2023.2 and Later

Term	Definition
Group	Draw>Group provides dialog to choose to create a cell, create a group, or create an instance array (if instances are in array configuration) Group alone now refers to the new L-Edit group feature
Ungroup	Moves object and nested groups from a group up one level (does not work on instances)
Flatten	Provides dialog to flatten instances one level, multiple levels, or all levels. Does not affect groups.

NOTE: The new default bindkeys are CTRL+U for flatten and SHIFT+U for ungroup groups.
Users should assign the new default bindkeys under **Setup>Application-Keyboard** tab in the Draw and Group Utilities Category.

Editing Groups



- Users can edit groups using two methods
  - Edit in-Place
    - Used in Groups just like is currently used for Instances or Ports
  - Individual Edit Mode (New)
    - All objects of groups will be selectable and editable directly as if they are not part of a group
    - In “Individual Edit Mode” objects in groups may be operated on (moved, edited, deleted, Etc.) directly, without having to push into the group

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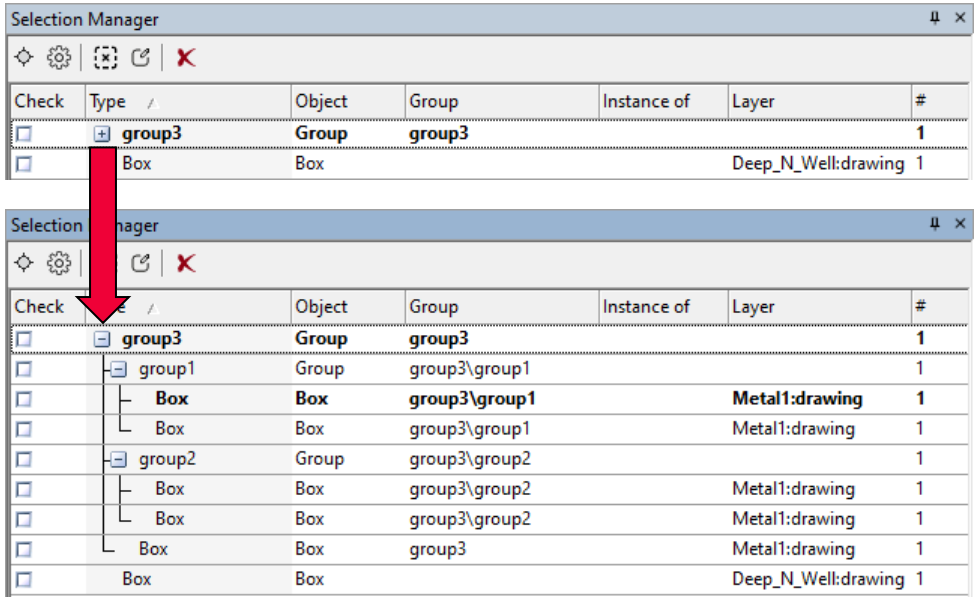
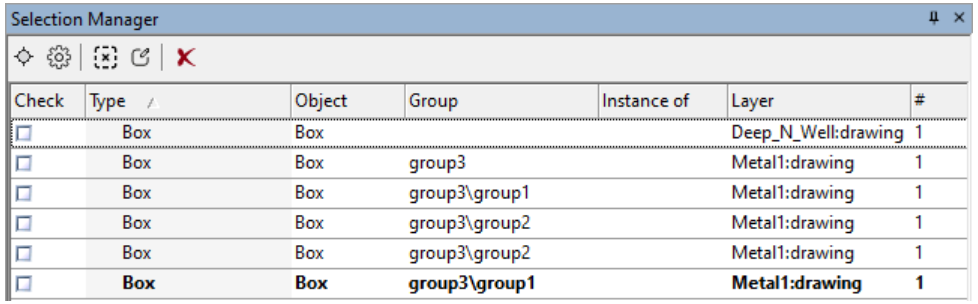
Selection Manager Display of Group Membership

- Selection Manager has been enhanced to show group membership
- With Individual Edit Mode (IEM) off, groups are shown as a tree, whereas with IEM on, groups are shown as a list.

IEM Off



IEM On



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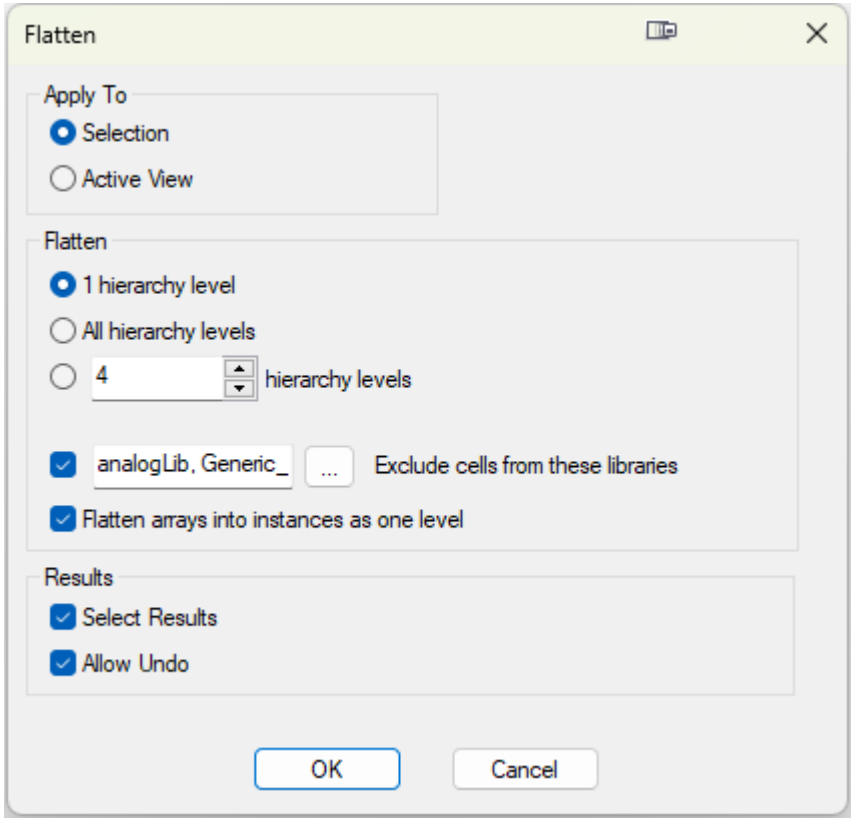
New Groups UPI Commands

- New UPI functions are available to create, move, delete, and perform a variety of operations on groups
- To avoid confusion with our previous use of the term group/ungroup for creating cells and flattening cell hierarchy, the following UPI commands have been marked as legacy and will no longer run unless `#define EXCLUDE_LEDIT_LEGACY_UPI` is commented out. The new replacement command with more appropriate naming is shown in parenthesis below:
  - `LSelection_Group (LSelection_CreateCell)`
  - `LSelection_UnGroup (LSelection_Flatten_Ex22)`
  - `LSelection_Flatten (LSelection_Flatten_Ex22)`
  - `LC_Ungroup (LC_FlattenOneLevel)`
  - `LInstance_Ungroup (LInstance_FlattenOneLevel)`
  - `LCell_Flatten (LCell_Flatten_Ex22)`
- Legacy commands cannot be run via Tcl/python

Enhanced Instance Flatten Dialog

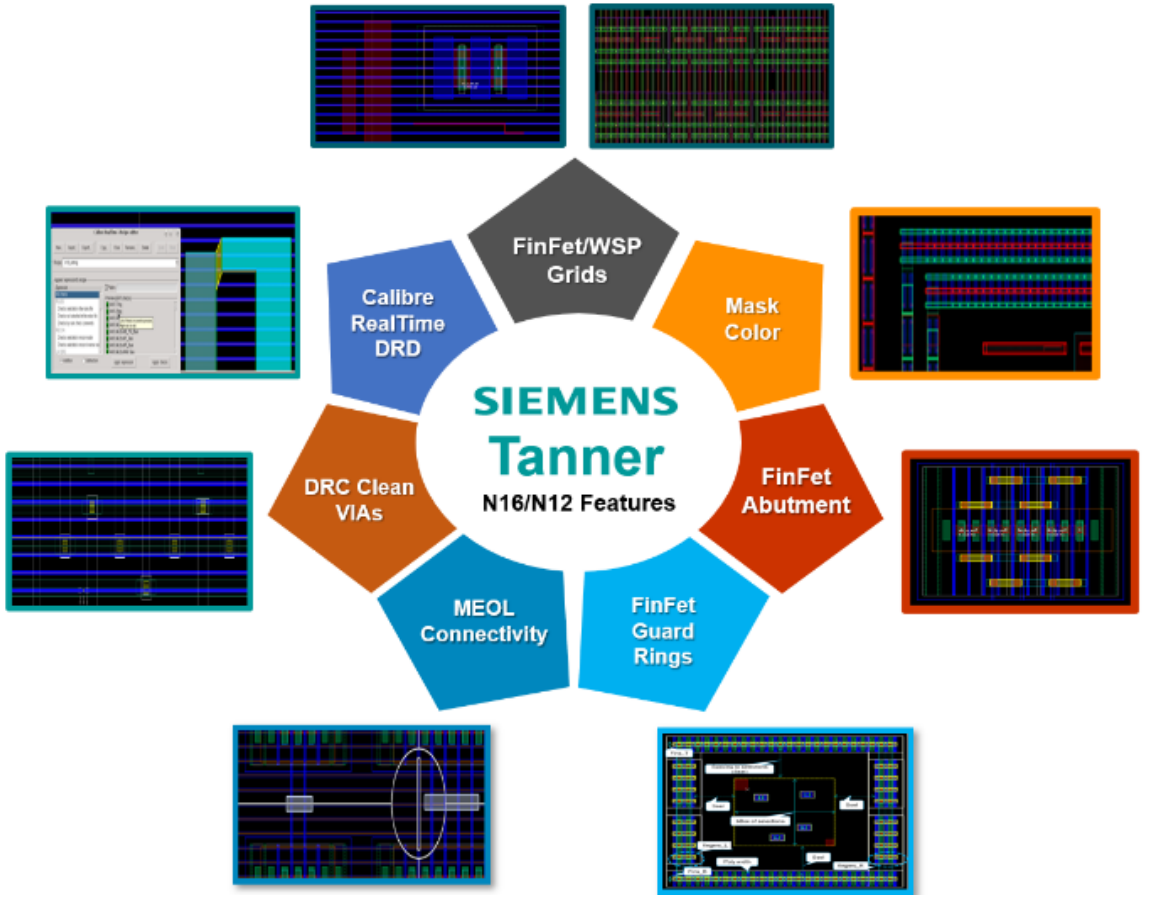
- **Draw>Flatten** (CTRL+U) or via the Editing Toolbar Flatten icon
- Enhanced with more features to work on Instances (not groups)
  - Flatten to a specified level of hierarchy
  - Flatten selections or active view
  - Exclude cells from specified libraries from flattening
  - Performance improvements when disabled
    - Allow undo
    - Select results
  - Note: Objects in instance hierarchy that are in a group will remain in the group after flattening



SIEMENS

L-Edit Advanced Node Features

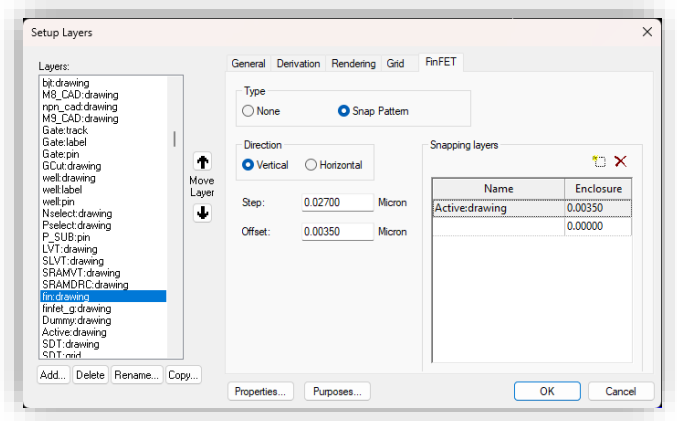
- Foundries have imposed a restricted design methodology for 16nm and below to mitigate the complexity of design rules
- L-Edit Advanced is a new product with advanced node features that support FinFET design
- The following L-Edit Advanced features improve FinFET designers' productivity
  - FinFET Grid
  - Auto-abutment
  - FinFET Guard Rings
  - Layout Coloring
  - Width Spacing Pattern (WSP)

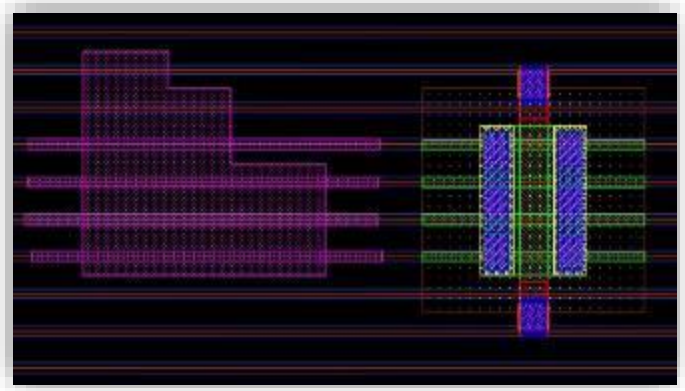


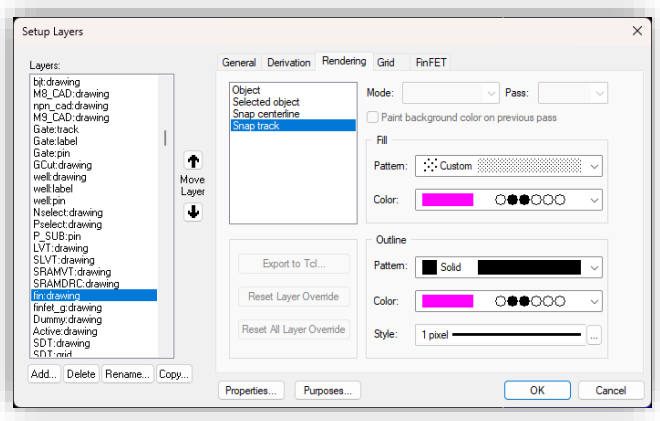
SIEMENS

FinFET Grid

- The restrictive rules for Diffusion and Fin layers in FinFET technologies lead to the usage of FinFET Grid
- FinFET Grid setup is included in Tanner iPDK of FinFET technologies
- Setup Layers Dialog has been enhanced with a new FinFET tab to visualize the FinFET Grid setup and create Poly grids for different Poly pitches
- Geometries on Diffusion and Fin layers as well as PCells and hierarchal blocks including these layers should snap to the FinFET Grid in order to avoid violations of Diffusion and Fin layers DRC rules
- Editing and Alignment commands have been enhanced to support FinFET grid snapping of geometries and hierarchal instances
- FinFET Grid rendering can be customized in the Rendering tab of Setup Layers dialog



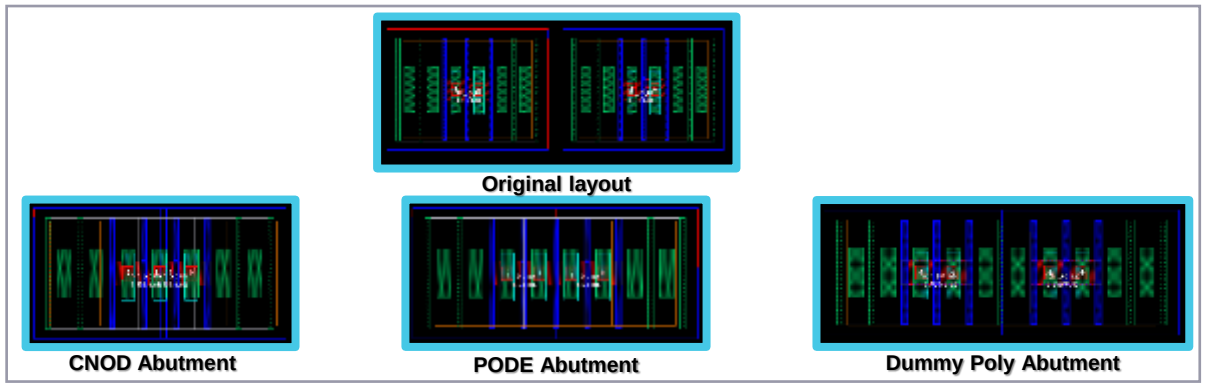


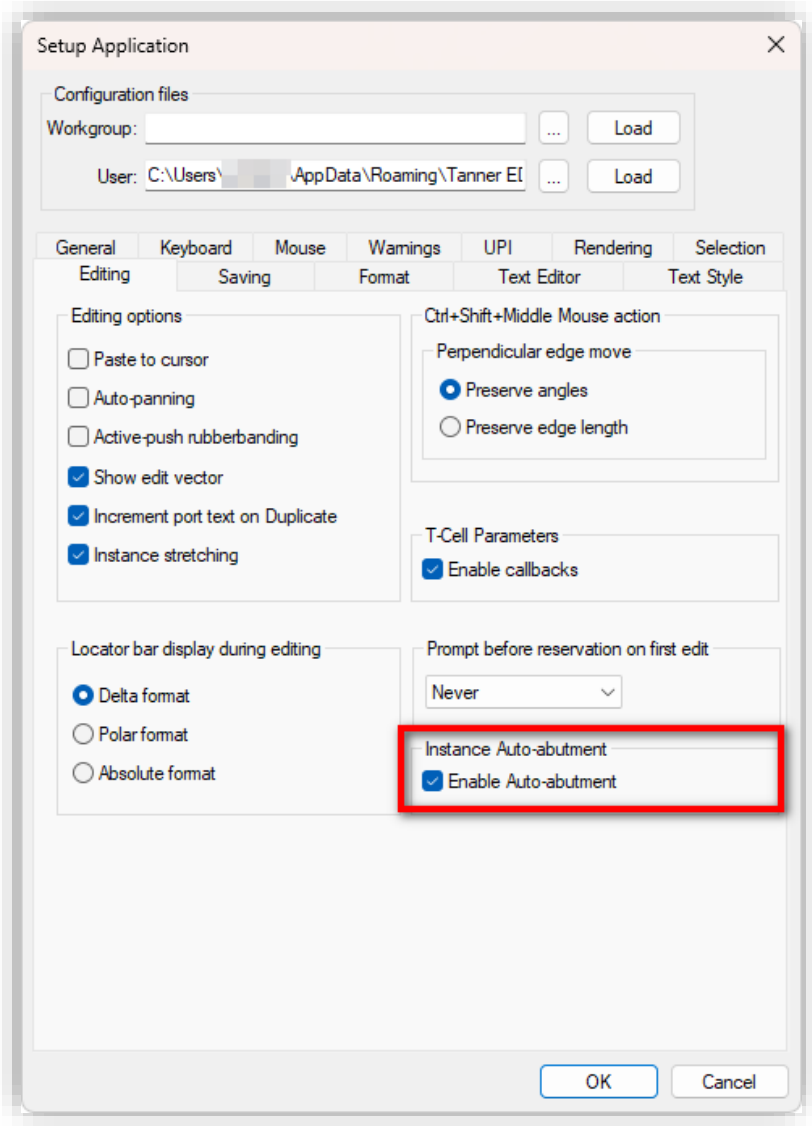


SIEMENS

Auto-abutment

- Continuous Diffusion helps to reduce Layout dependent effects in FinFET Design
- Auto-abutment ensures the continuity of Diffusion and generates DRC clean abutted instances
- New Enable Auto-abutment checkbox in the Editing tab of **Setup>Application** dialog enables Auto-abutment of connected instances
- Supports Foundry abutment procedure and options

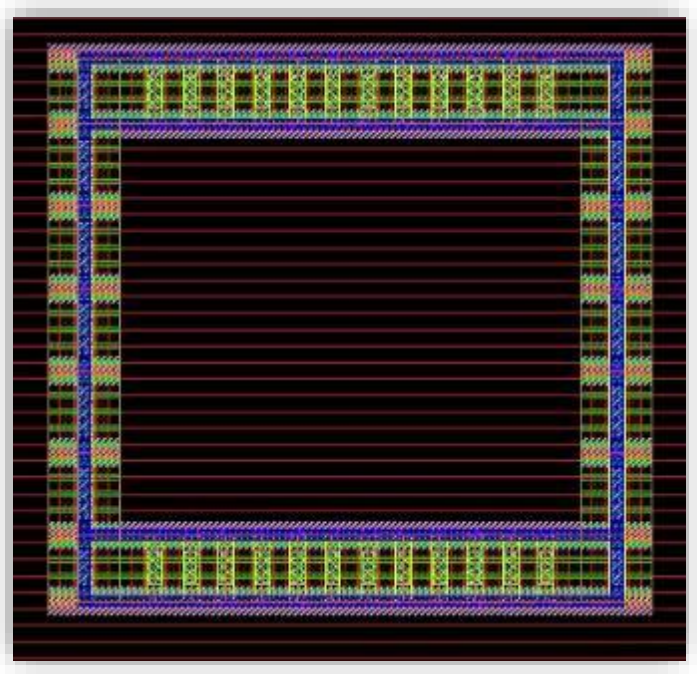


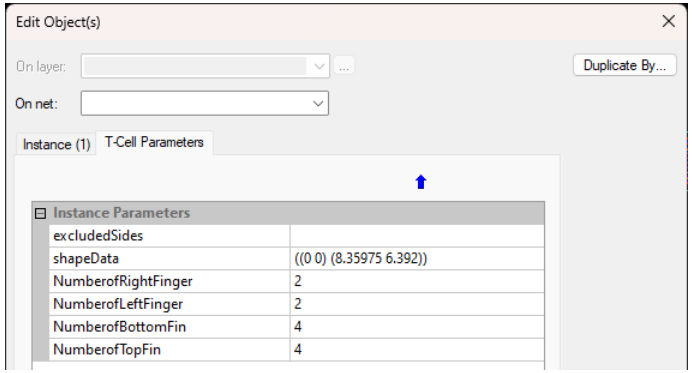


SIEMENS

FinFET Guard Rings

- FinFET Guard rings have MOSFET’s like structure including Poly, Diffusion and all MEOL and cut layers
- The Diffusion ring may not be continuous in FinFET Guard ring
- L-Edit generated FinFET guard rings are DRC clean and snap to FinFET grid automatically
- The Guard ring instance is parametrized and customized based on Foundry technology
- New commands under **Draw>Guard Rings** to chop and heal guard rings

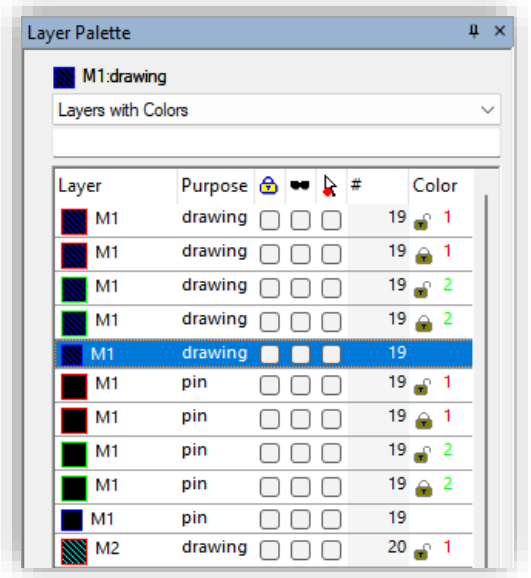


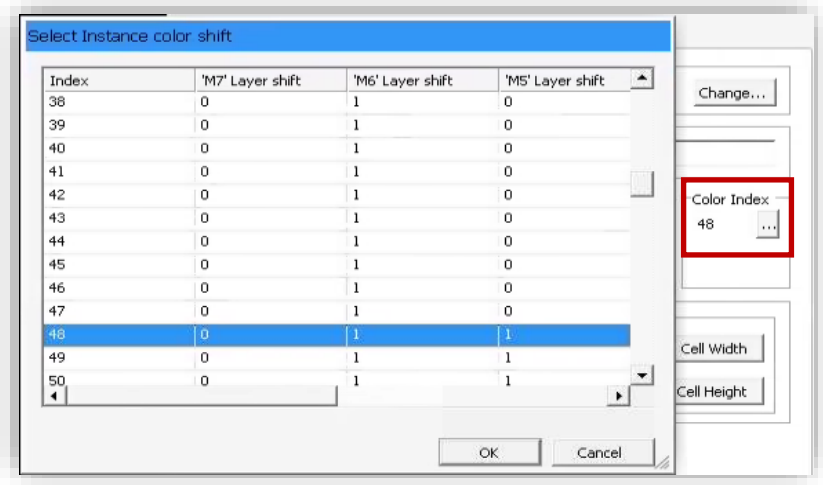


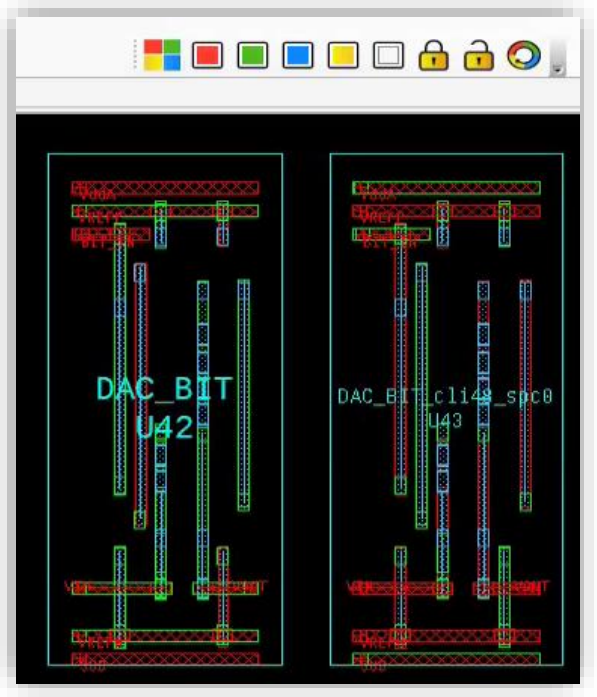
SIEMENS

Layout Coloring

- FinFET technologies require layout coloring to be divided between two different masks on the same metal layer
- Layout rendering has been enhanced to show the colors of geometries in layout
- Designers can handle the coloring by:
  - Selecting a mask color from the Layer Palette and draw geometries on it
  - Using the Mask Color Toolbar to assign colors to geometries or change their colors
  - Using the color index option to shift color for a specific instance



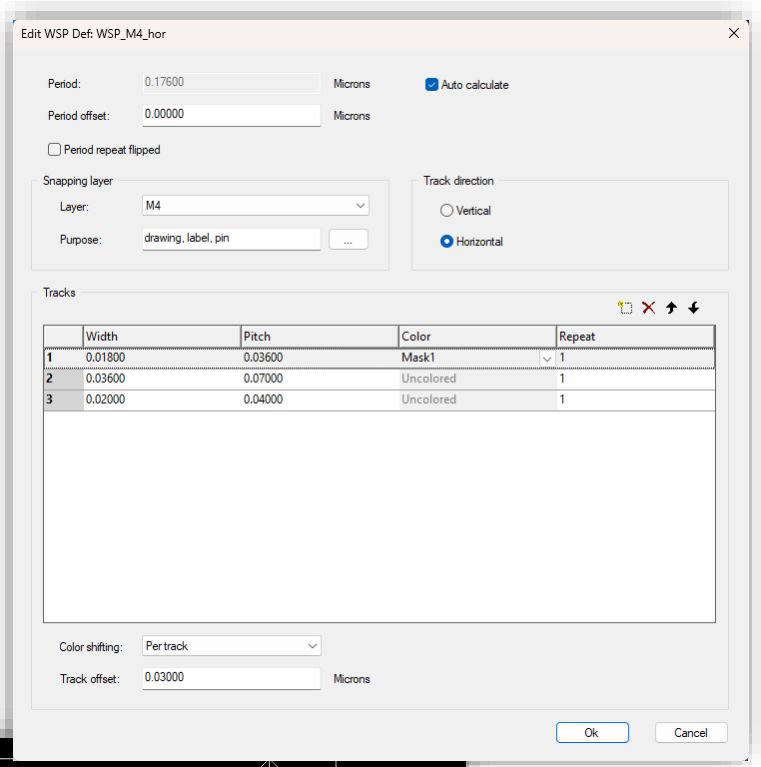


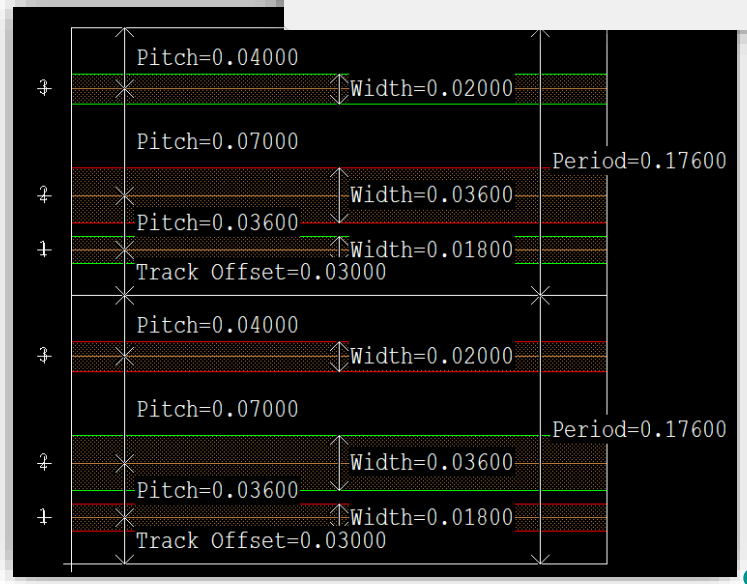


SIEMENS

WSP Defs

- The routing in FinFET technologies is restricted by many rules of discrete values of width-pitch pairs allowed in each routing direction
- WSP helps to define the routing tracks for Metal layers with respect to metal routing rules
- WSP feature allows the users to:
  - Create and edit WSP Defs
  - Open WSP Preview to visualize the tracks graphically
  - Generate a layout from a WSP Def in order to check DRC compliance or alignment of WSP tracks on Placement patterns
  - Generate or update an existing WSP Def from a selected Layout
  - Export WSP Defs to a CSV for reuse in another project
  - Import WSP Defs from a CSV file
  - Copy, rename or delete WSP Defs

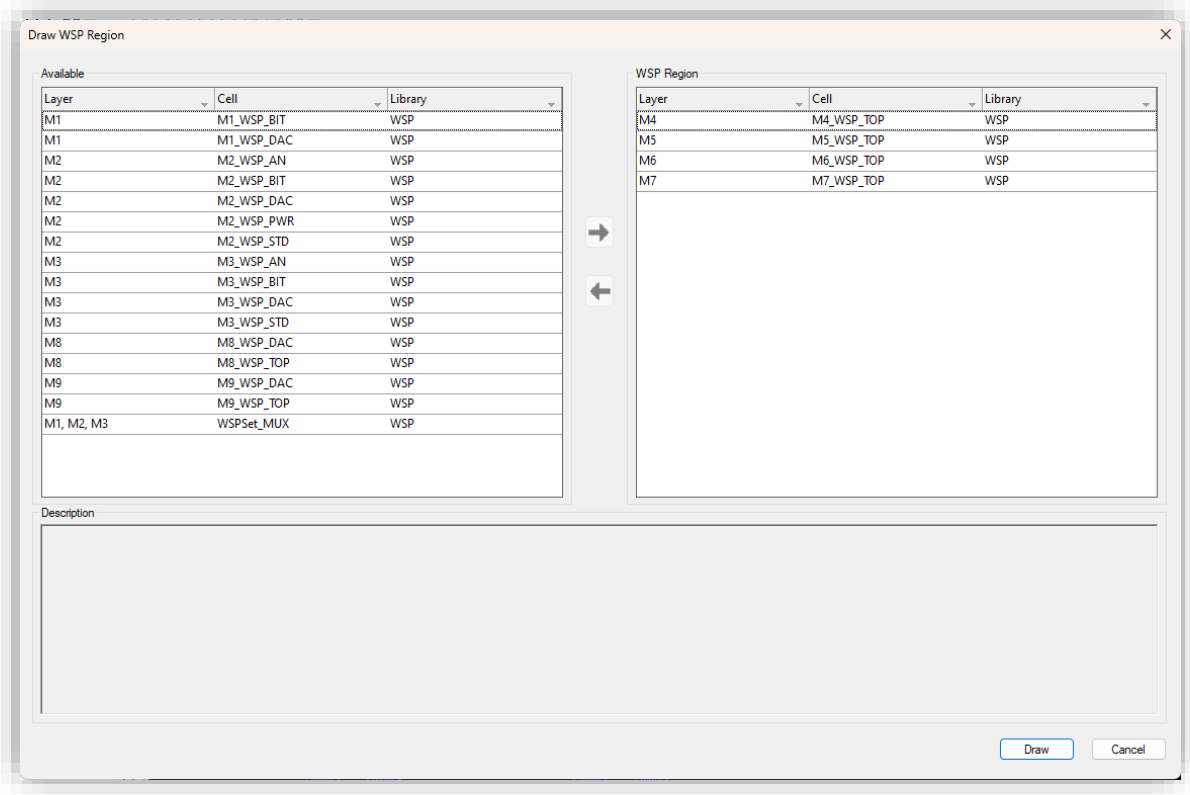




SIEMENS

WSP Region/ WSP Set

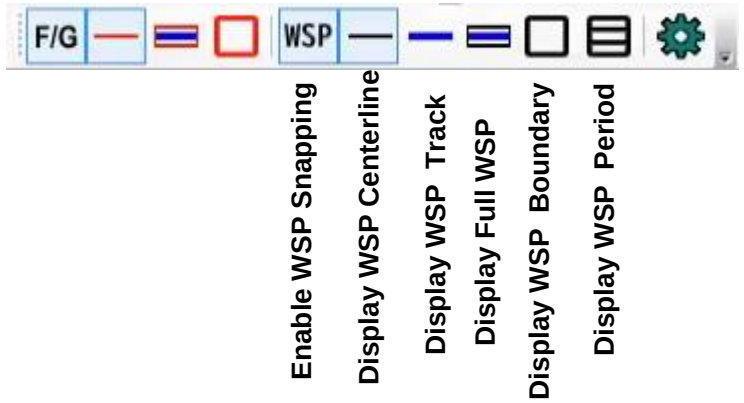
- Designers need to use many metal layers to route their layout
- **Draw>Draw WSP Region** allows users to define the routing tracks of many metal layers in the same region by selecting WSP Defs to apply to that region
- The regularity of metal density across the design impose the application of the same collection of WSP Defs in many design regions
- **Setup>WSP>New WSP Set** allows to group many WSP Defs that are intended to be used together into a WSP Set and save it permanently in the design database for reuse
- The user can edit, copy, rename or delete WSP Sets

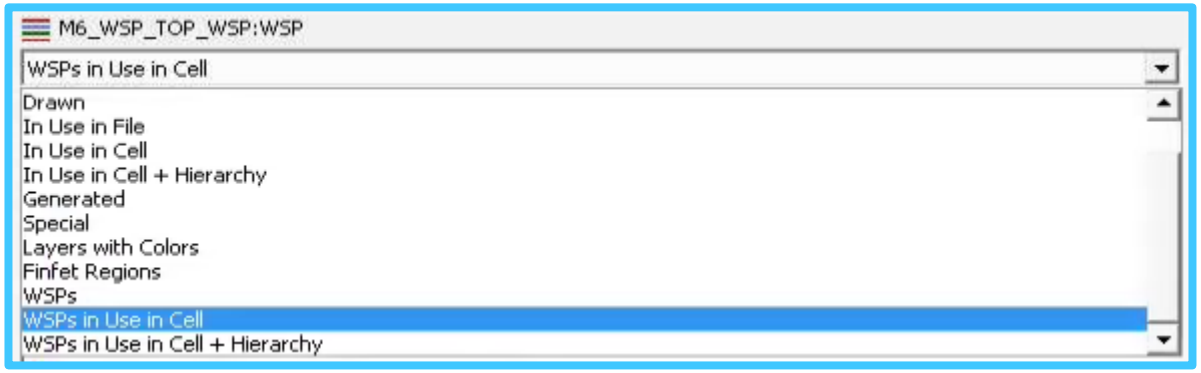


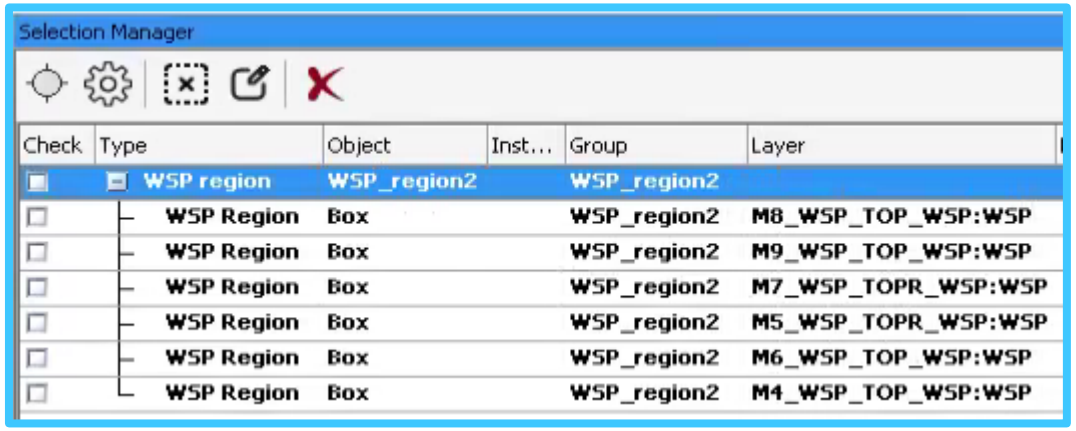
SIEMENS

WSP Region

- Metal routing snaps to their corresponding WSP tracks inside a WSP region
- The user can control WSP Display options using the FinFET grid toolbar
- Layer Palette has been enhanced with WSPs filters and layer operations that control the visibility and protection of WSP Layers
- WSP Regions are saved as groups in the design and the Selection Manager has been enhanced to recognize WSP Regions and their memberships





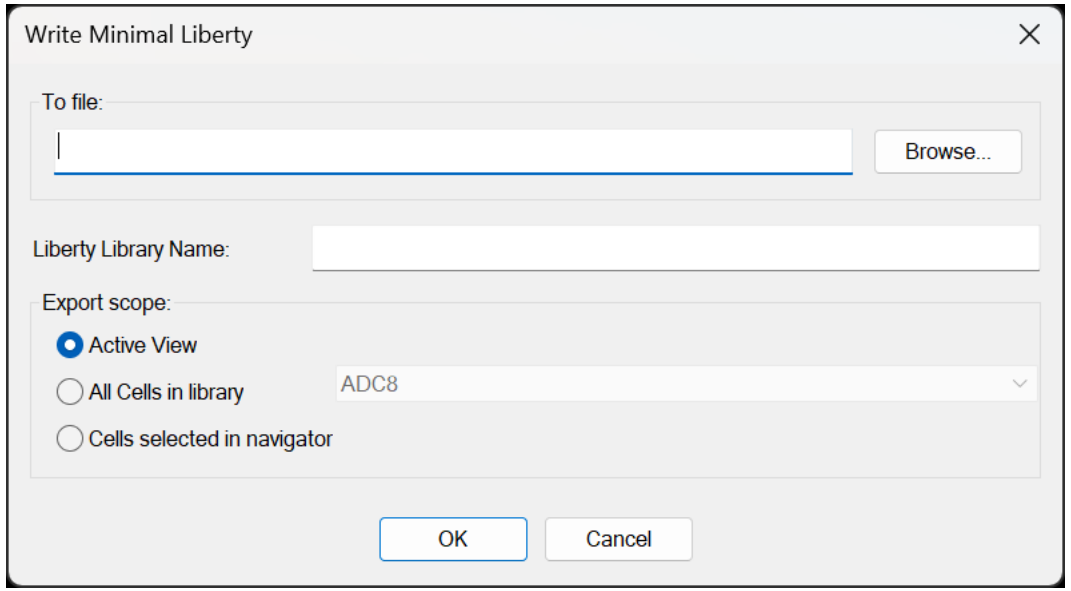


SIEMENS

LEF/DEF Features – Export Minimal Liberty

- **Tools>SDL Navigator>LEF/DEF>Write Minimal Liberty…** or SDL navigator drop down menu **>LEF/DEF>Write Minimal Liberty…**
- Generates a minimal liberty file compatible with PnR tools such as Aprisa and Nitro
- Streamlined liberty file includes the liberty library name and essential cell information
  - For each cell, it only contains area and pin info
  - For pins, it only contains direction
  - Does not contain timing, power, and other data

```
library (RingVCO) {
        cell (DiffCell) {
                area : 160.004;
                pin(Vdd) {
                        direction : inout;
                }
                pin(Vss) {
                        direction : inout;
                }
                pin(VTune) {
                        direction : input;
                }
                pin(Vb1) {
                        direction : input;
                }
                pin(Vb2) {
                        direction : input;
                }
                ......
        }
}
```



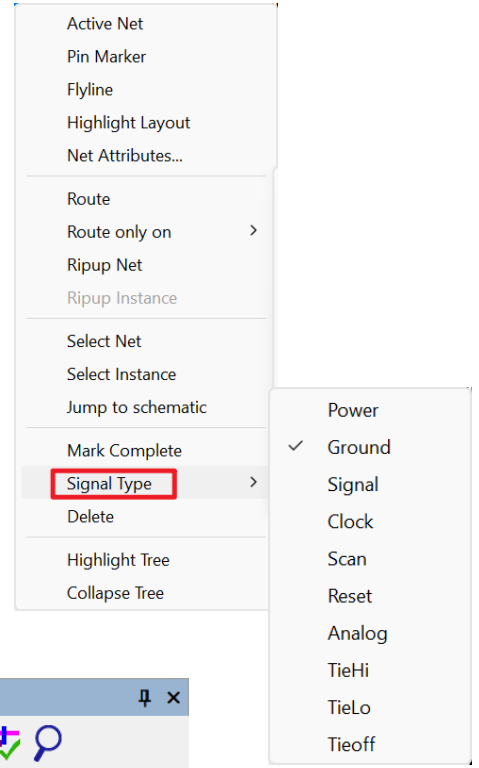
SIEMENS

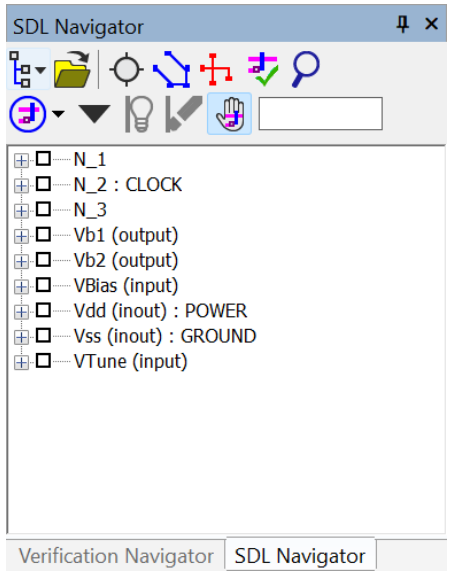
LEF/DEF Features – Set Net Signal Types

- Enhanced signal types to assign for nets (other than Power)
- Assists in generating accurate LEF output
  - If a net name includes **vdd**, it is exported as a **Power** net in the LEF
  - Similarly, if a net name contains **gnd** it is exported as a **Ground** net in the LEF

```
PIN vss!
   DIRECTION INOUT ;
   USE GROUND ;
   PORT
     LAYER Metal1 ;
        RECT 0 0 8.05 0.8 ;
   END
END vss!
```

- SDL Navigator net display has been enhanced by incorporating pin directions and net signal types for improved clarity and understanding

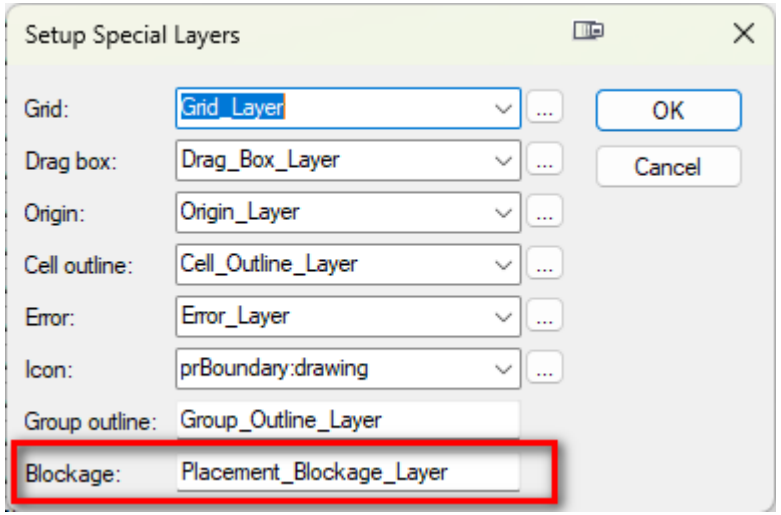




SIEMENS

LEF/DEF Features – Export Placement Blockage

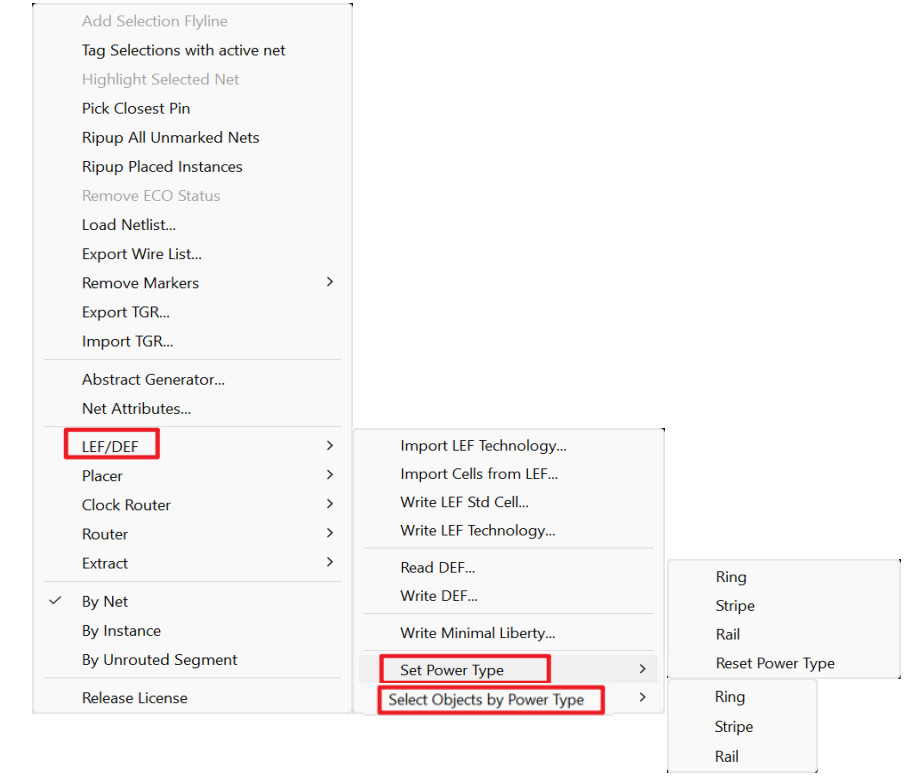
- L-Edit can export DEF for routing obstructions (but not for placement obstructions)
  - This allows users to generate placement blockages in floorplan layout view
- In **Setup>Special Layers…** dialog, a new blockage layer has been created with the default name *Placement_Blockage_Layer*
- Users can customize this name as desired
  - Keeping default name will not modify technology as the layer solely exists in L-Edit's memory and will not be stored in OA
  - Assigning a custom name to the layer will be saved in the Tech.tdb file

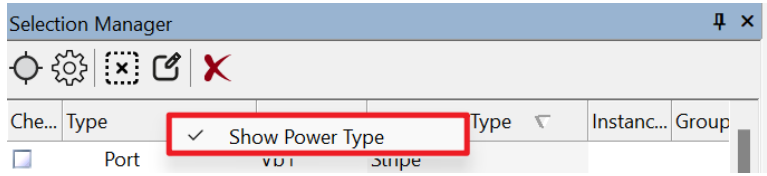


SIEMENS

LEF/DEF Features – Export Power Plan with Layout

- A new feature enables users to create patterns for power rings, power stripes, and power rails in the floorplan layout view, designate them with the appropriate types, and export them with the correct syntax in DEF format, providing a seamless workflow
- Several new options have been added under **Tools>SDL Navigator>LEF/DEF>** as well as in the **SDL Navigator dropdown menu LEF/DEF>**
  - **Set Power Type** assigns power types to selected objects within the active layout view
  - **Select Objects by Power Type** enables users to select objects based on their power type, allowing for quick assignment to another type or resetting of their current power type as needed
- Selection Manager has an added option to Set Power Type
  - Add the **DEF Power Type** column by RMB clicking the column header





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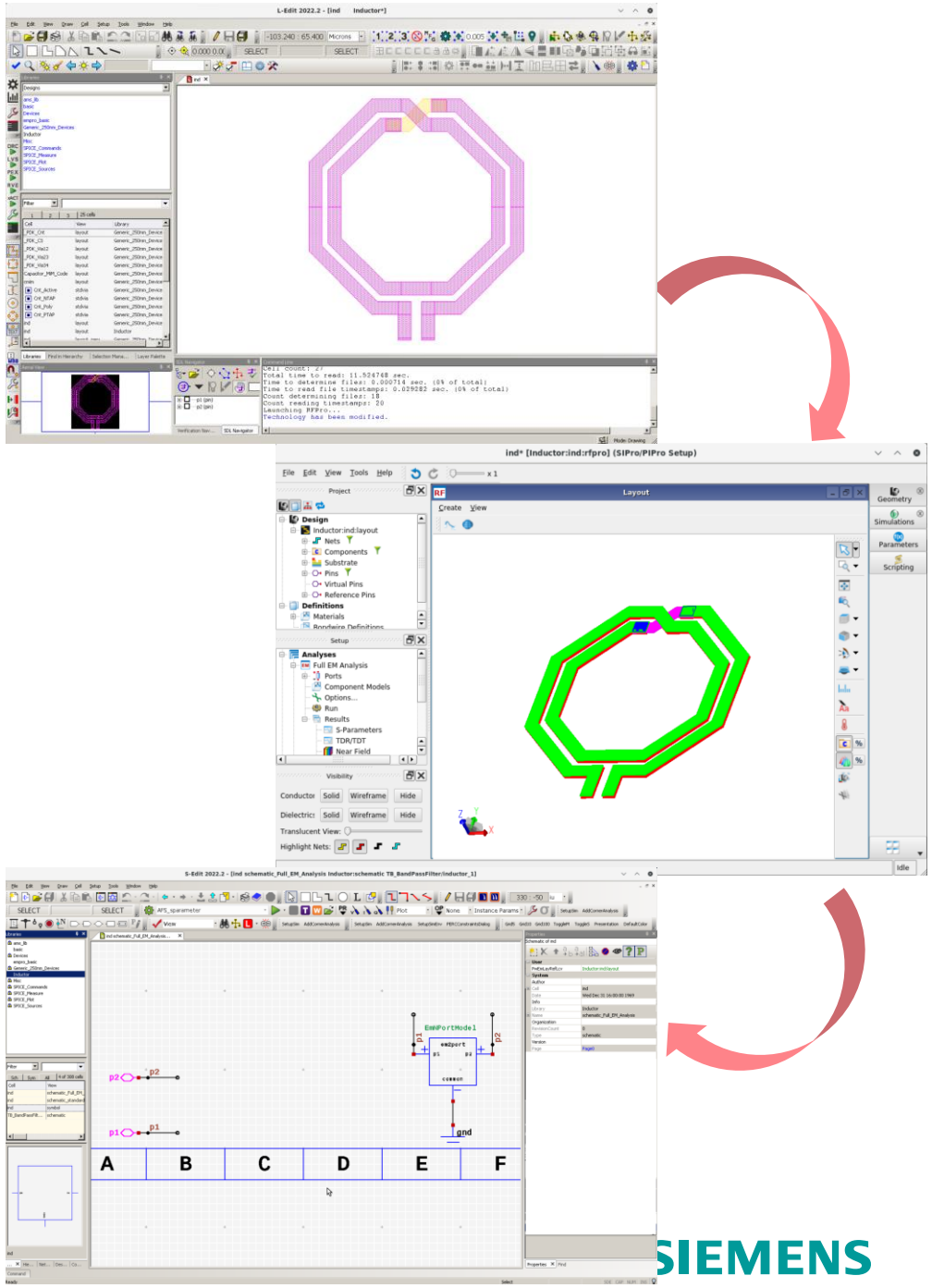
RFPro Integration with Tanner Tools

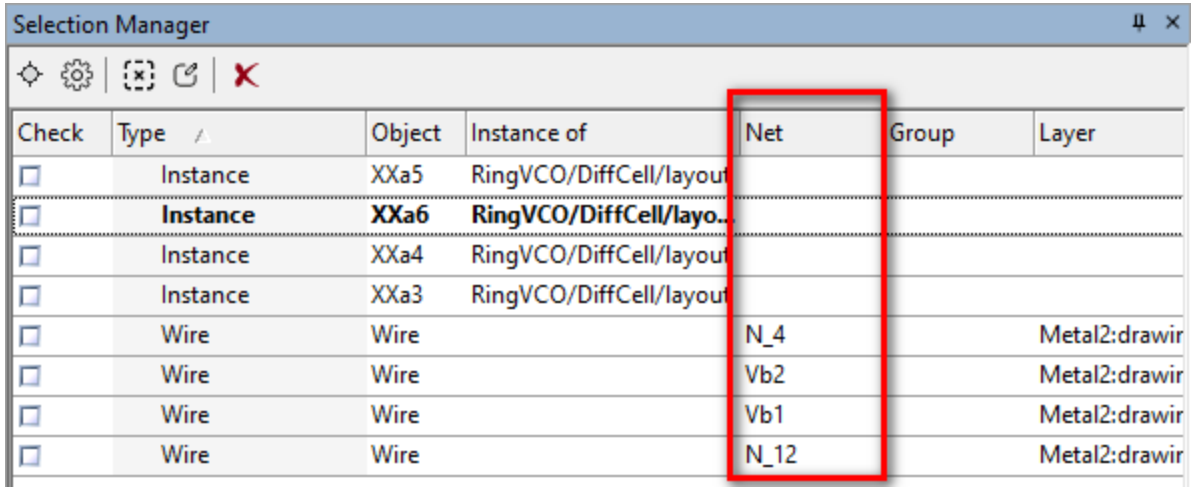
- RFPro, by Keysight, is an EM simulator
- RFPro generates S-Parameter models for discrete devices for RF simulation
- RFPro utilizes an OA layout view in L-Edit and a substrate file to generate a 3D structure of the layout
- EM analysis is conducted on the 3D structure to generate S-Parameters
- The S-Parameters are used to model the device and an OA subckt is generated to represent the S-Parameters in S-Edit
- Simulation can be performed using either AFS or Eldo



SIEMENS

Selection Manager Display of Net Names

- Selection Manager has been enhanced to show net names



SIEMENS

Improved AutoGen Cell Naming

- AutoGen names changed from ***<mastername>_Auto***_#_# to ***<mastername>_Auto_<md5 hash>***
- Using the previous naming convention, the same AutoGen could have different names under different conditions
- The new name ensures that AutoGen names are stable
- AutoGen names are normally hidden in the Library Navigator, but can be made visible via the Library Navigator **RMB Context Menu>Settings>Filters>Show Hidden Cells**

ShowInList Variable added to LLayerParamEx2022 UPI Structure

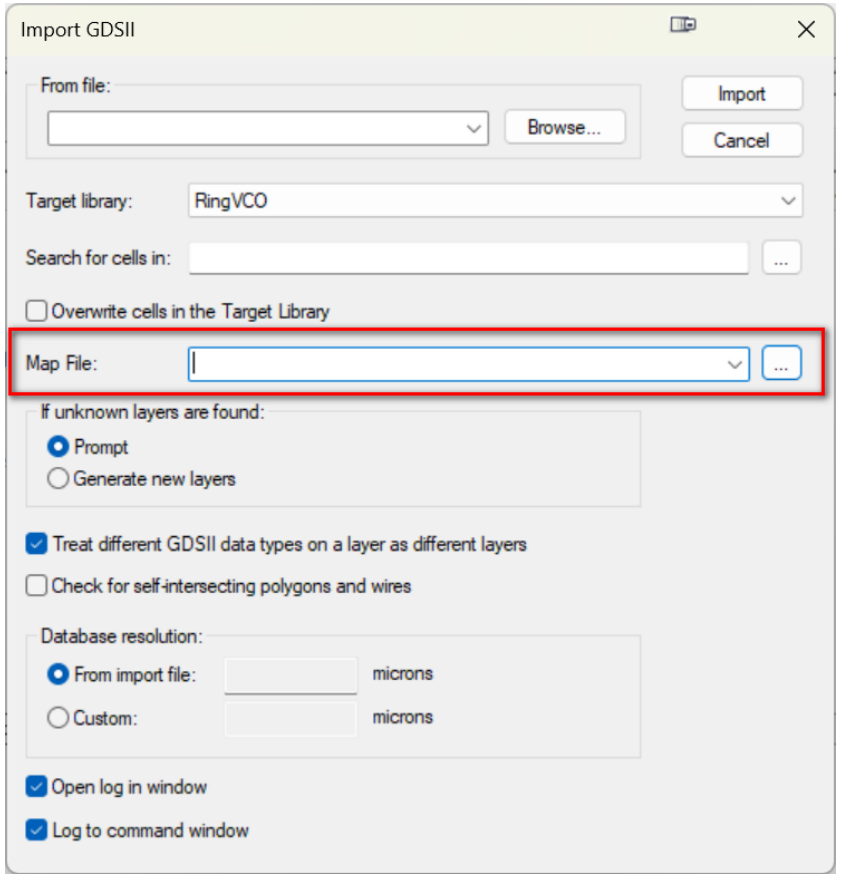
- **LLayerParamEx2022** structure used in new UPI functions **LLayer_SetParametersEx2022** and **LLayer_GetParametersEx2022** (similar to the earlier versions of those functions) now have an additional variable ***ShowInList***, which, when set to **LTRUE**, will set the layer as valid

Cellmap File for Resolving Conflicts in Calibre Results Probing

- In cases where there is same cellname in multiple libraries, or same cellname with multiple views, GDSII/OASIS export now names cells as ***<cellname>_<libname>_<viewname>*** rather than simply appending a digit on the cellname
  - ***<viewname>*** is omitted if the viewname is **layout**
- A cellmap file is also written on GDS export, both when GDSII/OASIS is explicitly exported via **File>Export Mask Data>GDSII…/OASIS…**, and also when GDSII/OASIS is written for Calibre
  - Calibre RVE will be able to use the cellmap file to resolve ambiguous cell names, starting in their 2023.4 release

GDS and OASIS Import Supports Layermap File

- GDS and OASIS import now support a layermap file



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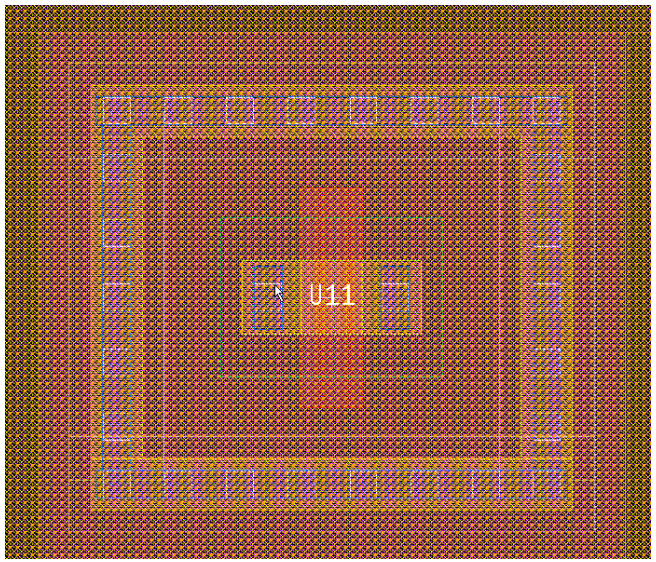
GDSII and OASIS Import/Export Automatic Layermap Discovery

- GDSII and OASIS import and export now automatically find a layermap file placed in the library folder
  - If the user types (or browses) to a file, it is used
  - If no file is specified, but a layermap file with name ***<libraryname>.cellmap*** is found in any of the libraries, it is used
  - If no file is specified, and no file is detected in any library, the GDS numbers in **Setup Layers** are used

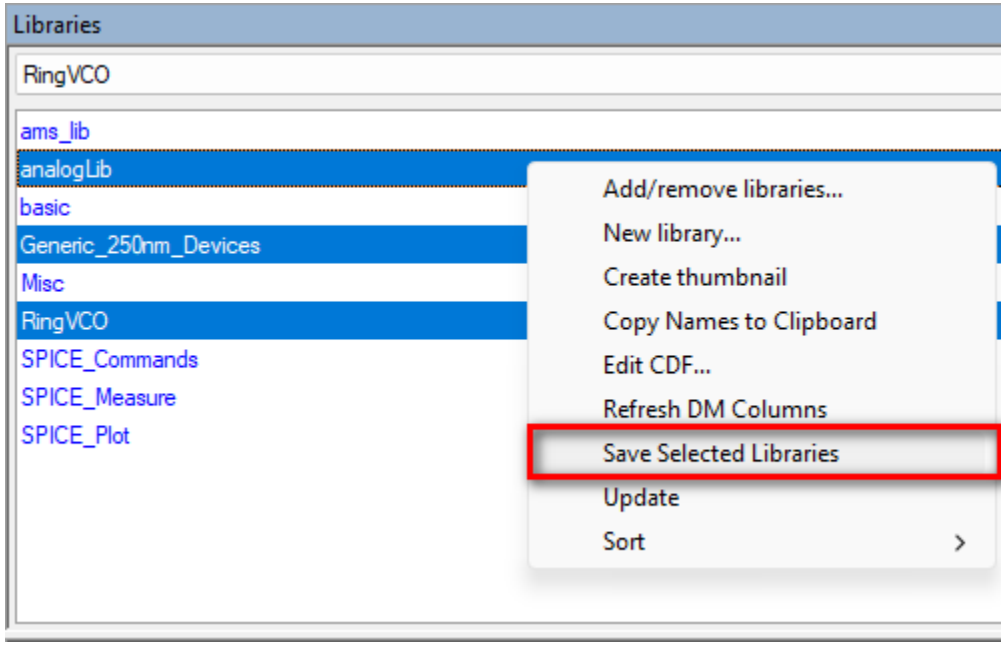
L-Edit Now Supports Interpreted Labels

- Interpreted labels are now supported in L-Edit
- In particular, instance names with interpreted labels ***[@instanceName]*** are now evaluated



New Library Navigator Option to Save Selected Libraries

- Library Navigator now has RMB context menu for **Save Selected Libraries** (same as S-Edit)



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Shipping Files/Installer

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Shipping Files

- New standard libraries located in the **StdLibs** directory at the top level of the shipping files installation
  - **ams_lib** – Same as previous but now has vnoise, and vbus#bits from old **SPICE_Sources** library
  - **analogLib** – New compatible library of standard symbols
  - **basic** – Basic library, mainly used for **NoConn** symbol for no connection
  - **Misc** – Smaller version of old **Misc** library includes **globalGnd** and Tanner title block symbols
  - **SPICE_Commands** – Same as previous and includes vector#bits from old **SPICE_Sources** library
  - **SPICE_Measure** – Same as previous
  - **SPICE_Plot** – Same as previous
- All front-end shipping files and the Generic 250nm PDK have been converted to 1/160 resolution and to use the new Standard Libraries
- Old standard libraries located at ***<install>\Process\Legacy*** and will no longer be updated
- No script to convert old standard libraries to **analogLib**

Known Problems & Solutions

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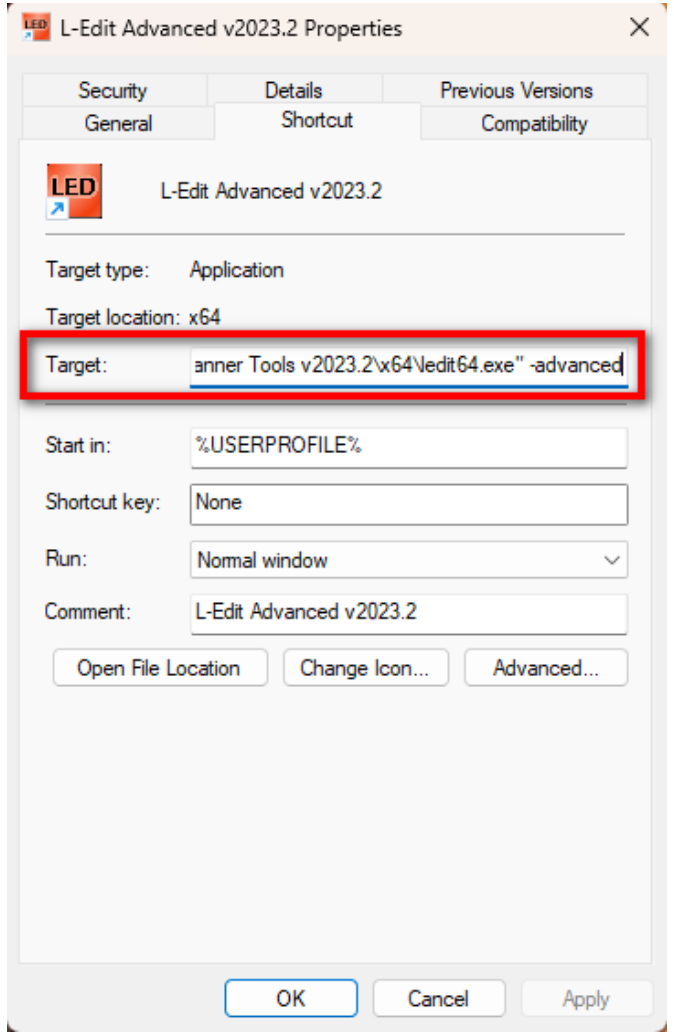
KPS

- To use advanced node features users must add `-advanced` to the **ledit.exe** command line string when the tool is launched
  - On Windows:
    - RMB click on desktop icon and select Properties
    - Add `-advanced` in the Target field in replacement of `-ic`
  - On Linux:
    - Issue the following command to start L-Edit at terminal:
      `ledit -advanced`



SIEMENS

KPS

- When you run an SDE test across corners and annotate individual corners' DC OP results, S-Edit displays only the first set of annotations
  - Any subsequent corner annotations fetch the same (previous) results
  - There is no work-around for this issue, and it will be fixed in a future product release
- Custom presentation of Library/Cell/View names is available in L-Edit and S-Edit, but is not yet available in Library Manager
- Implicit Selection is not currently available in L-Edit groups
- `database layers` tcl command has been renamed to `database lpps` in this release
  - Scripts will need to be updated to use the new command
  - A `-tcl` option has been added to the command to output all lpps to a tcl script to save rendering attributes for lpps
- In **analogLib** library:
  - The following symbols are symbol pcells and will not regenerate: `nport`, `pvccsp`, `pvcvsp`, `vccsp`, `vcvsp`
  - `isource` and `vsource` are not generating the correct netlist and shouldn't be used yet

Corrected Issues

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Corrected problems

- S-Edit
  - Improve performance loading large schematics with inherited connections.
  - Long delay from the end of AFS simulation until "Simulation finished" message and EZwave launch is resolved.
  - When exporting a netlist for Symphony simulations, empty subcircuit definitions are now generated for digital blocks, in order to support the mapping of pins by name.
  - Fixed problem where Import Spice with Parse Connectivity results in “missing port(s)” errors.
  - Fixed problem where tooltips over the simulation progress bar did not always appear.
  - Signals with wildcard in Setup Simulation > Results page now works for AFS simulation.
  - Fixed problem on Linux where many commands such as New Library, and also the Command window, default to a random path instead of the directory the tools are launched from.
  - Prevent crash when saving after renaming a cell by changing case only.
  - Fixed problem where Netset property assignment does not get exported to SPICE, unless the design is closed and reopened.
  - Testbench field is now updated after duplicating, renaming or deleting it on Properties window or by tcl.
  - Fixed problem where shorting inherited nets on top level caused shorts in subcircuit and incorrect evaluation of inherited nets in schematic.
  - On Linux, "Pick from schematic" under all applicable AFS Analyses' fields in Sim Setup can now be cancelled.

Corrected problems

- S-Edit (cont.)
  - ClioSoft error messages are now sent to the command window.
  - Fixed problem where Renamed Property names disappeared from the properties navigator when "Query" is checked.
  - The Stop Simulation behavior has changed so that the first press will attempt a graceful stop that releases licenses and closes files, while a second press will forcefully terminate the simulation.
  - Fixed problem where DC result annotation disappeared or cut off while panning around the schematic with the keyboard arrow keys.
  - Double-clicking on a label and then approving the dialog box no longer results in shifting of the entire label.
  - Deleted views are now ignored in design check, as both views to check, and as views to check against.
  - Fixed reading of OpenAccess cdsTerm labels written by Custom Compiler so “annotate port” no longer appears. Replace [] with <> in port names, net labels, and evaluated labels.
  - Fixed issue where "Save All" took longer when the design is in SVN working copy and not managed compared to the design which is out of working copy.
  - Several import issues fixed and more data is now imported from ADE state files into Setup Simulation.
  - Fixed warning from '24 Overlapping net label and pin' when net label is overlapping text label in a symbol.
  - EZwave is now brought to the foreground when probing from schematic.

Corrected problems

- S-Edit (cont.)
  - In Setup Simulation, on all pages, all controls on the "Value" side (RHS) of the setup table are now consistently displayed in English, even when in Japanese mode. These correspond to simulator options and so they are in English. This cases situations where fields were enabled/disabled incorrectly in Japanese mode.
  - Fixed problem in import of CalibreViews case of properties was not being imported correctly.
  - Corrected EZwave error “The file <name> cannot be opened” when S-Edit Waveform viewing is set to ‘During’ for an AFS simulation.
  - Corrected a Windows to Linux EZwave probing failure with error message “The file <name> cannot be found”, when the simulation results folder name begins with a slash.

Corrected problems

- L-Edit
  - Fixed problem on Linux where many commands such as New Design, Open etc. menus and Command window would default to a random path instead of the directory the tools are launched from.
  - DEF Export now writes extension values for all coordinates of a wire with "End Style" set to Extend. Previously on the endpoint vertices had extension values written.
  - Tori and Arcs are now exported to ODB++.
  - Pick Layer now works when editing in place but picking a layer outside the cell you are editing in place.
  - Fixed problem on GDS import, when there are two layout views for a cell in "Search cells in" library, GDSII import uses different layout views randomly. Also, views named “Layout” are now given priority.
  - The Net name of an object is now visible and editable on the Edit Objects dialog.
  - GDSII Import "Search for cells in" is now updated correctly when the value is deleted.
  - Invoking Custom Layer Palette dialog will no longer reset the current palette, even after Cancel.
  - Temporary rulers no longer disappear while moving instances.
  - Improved Performance of Cell Copy with hierarchy when the top cell is open.
  - Fixed issue where SDL > Check Connectivity was incorrectly reported in the Verification Error Navigator when multiple views of the cell were present.

Corrected problems

- L-Edit (cont.)
  - Fixed a problem where Mask Bias would assign data type.
  - Fixed a problem where the GDS numbers in Setup layers were used instead of the GDS layermap file for GDS Export during LVS.
  - Fixed problem where TCL parameters defined on a T-Cell were missing when the T-Cell was instanced.
  - In Draw > Convert > Snap to grid, instances, vias, and circles are now correctly snapping to the Mouse Grid.
  - Fixed command line -U option. Command line scripts (-u, -U, -t, -T, filename) are now executed in the order they appear on the command line, in both L-Edit and S-Edit.
  - Fixed problem where after using Duplicate and auto-increment, the entire set could not be renamed to the initial label if the rename is to the first value of the sequence.
  - Improved performance of loading and refreshing layer palettes when there are a very large number of Layer-Purpose-Pairs. Layer Palette data is now stored in %appdata% in the L-Edit/SetupDesign/<design>/LayerPalettes folder. This allows palettes to be shared between users.
  - Fixed problem when editing an object in L-Edit (Ctrl-E) to modify the number of columns or rows (usually a via array), if the existing value is deleted a pop-up error is immediately displayed saying "Enter an integer".

Corrected problems

- T-Spice
  - Corrected BSIM4 cgtot, total gate capacitance, printed values (internal capacitance values were correct).
  - Fixed a .measure error ‘boost::bad_get: failed’ when measurement result values are chained into the expression for a subsequent measurement
  - Enable use of named .print values within measurement calculations.
  - Recognize // as a comment line in netlists
  - Corrected DC Sweep hysteresis simulation results which under some circumstances did not show hysteresis effects
  - Corrected some noise contribution terms for M multiplicity scaling with VBIC, JFET, MesFet, EKV, and bipolar devices
  - Fixed memory leaks and reduced memory consumption with some device models
  - Corrected Rise=Last measurements that were ‘Not Found’ under certain circumstances.
  - String parameter declarations will now support str(<param_name>) syntax used by some PDKs
  - Added support for auto-completion in the T-Spice editor using <Ctrl><Space> keystroke

Corrected problems

- Library Manager
  - Fixed issue where opening a new schematic view from Library Manager gives *.tmp cell not found error if a schematic view is already open.
- Waveform Viewer
  - Fixed problem where moving magnitude curves of a complex trace onto a different plot would show the deg component on the new plot.
  - The menu accelerator key bindings to drop down menus have been removed from the Japanese menus.
  - Bindkeys “Zoom In” and “Zoom Out” have been changed to “Zoom In Horizontal Around Center” and “Zoom In Horizontal Around Center”. Defaults bindkeys for Zoom In Horizontal Around Center is “]” and for Zoom In Horizontal Around Center is “[“. As with all bindkeys, these can be custom bound to any key as user prefers.
  - Bindkey for Save Chartbook, “Ctrl+S”, is now persistent between sessions.
  - Bindkeys for Chart > Move Curves > Up/Down are now persistent between sessions.
- Tanner Designer
  - The grouping of Monte Carlo measurement results into Data Sets has been corrected for certain circumstances.
  - The Waveform Viewer button will now open Eldo simulation results using display formatting specified in the associated .swd file.

Corrected problems

- Linux
  - Fixed problem using soft link to /home in the wine configuration directory while opening lib.defs.
- ESI
  - The version of Putty installed with Tanner Tools has been upgraded to 0.78, providing compatibility with PPK version 2 and 3 private key formats.
  - DISPLAY (and all Environment variables) is now treated as case insensitive in ESI.
  - Fixed problem saving ESI settings to registry.
  - Fixed problem in ESI resulting in the message, “Error: could not open file” when running a MC simulation.