

# Tanner Digital Implementer

## Complete RTL to GDSII flow integration from Siemens Digital Industries Software

### Benefits

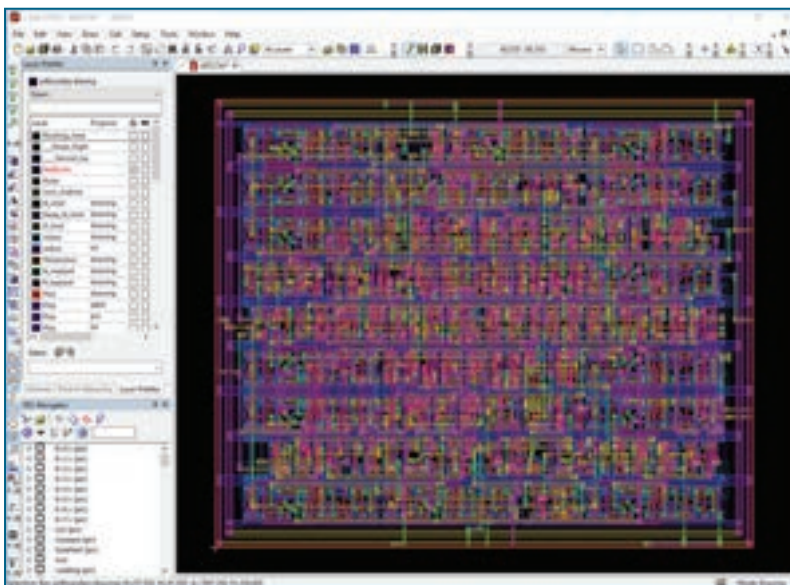
- Full integration with Oasys-AMS Synthesis and Nitro-AMS Place and Route
- Simplified setup wizard in L-Edit
- Physical synthesis
- Oasys patented "PlaceFirst" synthesis technology enables RTL optimization to deliver best quality of results
- High performance timing-driven place and route with patented multi-corner, multi-mode (MCM) analysis and optimization architecture
- Floorplan and power plan functionality
- Clock tree generation
- Low-power design methodologies
- Access to synthesis and place and route scripts for customization and advanced functionality
- Foundry PDK support
- Intuitive and easy to use with a quick learning curve
- Unparalleled customer support
- Flexible licensing

### Complete RTL to GDSII flow for "analog on top" designs

Tanner Digital Implementer (TDI), powered by the Oasys Synthesis and Nitro Place and Route engines, is integrated into L-Edit, Tanner's physical layout tool, to address the physical implementation of the digital needs of "analog on top" designs. More and more analog designs are becoming digitally-assisted resulting in more digital content to enhance analog capabilities, such as automated

calibration and more programmability. TDI integration into L-Edit is the ideal cost-effective, easy-to-use digital synthesis and place and route solution. It addresses performance, capacity, time-to-market, power and variability challenges. The tool is optimized for analog specialty process technology nodes at 22 nm and above, with up to 75K instances of digital logic per license and the ability to stack 4 licenses.

Tanner Digital Implementer can help whether designing an analog IC with a small amount of digital control or a more complex mixed-signal ASIC. The tool facilitates bringing together complex digital circuits with high performance analog interfaces, providing a complete flow. It is backed up with unparalleled support and can evolve to meet the needs of designs for tomorrow.



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No other EDA vendor offers a digital implementation tool flow so closely aligned with the needs of “Analog on Top” design, addressing companies working in applications such as automotive, internet of things (IoT) imaging/display, industrial control, medical, sensors, automotive, RF, space and power management.

## Import design data and technology data and specify timing

Tanner Digital Implementer provides a streamlined user interface to import technology data such as LEF and TCL technology files, Liberty® and PTF files. Users can import a Verilog/VHDL netlist and define timing requirements by specifying clocks or by using a SDC file.

## Define floorplan and power plan requirements

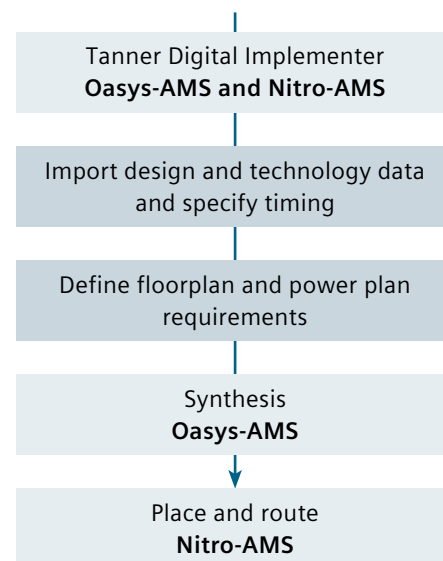
For floorplan requirements, TDI enables the user to specify chip size or aspect ratio and utilization, margins and row

site names, or define the requirements in the layout or via a DEF floorplan file. For power requirements, TDI enables the user to specify power/ground ring and stripe parameters, or define the requirements in the layout or via a DEF floorplan file. After the synthesis and place and route programs complete, the results are imported automatically into L-Edit.

## Supporting standards

Tanner Digital Implementer uses industry standard file formats for easy interoperability with libraries, tools and flows from any foundry or vendor. Formats include Verilog/VHDL, OpenAccess and GDSII data for layout, LEF and TCL for technology information, LEF/DEF for abstracts and routing, Liberty for timing data, SDC for design constraints, interconnect technology file (ITF)/process technology file (PTF), UPF for power, SPEF for parasitics and SDF for timing annotation.

## Tanner Digital Implementer Flow



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