

Verifying with speed and accuracy with Siemens Digital Industries Software

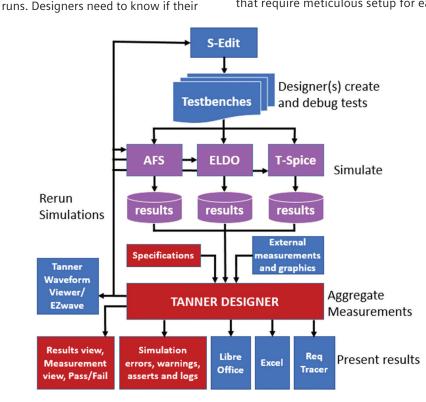
Benefits

- Track and aggregate all simulation measurements for a project
- Incrementally customize as the project progresses
- Launch and rerun specified simulations
- Group or sort results and launch specific simulations
- Generate custom reports for team members via CSV, HTML, ReqTracer, LibreOffice or Excel
- Build documentation from reports
- A single dashboard shows all team members passing/failing specifications for all simulations
- Integrated into the Tanner design flow
- Supports AFS, Eldo and T-Spice simulators
- · No proprietary languages to learn
- Minimal setup
- Easily start with existing simulation results
- Platform independence on Windows® or Linux®

Tanner Designer – the solution for analog verification management
Design teams create and verify blocks that together comprise the system or product that they will bring to market.
Over the product development cycle, there can be thousands of simulation

design blocks have been completely verified and meet specifications, system designers need to verify that the blocks all work together and project managers need a method to understand the verification status of each block and the entire system. Without a tool to help them, the team can be overwhelmed with analog verification results, to the point that they have little confidence that the blocks have been completely verified.

In the world of analog verification, simulation results are typically managed manually, or with very expensive tools that require meticulous setup for each



Tanner Designer helps teams easily track analog verification throughout the entire design cycle.

Tanner Designer

project and that use proprietary methods that are hard for new team members to use. What teams need is a tool that is easy to set up and that can be immediately used in their design flow to track analog simulations and to determine that each block meets specifications.

Tanner Designer is specifically designed for analog verification management that is easy to set up and the team can immediately deploy it in the integrated Tanner design flow. Tanner Designer presents a dashboard that every team member can use to monitor the analog verification progress over the entire life

cycle of the design and verification process. Analog FastSPICE (AFS), T-Spice and Eldo® simulation verification progress and results can be seen in realtime, targeted simulations can be re-run and users can interact with measurement details. Tanner Designer utilizes the familiar spreadsheet structure of Microsoft® Excel® and LibreOffice so there is unlimited flexibility to capture specification requirements, calculate formulas, enter user-defined specifications and to customize reports.

Getting started with Tanner Designer is as easy as pointing the tool to an existing set of simulation results and viewing them within the dashboard. The dashboard (figure 1) lets designers interact with the schematic, view waveforms and run one or more simulations

Getting started quickly

using T-Spice, AFS or Eldo.

Testbenches							
Name	Result	Fresh	Status	Schedule	Include in Report	Result From GUI	
TB_ODAMD_OL_GBW_Supply_TSP	~		Completed		M	~	
TB_OpAmp_PSRR_Corner_TSP	~		Completed		☑	<	
TB_OpAmp_SR_IDD_MC_TSP	~		Completed		☑	<	
TB_OpAmp_SR_IDD_SR_Supply_TSP	~		Completed		☑	<	
TB_OpAmp_SR_IDD_Typ_TSP	~		Completed		☑	<	
TB_OpAmp_VOS_MC_TSP	~		Completed		☑	<	
TB_RingVCO_TSP_FreqVsLoad	*		Completed		Ø	*	
TB_RingVCO_TSP_MonteCarlo	~		Completed		☑	<	
TB_RingVCO_TSP_PVT	~		Completed		☑	<	
TB_RingVCO_Assert_Warnings_TSP	~		Completed		☑	<	
TB_RingVCO_Eye_TSP	~		Completed		☑	<	
TB_RingVCO_Tune_TSP_PostLayout	~		Completed		☑	<>	
TB_RingVCO_Tune_TSP_Schematic	~		Completed		☑	<	
TB_RingVCO_Tune_TSP_VerilogA	~		Completed		☑	₩	

Figure 1: Tanner Designer dashboard.

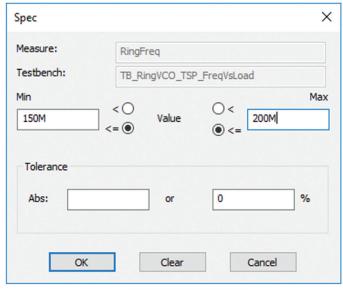
Testbenches TB_RingVCO_AFS_FreqVsLoad_rem > DataSet 1:TB_RingVCO_AFS_FreqVs							
Сар	temp	RingFreq <hz></hz>	RingFreq_Period				
5.000f	-10.00	218.2M	4.584n				
5.000f	0.000	204.0M	4.902n				
5.000f	10.00	191.7M	5.217n				
5.000f	20.00	180.2M	5.551n				
5.000f	30.00	170.0M	5.882n				
5.000f	40.00	160.5M	6.230n				
5.000f	50.00	151.7M	6.593n				
14.00f	-10.00	209.3M	4.778n				
14.00f	0.000	196.3M	5.095n				

Project managers can determine the status of the simulation runs in order to track the project. The tool creates individual measurement views, results views or a general testbench specs pass/fail view, or generate an Excel/LibreOffice workbook with tabs that present detailed information about each simulation result (figures 2-5).

Figure 2: Measurement view.

Testbenches	TB_RingVC	O_AFS_FreqVsLoad_ren	n >	DataSet 1:TB_RingVCO_AFS_FreqVs × Specs ×						
Measure	Average	Spec	In Spec	Out of Spec	Invalid	Total	Pass/Fail	Min	Max	DataSet 1 (42)
RingFreq <hz></hz>	166.3M	range 150.0M 200.0M		15	0	42	Fail	126.7M	218.2M	166.3M
RingFreq_Period	6.124n		42	0	0	42	Pass	4.584n	7.893n	6.124n

Figure 3: Results view.



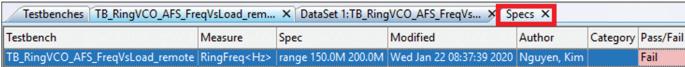


Figure 4: Testbench specs view.

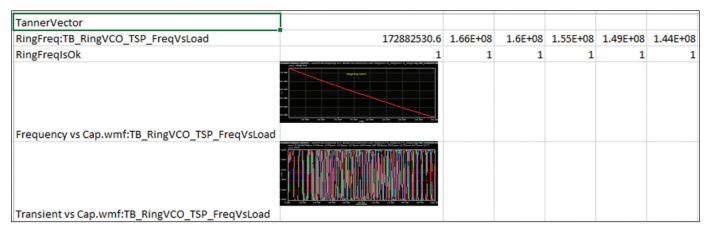


Figure 5: Excel/LibreOffice.

Easily customize the solution

As the project progresses, team members might want to customize what they see in the dashboard or the content of reports. That is easily accomplished by taking advantage of the flexibility and power of the Tanner Designer interactive tool and Excel/LibreOffice. Typical customizations include:

- Adding columns to display extra information such as test names, notes, errors, warning, asserts or other descriptive information
- Sorting and re-arranging results for easy debugging

- Defining equations based on measurements to display information using a direct interface to Excel/ LibreOffice
- Creating user-defined measurement specs for pass/fail criteria
- Making queries to the measurement database
- Inserting graphs and illustrations in the Excel/LibreOffice spreadsheets to generate presentation-quality graphics (datasheets)
- · Linking to simulation waveforms

Siemens Digital Industries Software siemens.com/software

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