Intelligent Outlier Detection & Removal

Galaxy™ PAT-Man

DATASHEET

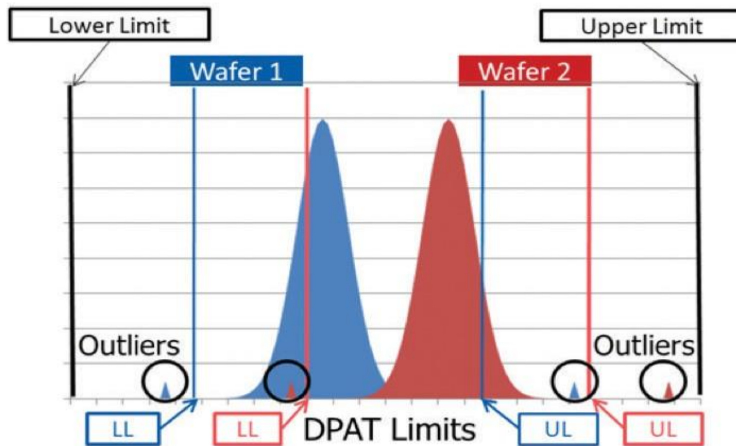

Figure 1. PAT-Man exceeds the AEC-Q001 guidelines for Dynamic PAT (DPAT). It identifies parametric test outliers based on the distribution of values for each wafer or lot and adjusts for site-specific offsets.

Overview

Galaxy PAT-Man™ is a comprehensive solution for PAT (Part Average Test) and related outlier removal techniques, which manages the DPM (Defects Per Million) reduction process from initial wafer sort through final test to RMA analysis. Based on a proven architecture with more than twenty production deployments around the world, PAT-Man™ integrates easily with your existing production test environment and provides the most robust and cost-effective solution for DPM reduction in the industry.

PAT-Man for Wafer Sort

In general, PAT is most economical when deployed at wafer sort since any resulting scrap is not burdened by the additional cost of packaging and final test. PAT-Man at sort analyzes the test results for the entire wafer before identifying any specific dies as outliers. It checks for parametric test outliers, spatial failure patterns, reticle defects and historical anomalies (relative to other wafers and lots). It then creates a new wafer map that is passed to your MES system or OSAT for packaging.

Intelligent Outlier Removal Rules Maximize Yield and Quality

PAT-Man includes a powerful recipe editor and yield simulator that enable users to experiment with different tests and PAT algorithms and measure the resulting yield impact based on simulations against historical data. Recipes can be based on a

FEATURES

- Automated outlier removal for wafer sort and final test
- Supports SPAT, DPAT, Z-PAT, MultiVariate PAT, GDBN, Clustering, NNR, reticle patterns, automatic scratch detection and custom recipes
- Smart and Adaptive recipes with automatic shape detection:
  - Gaussian
  - Gaussian with one tail (L or R)
  - Gaussian with two tails
  - LogNormal (L or R tail)
  - Multi-modal
  - Bimodal
  - Clamped (one side)
  - Clamped (two sides)
  - Categorical (distinct classes)
- Easy to use recipe editor with automated test selector and yield impact simulator
- Yield-Man integration for AEC-Q002 compliant Statistical Yield Analysis and maverick lot detection
- PAT and raw binning automatically stored in Test Data Repository (TDR)
- Special PAT reports, including:
  - PAT bin Pareto
  - PAT yield trend
  - Rule effectiveness
  - Tests with most outliers
  - Marginal dies
- PAT yield alarms
  - Low yield alert
- Integrates with MES systems for fully automated operation

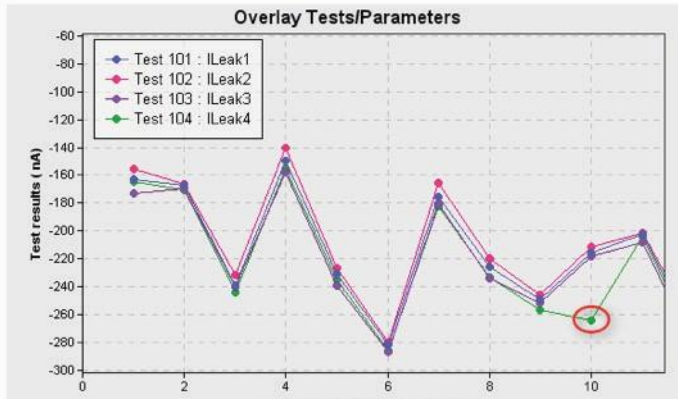

Figure 2: Example of Multi-Variate outlier that would be missed by most PAT solutions

combination of parametric test distributions, spatial patterns like GDBN (good die in bad neighborhood), and maverick wafer/lot detection like SYA (AEC-Q002 compliant statistical yield analysis). PAT-Man's "smart and adaptive" setting recommends tests for PAT binning, and employs sophisticated automatic shape detection, which automatically adjusts for Gaussian and non-Gaussian distributions on-the-fly, thereby ensuring accurate outlier identification. PAT-Man also incorporates site-specific limits to compensate for tester, probe card and socket variations and drifts, thereby eliminating unnecessary yield loss.

Multi-Variate PAT Finds Hidden Outliers

PAT-Man offers the industry's first multi-variate PAT solution, which can automatically identify groups of correlated tests and catch hidden outliers that are missed by other algorithms. Multi-Variate PAT (MVPAT) looks for variations across groups of similar/ correlated tests instead of just looking at each test individually. Figure 2 shows a simple example of MVPAT in which four leakage tests tend to correlate closely, except for part ID 10 where the leakage for test 104 is on the high side (note negative scale). PAT-Man's MVPAT recipe would detect this part as an outlier, whereas a traditional, univariate recipe would not, since it falls within +/- 6σ.

Increase Yields with In-depth Outlier Analysis

PAT-Man users have discovered that by analyzing the outlier data and feeding back their findings to the manufacturing process they can improve overall yield by better centering the fab process and/or eliminating assembly related defects. For example, instead of seeing yield drop from 90% to 89% after adding PAT binning, they may see yields improve to 92% or more after incorporating PAT-driven process improvements. PAT-Man's integration with Galaxy Yield-Man facilitates this process with additional reports that analyze PAT fallout in detail, including tests that generate the most outliers, PAT yield trends, PAT Bin Paretos, marginal dies, etc.

PRODUCT CONFIGURATIONS

Examinator-PAT™

A special version of Examinator-Pro™, including the PAT recipe editor and yield impact simulator. Can also be used for RMA analysis to experiment with different recipes that can detect hidden outliers.

PAT-Man for Wafer Sort

Includes PAT-Server software for wafermap post-processing, yield alerting and MES integration.

SYSTEM REQUIREMENTS

PAT Server Requirements

- O/S: Windows Server 2019 (64 bit) or CentOS 7 (64 bit)
- Hardware configuration is a function of data volume

Examinator-PAT Client Requirements

- OS: Windows 10 (64 bit) or Linux RHEL/CentOS 7 (64 bit)
- CPU: 2 or more cores @ 2 GHz
- RAM: 16 GB or 2.5X File Size in GB (whichever is larger)

For the latest product information, call us or visit: https://www.galaxysemi.com/

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