Unity™ Chip Planner

Hierarchical Floorplanning for Custom Designs

As semiconductor-processing technologies move toward smaller geometries, the complexity of custom integrated circuits (ICs) increases significantly every year. However, many custom design teams are still using the same, primarily, manual floorplan assembly methodologies that have been used for the last 10 years or more. Pulsic Unity Chip Planner, the first truly hierarchical floorplanner for custom design, enables custom design teams to manage growing complexity while accelerating design closure and improving design quality.

Rising Chip Complexity Requires a New Approach

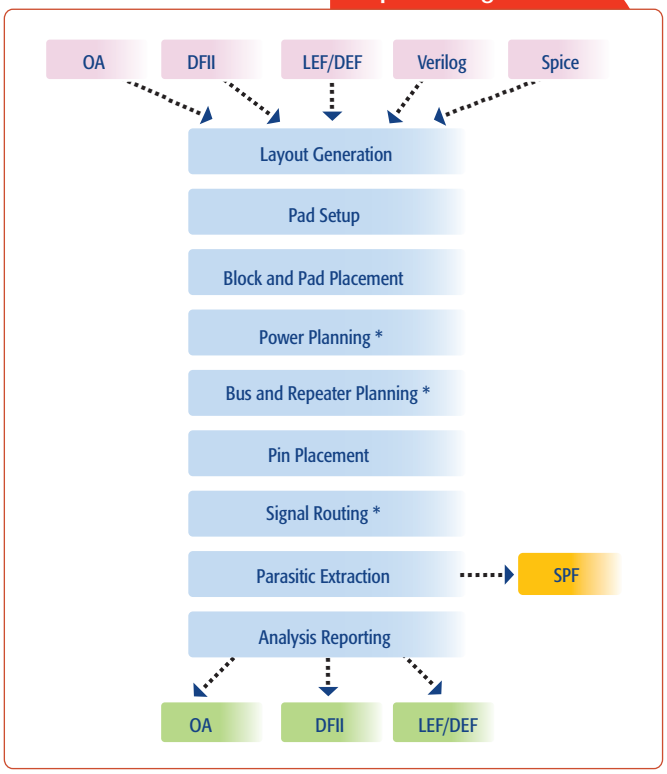
As design complexity has grown in all areas of chip design, design tools aimed at digital designs have largely kept pace. Automated, hierarchical floorplanners are a standard part of the digital design flow. However, these tools do not address the unique needs of custom design. So, until now, many custom design teams have struggled with bottom-up assembly methodologies that lack a global understanding of a chip's routing congestion and top-level parasitic data for simulation until the chip is almost complete.

Lack of automation makes pin placement and routing problematic. And, generally, the various layers of hierarchy are created in isolation of each other, which leads to problems once the design is assembled fully. Excessive layers of hierarchy created by bottom-up methods waste both design effort and silicon resource. With these manual approaches, the frequent netlist changes that are a natural part of a leading-edge design process become very difficult to manage efficiently, resulting in a loss of productivity.

Fully Hierarchical Floorplanning Speeds Custom Design Closure

Pulsic Unity Chip Planner addresses these critical issues with the first fully hierarchical, top-down and bottom-up floorplanner for custom design. By providing a high level of automation, Unity Chip Planner gives accurate results quickly and enables custom design teams to respond to netlist changes quickly and easily. Unity Chip Planner provides all the necessary tools and technologies within a fully integrated floorplanning environment. The guided flow offered in Unity Chip Planner helps ensure faster design closure with successful results every time.

Chip Planning Flow



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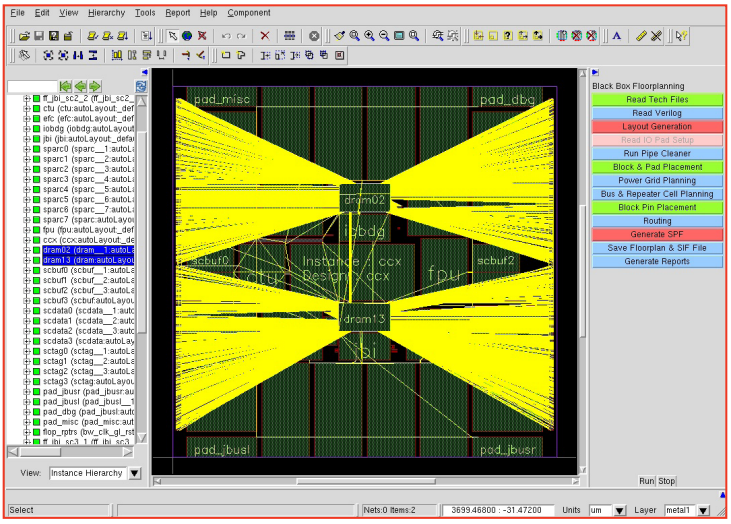
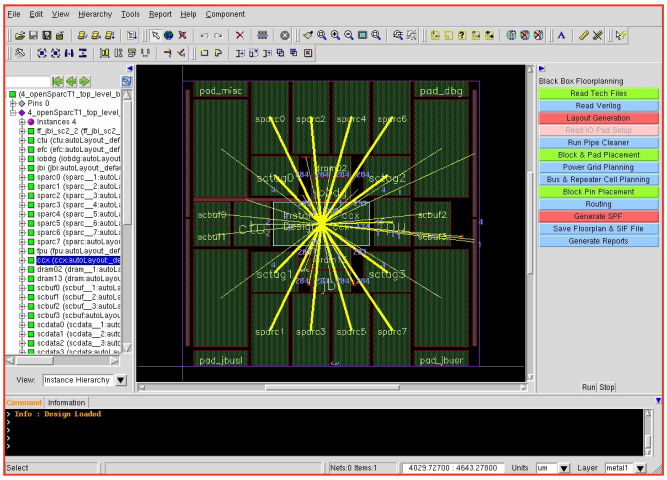


Top level block placement is completed with flightlines for datapaths illustrated above

Unity Chip Planner: A New Approach to Custom Design

Custom designers face unique challenges. Custom designs generally incorporate large hard IP blocks and analog content and have few metal layers available for routing. As process geometries shrink, the extreme aspect ratios of the routed wires and highly resistive metals make understanding parasitics critical. At leading-edge process nodes (28 nm and below), process rules constrain designs in new ways. Pulsic has applied insights gained in over 10 years of work with leading-edge custom designers to develop Unity Chip Planner to address the unique needs of custom design.



Summary flight lines are illustrated for the floorplan of a cross bar floorplan topology

Efficient, effective custom design floorplanning requires a series of top-down optimizations, followed by a bottom-up optimization, that determine pin placement in consideration of the block placement at lower levels of hierarchy, then use those pin placements as the backbone of communication between levels of hierarchy.

The Unity Chip Planner area estimation technology analyses the netlist and hierarchically determines the area required for hard IP, analog blocks, soft blocks and multiple standard-cell form factors concurrently, giving an accurate hierarchical estimate of the area required. Pin placement takes lower-level placement into account and is optimized to enable the ideal routing pattern for every net, with minimum wire crossing, easier shielding, and shortest interconnect length for better noise reduction. The Unity Chip Planner block placement technology can place hard IP and softblocks simultaneously, including block clustering and softblocks with multiple instantiations (with no need to uniquify). The unique "push down" feature enables designers to push top-level power bus and routing structures down the hierarchy, making these top-level structures visible throughout the layout hierarchy. The Unity Chip Planner hierarchical ECO feature enables designers to incorporate changes throughout their design hierarchy rapidly by simply loading the new netlist.

Rapid Floorplan Prototyping

Tight design cycles rarely afford custom designers time to explore different floorplans to find the best fit for the die area. The Unity Chip Planner has a flexibile and easy- to- configure interface that enable designers to explore different packages and to prototype multiple floorplan topologies quickly to find the optimal use of the die area allocated for the design.

Benefits

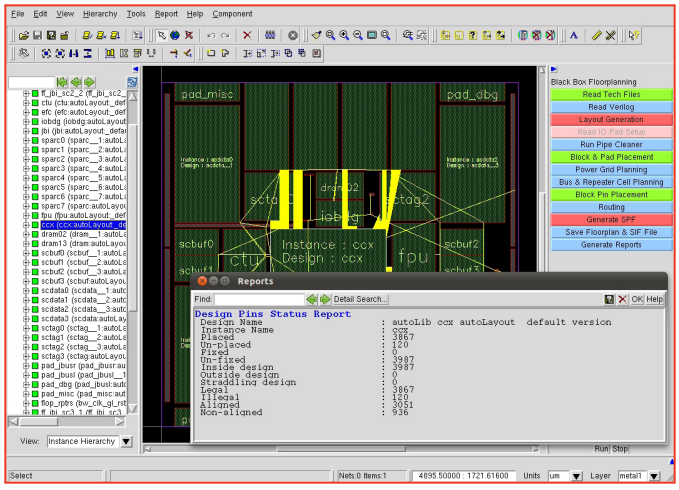
- Achieve design closure faster with the first and only top down hierarchical floorplanner for custom design
- Explore options and implement floorplans rapidly with accurate area and parasitic data
- Obtain accurate parasitics for early simulation and static timing analysis
- Execute ECOs quickly and precisely

Features

- Hierarchical and pseudo-hierarchical floorplanning for custom design
- Hierarchical area estimation, including custom digital and analog estimation
- Automatic block placement and softblock shaping
- Hierarchical automatic pin placement and sorting optimization
- Intelligent, router- aware pin placement for efficient top- level routing
- Complete hierarchical ECO solution
- "Push down" of power and signal net routing for visibility in lower layers
- Design partitioning
- Interfaces to LEF/DEF, CDBA, OpenAccess®, Verilog®, SPICE, CDL, .LIB and .SDC

Specifications/System Requirements

- Linux: x86 and x86_64
- Solaris: Sparc 64 and x86_64



The Unity Chip planner flow toolbar guides designers through the floorplanning process step by step

for more information, please go to our website at www.pulsic.com or email us at sales@pulsic.com