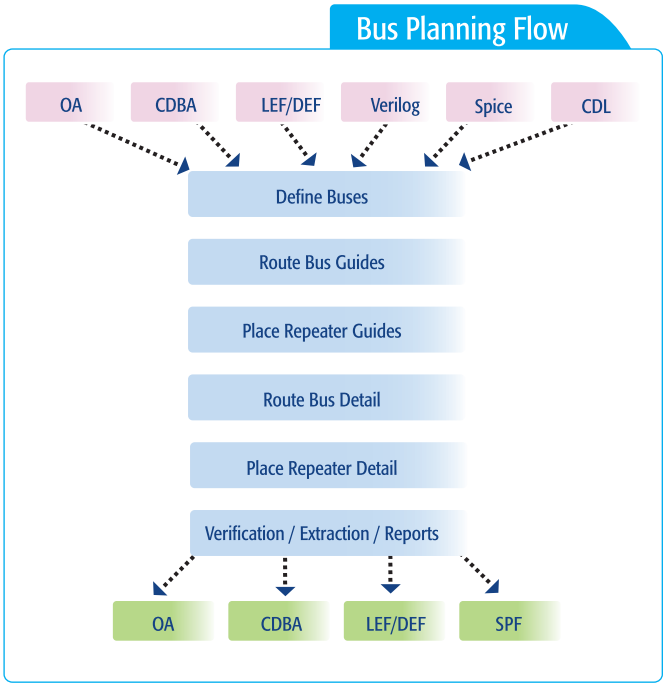
# Unity™ Bus Planner

## Bus and Repeater-Cell Planning for Custom Microprocessor Designs

Modern microprocessor designs, particularly those with multi-core architectures, include hundreds of datapaths that traverse the width or length of a chip, some of which are very wide (1000+ bit) buses. To meet signal timing and slope targets for these buses and critical-signal nets, designers must insert a series of repeater cells to improve the speed of the signal. Until now, bus planning, routing, bus interleaving and repeater-cell insertion have been manual tasks. But the numbers of buses and nets in complex microprocessor designs has made a manual approach impractical, both in terms of execution time and accuracy. Pulsic Unity Bus Planner is the first and only automated product to provide an easy, GUI-driven, guide-based methodology for interactive planning and routing of multiple large buses and associated repeater cells.

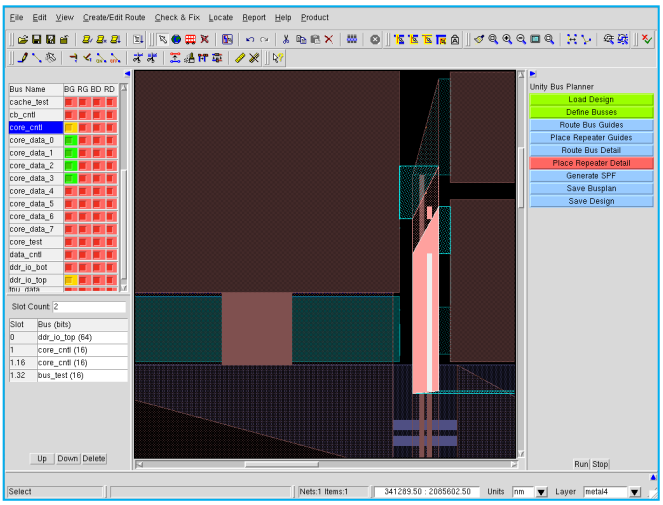



## The Bus-Planning Bottleneck

During the initial floorplanning phase, designers undertake block placement and power-grid planning; followed by bus planning and repeater cell insertion. To know whether a particular block-placement or pin-placement will be a good solution, designers need to determine the location of buses, and the kind of repeater-cell structure (if any) needed to support those signals. So, cross-chip buses and critical nets such as clocks and control signals must be planned carefully, early in the development process. The goal of this process is to get parasitics data (SPF), for critical datapaths to use in dataflow simulations. The earlier in the design cycle these simulations start, the better.

During bus planning, designers fit as many buses as possible through dedicated channels to avoid issues that could impact their ability to meet timing specs. Very fast bus signals require shielding with direct-current (DC) signals (e.g., VCC and GND) to prevent noise created by nets routed side-by-side. Chip architects interleave buses so that they provide shielding for each other, rather than using valuable routing resources for dedicated shielding. However, planning and routing the interleaving of hundreds of buses manually is painstaking and error-prone. Internal tools for this task are often unmaintainable or inadequate for the automation of larger chips.

Designers also face the challenge of meeting timing and slope constrains for wide buses and critical signals. This is accomplished by inserting repeater cells that keep a signal at the necessary strength as it journeys across the chip. Banks of repeater cells associated with a bus are placed in a series and in specific locations to ensure that bus signals meet timing constraints and avoid rise and fall signal violations. Repeater-cell structures can be simple buffers, inverters, complex gates, flip-flops, latches or any combination of these cells.



*Plan guides defining the eventual position of the bus routing*

Signals on wide buses should arrive simultaneously with similar slopes at the receiving input gates. In order to accomplish that, designers must match the metal layers, number of vias, repeater cells, and repeater cell location and type, a time-consuming process if done manually. In addition, designers must have a reliable methodology for managing the repeater cells through the many inevitable changes that are part of any design cycle. Many design teams have developed various script-driven, in-house methodologies to handle repeater cells, adding the additional task of code development and script-maintenance to over-burdened design teams.

## Unity Bus Planner: Automating a Critical Design Function

Pulsic Unity Bus Planner is the first and only automated product to provide an easy, GUI-driven, guide-based methodology for interactive planning and routing of hundreds of large buses with 1000+ bits per bus, along with their associated repeater cells. Users are able to configure and manage interleaving buses. Unity Bus Planner also enables interactive and automatic repeater-cell insertion and re-sizing for each bus to optimize both timing and signal slope.

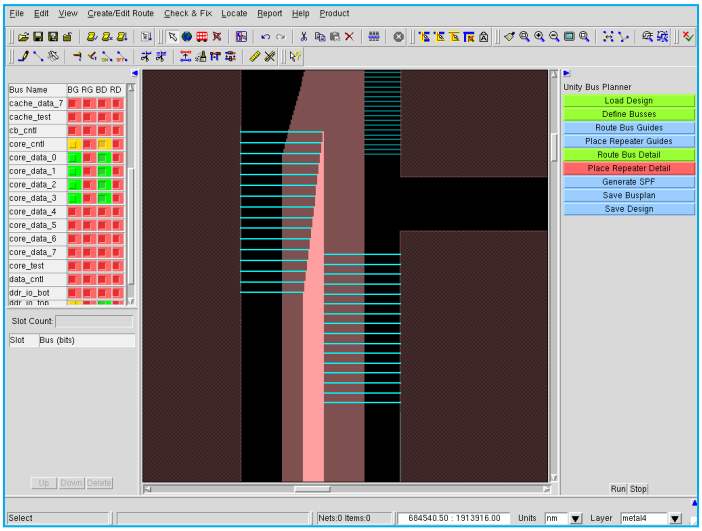
With the interactive and automated planning, routing, and management capabilities of Unity Bus Planner, designers can complete bus and repeater-cell planning in minutes or hours rather than in days or weeks. Automation also makes the process easily repeatable when design changes necessitate modifications to a bus.

## Speed and Flexibility in a Complete Bus-Planning Flow

Pulsic has used its experience with custom design teams to develop technologies and products that uniquely address the needs of advanced custom designs. The Unity Bus Planner combines the speed and structure of digital design methods with the flexibility of a custom design solution.

The Unity Bus Planner GUI-driven flow enables designers to quickly and easily plan the routes of hundreds of buses with 1000+ bits per bus. A guide-based method for controlling bus interleaving when they are routed through the same physical area is also included. Unity Bus Planner selects and sizes repeater cells to optimize timing, and provides interactive editing of this repeater-cell plan.

In addition, Unity Bus Planner incorporates Pulsic DRC-correct, automated detailed routing for buses and repeater cells, providing designers with instant feedback on design rule adherence. Unity Bus Planner also accommodates netlist changes and recreates previously defined bus and repeater-cell configurations automatically.




*Interleaved bus routing created using Unity Bus Planner*

## Benefits

- Converge on a floorplan solution quickly through fast implementation analysis of global congestion due to buses and critical signals
- Obtain early access to parasitics data (SPF file) for critical datapath simulations
- Interleave multiple buses to allocate routing resources efficiently through the same physical location
- Meet timing and slope requirements for top-level buses and critical signals early in the design process
- Avoid power grid issues through optimal placement of repeaters
- Avoid noise with robust shielding
- Handle netlist changes easily with the productivity and accuracy benefits of automatic place and route for critical buses

## Features

Each step supported by Unity Bus Planner may be performed on a single bus, several buses, or all the buses in a design.

- Bus-route planning: interactive planning for the paths (location and layer) of up to several hundred buses with 1000+ bits per bus
- Bus interleaving: interleaving of the segments of buses, primarily controlled by the relative position of guide segments
- Bus routing: executing detailed routing of the bus
- Repeater-cell plan generation: selection and optimization of the repeater cells for a bus
- Repeater-cell placement: detailed placement of repeater cells and modification of the bus netlist to include the repeater cells
- Repeater-cell plan editing: interactive editing of the repeater cell plan for a bus. Interactive insertion of latches/registers into the repeater cell plan
- Repeater-cell routing: connection of the repeater cells to the bus routing
- Change management: easily return to the process and redo the steps to accommodate changes
- Logic-gate planning: interactive planning for the position of any logical gates (e.g., AND, OR) required for the buses

## Specifications/System Requirements

- Linux: x86 and x86_64
- Solaris: Sparc 64 and x86_64

for more information, please go to our website at www.pulsic.com or email us at sales@pulsic.com