SIEMENS
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Calibre DESIGNrev

Chip finishing platform

Benefits

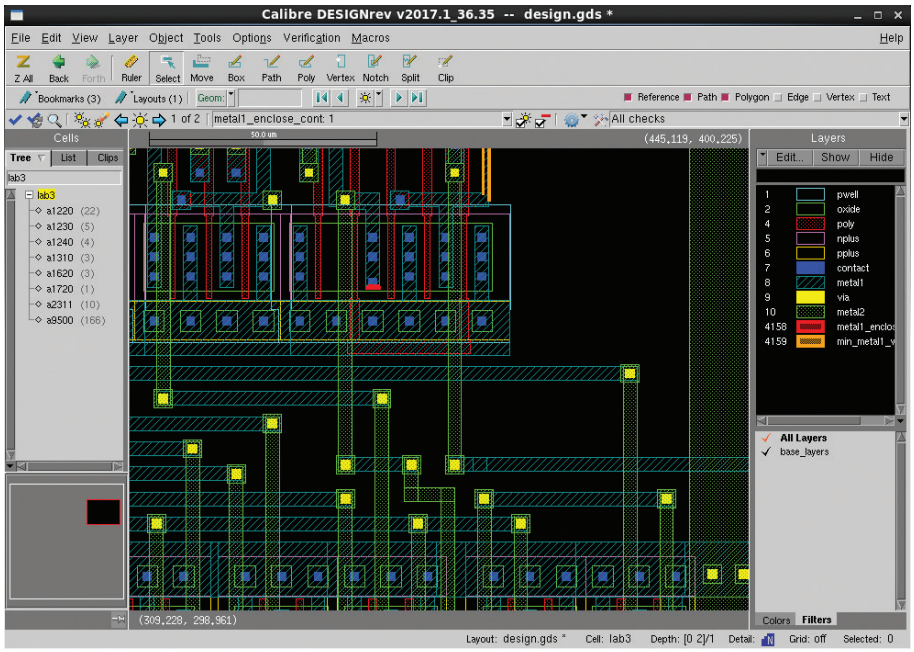
- Complete chip finishing platform
- Lightning-fast and easily customizable chip assembly process
- Accurate, fast debugging for the most complex designs
- Tight integration with the Calibre platform provides a full range of signoff-quality verification features
- Rapid layout review handles the largest files with ease
- Fast and easy navigation for viewing/zooming/panning layouts

Features

- Express drawing engine
- Extremely fast database merge with minimal memory
- Loads massive files in seconds on typical workstations
- Fast, flexible overlay and compare functionality
- Fast layout viewer integrated with lithography simulators and editors supports GDSII and fracture formats
- Full range of advanced debugging capabilities

Fast and flexible chip finishing platform

The Calibre® DESIGNrev™ platform loads and displays the largest layouts on a typical engineering workstation in seconds. Incremental loading capability provides a scalable solution that is less dependent on I/O, and more efficient for multi-site collaboration. The Calibre DESIGNrev platform also provides an extensive set of debugging features, including net extraction and visualization, overlay, and editing. Users can directly manipulate native GDSII/OASIS database objects such as cells, instances, polygons, edges, and text. The Calibre DESIGNrev net extraction and editing features provides easier setup and migration between process nodes for CAD engineers, as well as accurate, easy-to-use net visualization. Its extensive capabilities, combined with its user-friendly design, make the



Calibre DESIGNrev robust and flexible chip finishing and review capabilities provide design teams a platform to integrate large GDSII or OASIS files and verify tapeout requirements with Calibre confidence.

Calibre DESIGNrev

Features *continued*

- Extensive batch and interactive editing
- Calibre WORKbench TCL/TK API
- Support for GDSII, OASIS and Gzipped layouts
- Fast database format converter and optimizer
- Direct read LEF/DEF, OpenAccess, and Milkyway
- Signoff DRC with Calibre RealTime integration

Calibre DESIGNrev platform the high-performance choice for fast, accurate, and efficient chip tapeout preparation.

High performance rendering
Rapid rendering delivers rapid zoom/pan visibility. Set individual layer characteristics for customized viewing needs.

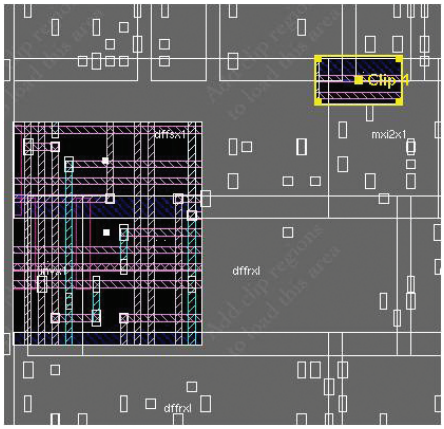
- Enable/disable individual layer visibility
- Enable/disable individual layer selectibility
- Set custom layer color, fill pattern, and line width
- Sort layer list by name, context, and other options

Lightning-fast data merge
Effectively manages the most challenging chip assemblies with its ability to process massive databases in very short runtimes while using a small memory footprint.

- Merge 10Gb of data in as little as 5 minutes
- Supports GDSII, OASIS, and GZipped layout inputs
- Comprehensive single pass file merging support all use models
- Optional SmartDiff technology replaces duplicate cells for smaller output file size

Unlimited capacity with incremental loading
Incremental loading capabilities lower resource requirements and improve efficiency for targeted viewing requirements.

- Unlimited capacity allows users to load multiterabyte layouts on typical engineering workstation in seconds
- Shared cache file efficient for multi-site collaboration



Clip layout to load, view, and save hotspots as needed.

- Less dependent on I/O because less data is transmitted
- Load, review and manage polygons and hotspots as needed

Flexible chip review with overlay
Allows users to place two or more layouts in one canvas, making it easy to perform a variety of chip finishing functions:

- Visualize layout differences
- Assemble block-level designs as chip-level configuration
- Measure alignment of MDP files
- Shift, magnify, rotate and mirror a single layout

Superior layout manipulation debugging capability
Provides a full range of advanced debugging capabilities. The extensive debugging feature set in the Calibre DESIGNrev platform includes:

- Trace net connectivity by user defined connectivity or properties
- Highlight extracted nets in a region
- Extraction of entire net or nets in selected region

- Find shortest point-to-point path through connected objects
- Edit native GDSII or OASIS layouts from the GUI or batch

Calibre WORKbench TCL/TK API extension

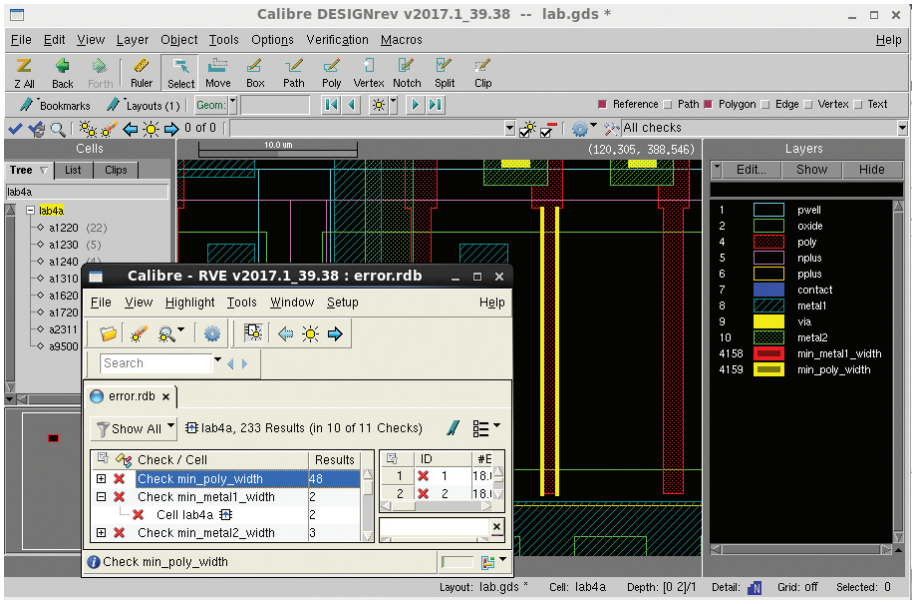
With its support of open standard TCL/TK, the Calibre DESIGNrev platform makes it easy for users to customize and simplify their chip finishing process:

- Fast/flexible batch processing for GDSII/OASIS data with scripting
- Extensive TCL command interface supports customized flow automation
- TCL-based object iteration and attribute queries

Tight Calibre integration

The Calibre DESIGNrev platform is part of the Calibre nm Platform, the industry's leading physical verification platform, providing users a full range of signoff-quality verification features:

- Calibre's best-in-class performance, accuracy and reliability delivers Calibre sign-off quality and confidence
- Calibre RealTime in-design DRC – invoke realtime signoff DRC checks during design



Navigate through layouts quickly and easily with the Calibre DESIGNrev platform.

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