TRANSFORMING IC DESIGN FLOWS WITH CALIBRE

JEFF MILLER, PRODUCT MARKETING AND STRATEGY, MENTOR GRAPHICS

WHITEPAPER

Mentor Graphics®

AMS DESIGN & VERIFICATION

www.mentor.com

INTRODUCTION

The Tanner IC design flow provides a complete, top-down solution from schematic capture and mixed-signal simulation, to full chip assembly and physical verification. Integrating Calibre® into this design flow provides you with the confidence that you will successfully tape out your design using the latest technology from your chosen foundry. With the click of a button, you can interact with:

- *Calibre nmDRC™*: to ensure that your physical layout can be manufactured. Using accurate and proven rulesets from the foundry, quickly debug violations for physical verification signoff.
- *Calibre nmLVS™*: to check that your physical layout is electrically and topographically the same as your schematic. Calibre nmLVS provides actual device geometry measurement, programmable electrical rule checking, and sophisticated interactive debugging capabilities to ensure accurate circuit verification.
- *Calibre xRC™*: to verify that layout-dependent effects do not affect the electrical performance of your design. Calibre xRC delivers accurate parasitic data for use in comprehensive post-layout analysis and simulation.

Calibre is the overwhelming market share leader for IC verification and signoff providing accurate and reliable solutions that ensure successful tape outs. Every major foundry uses Calibre nmDRC for process development and validation. This means that Calibre rule decks are proven long before you need them. Calibre nmLVS delivers the trusted device recognition accuracy and timely execution required for world-class silicon delivery. And, every major foundry defines extraction rules for Calibre xRC based on leading-edge processes descriptions.

UNDERSTANDING THE FLOW

When using L-Edit to define your design layout, you can access the Calibre toolbar to perform DRC, LVS, or parasitic extraction (Figure 1). After the run, Calibre RVE™ provides a graphical debugging environment that allows you to track down and fix any issues.

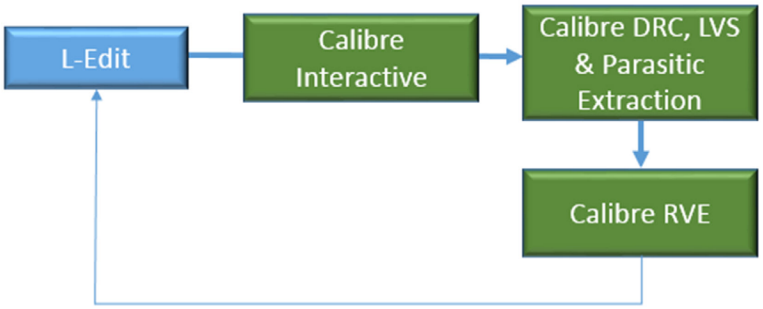

Figure 1: The Calibre flow.

ACCESSING AND USING CALIBRE INTERACTIVE

The Calibre toolbar within L-Edit invokes Calibre Interactive for DRC, LVS, or parasitic extraction. Based on your current layout, L-Edit pre-populates the dialog boxes. For example, Figure 2 shows a DRC run.

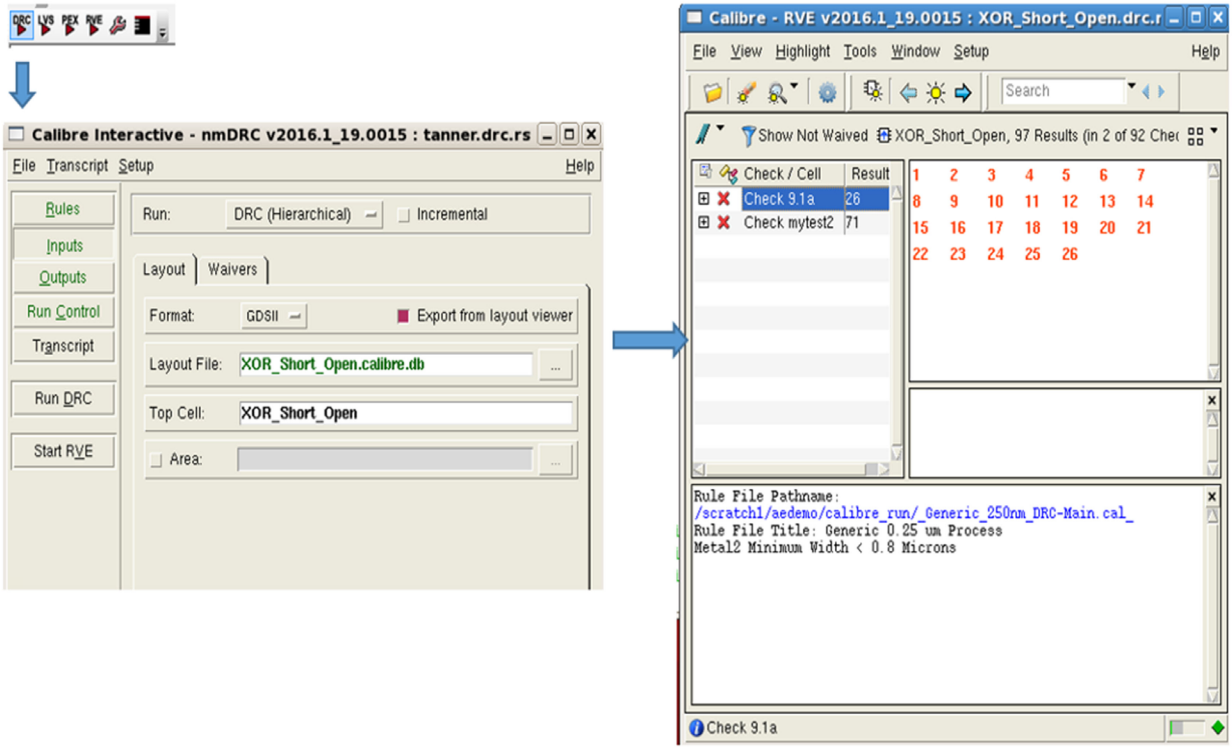

Figure 2: Sample DRC run.

Calibre Interactive allows you to set up the tool, define inputs and outputs, and specify options before running the Calibre tool that you choose.

DEBUGGING DRC VIOLATIONS

Based on rules defined by foundry process data, your physical layout could have violations that can prevent successful manufacture of your design. For example, you could have metal widths that are too small. Clicking on the violation in Calibre RVE, highlights the violation in L-Edit. Figure 3 shows a metal width violation that you can correct by resizing it.

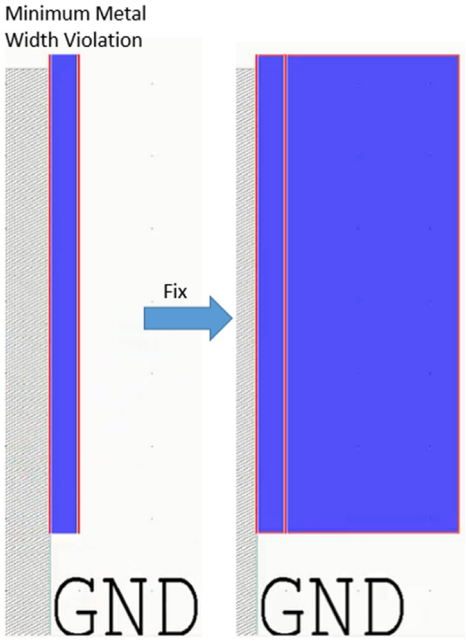

Figure 3: Detecting and fixing a metal width violation.

Another common DRC violation occurs due to improper spacing between layout elements. For example, Figure 4 shows a spacing violation between two metal polygons. Moving one of the polygons to another location fixes this violation.

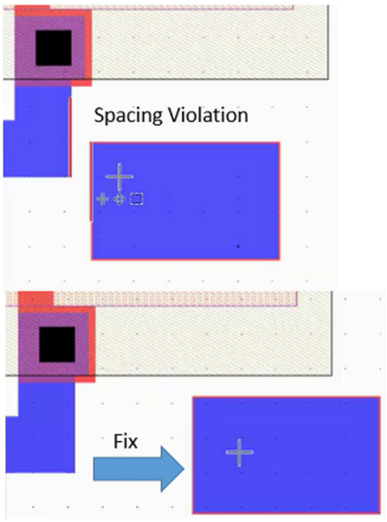

Figure 4: Detecting and fixing a spacing violation.

You can find additional information in the auxiliary RVE database to help you quickly fix violations. For example, you can report additional statistics such as area and perimeter of each layer of interest to help fix antenna and density violations (Figure 6). Figure 5 shows an antenna report with violations sorted on a per-net basis. You can fix this violation by either shortening the antenna path with a connection to a higher metal layer, or by connecting a

diode to the net. The area information in the report gives you an idea of how much antenna path you need to shorten.

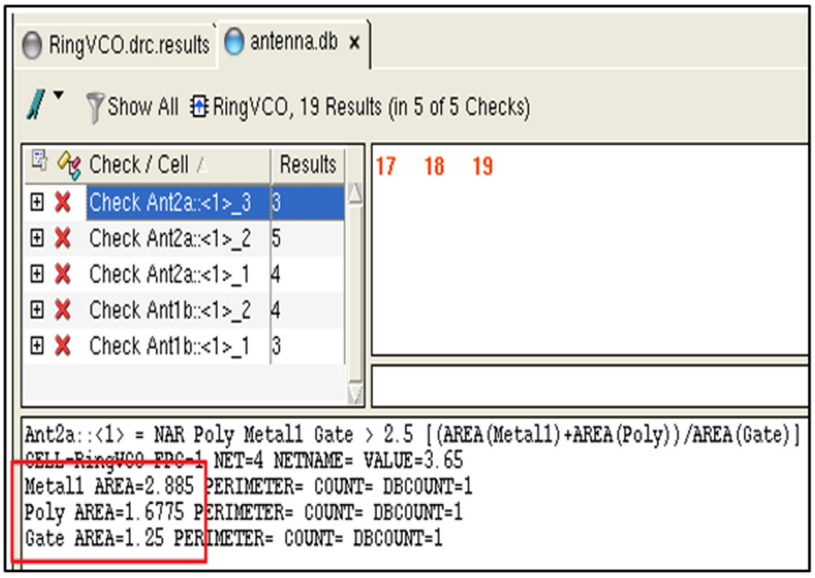

Figure 5: Antenna report showing additional statistics.

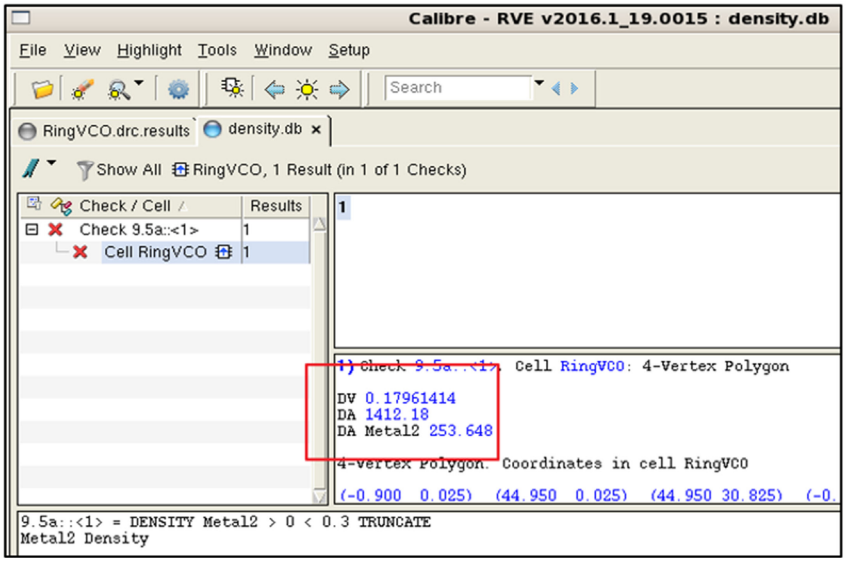

Figure 6: Density report showing the calculated density value (DV), window area (DA), and metal density (DA Metal2).

DEBUGGING LVS PROBLEMS

Launching Calibre nmLVS sends both your schematic and layout to the tool for analysis. This analysis can result in errors due to the extraction process and the schematic versus layout comparison. For example, the extraction process could reveal a short. Figure 7 shows a detected short in the layout between an input and output port. To fix this problem, you remove the metal causing this short.

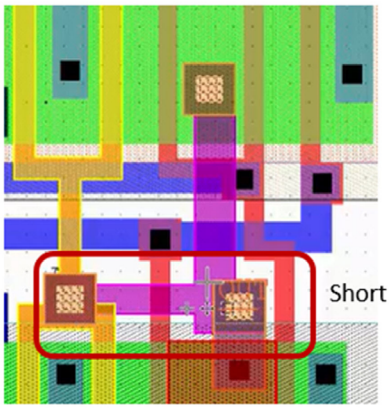

Figure 7: A short detected by LVS.

Figure 8 shows a LVS comparison problem. On the schematic, there are two pairs of transistors connected in series, but the layout shows all four transistors connected in series resulting in instance mismatches between the schematic and the layout. In this example, there is a problem in the layout to investigate.

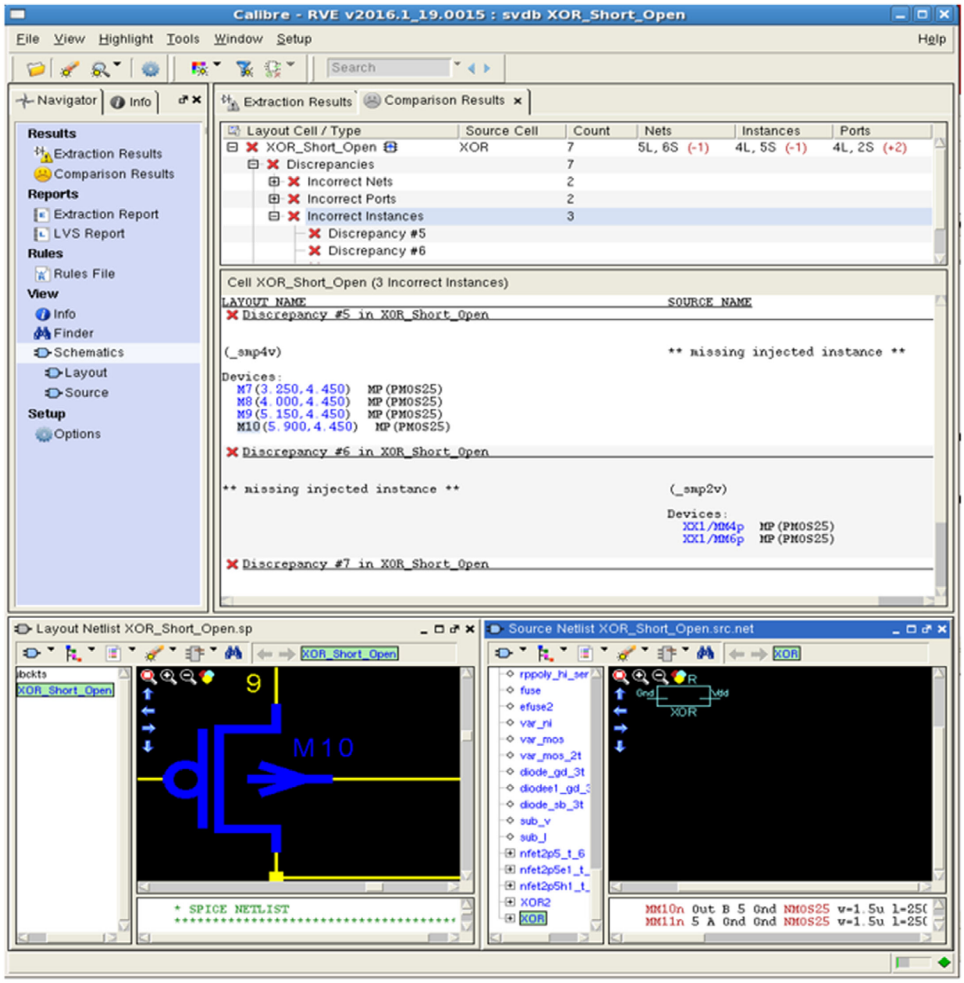

Figure 8: LVS comparison results.

Figure 9 shows that by using the L-Edit capability to turn on and off layers, you can isolate the problem by viewing the Active and Contact layers together. In this example, there is a missing contact for the source to drain. Adding a contact resolves the problem.

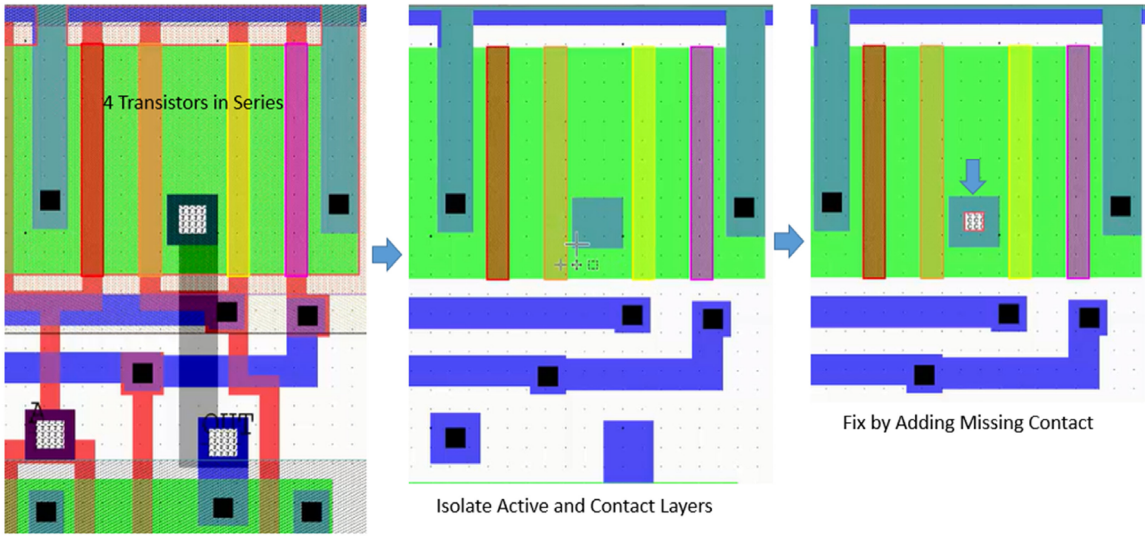

Figure 9: LVS instance violations

PERFORMING PARASITIC EXTRACTION

Launching Calibre xRC for parasitic extraction from the L-Edit toolbar allows you to specify what type of extraction that you want the tool to perform. For example, you might only want to extract resistance (R), only capacitance (C), or both. When you initiate the run, Calibre performs LVS analysis first. So, if you have any LVS errors, you should address those problems first, then re-run xRC. You can view the results in Calibre RVE.

After a successful extraction run, you can drag and drop the SPICE netlist file that Calibre xRC generates into T-Spice in order to analyze the impact of the extracted data. Typical analysis includes examining delay impact, parasitic effects on critical nets, and power issues.

You can review the parasitics report (Figure 10) in Calibre RVE, sort the results based on the net, resistance count, or capacitance value. By double-clicking on an entry, you can calculate point-to-point resistance for a particular next and highlight the resistance path in L-Edit.

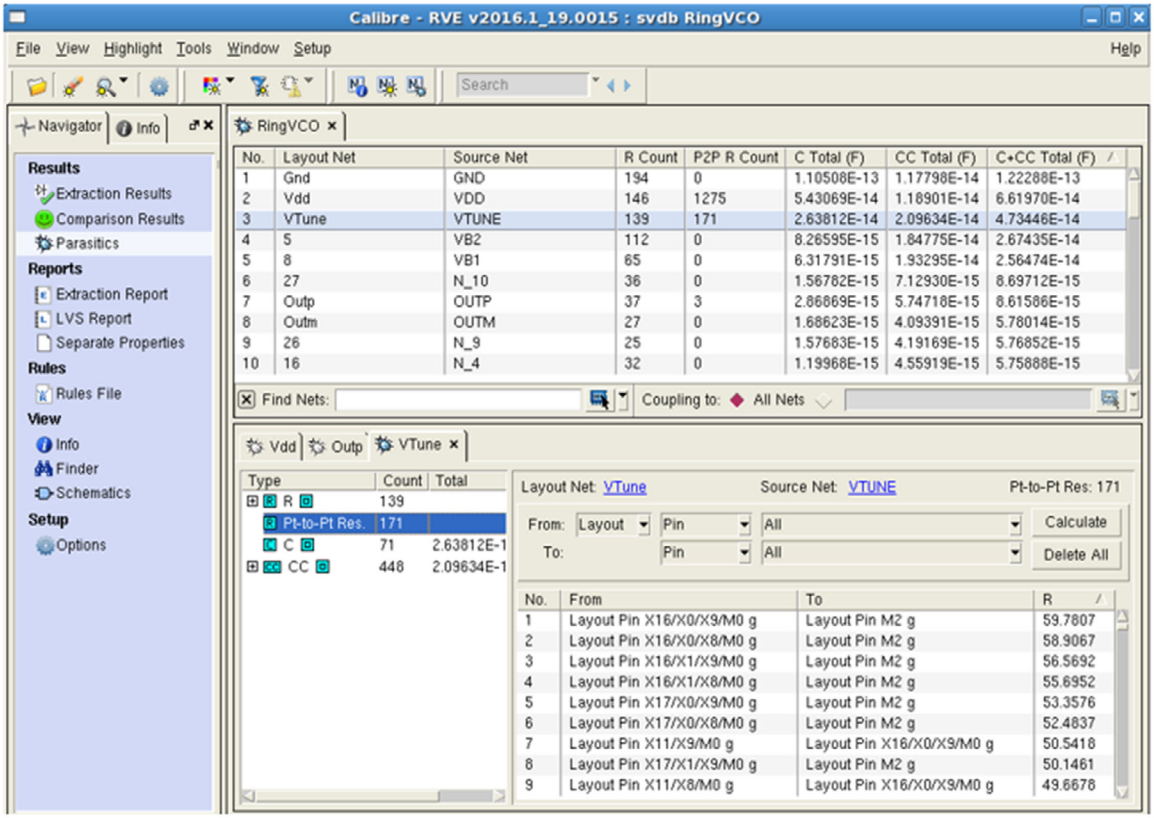

Figure 10: Extraction results in Calibre RVE.

CONCLUSION

The integration of Calibre into the Tanner design flow brings a world-class IC verification solution to bear on your design. You can detect problems in your layout using rulesets from every major foundry, compare your layout to your schematic in order to detect problems, and run parasitic extraction for post-layout analysis and simulation. Using Calibre in your design flow gives you confidence that you will achieve successful tape outs. For more information about the Tanner design flow, visit: https://www.mentor.com/tannereda/

For the latest product information, call us or visit: **www.mentor.com**

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

MGC 6-16 TECH14320-w