Tanner Analog/Mixed-Signal IC Design Flow
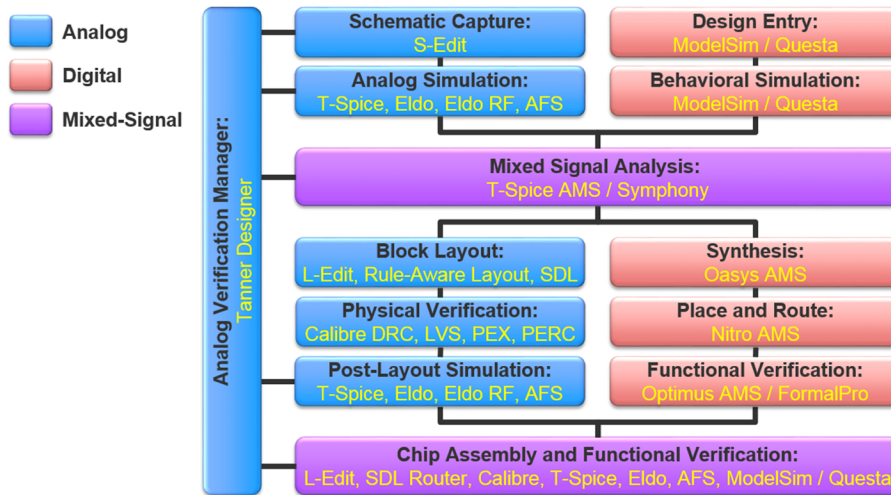
End-to-end design flow for analog/mixed-signal IC Design.

The Full Flow AMS Solution

Tanner EDA provides a complete end-to-end analog/mixed-signal (AMS) design flow for IC design. The flow is optimized for creating custom analog or "Analog on Top" mixed-signal ICs, working at 28nm and above. The flow is used in a wide variety of markets including: automotive, Internet of Things (IoT), imaging/display, industrial control, medical, sensors, automotive, RF, space, and power management.

The Tanner AMS IC design flow consists of highly-integrated front and back-end tools, from schematic capture, to mixed-signal simulation and waveform probing, viewing, and RTL netlist synthesis; to physical layout, place and route, static timing analysis, and foundry-certified physical verification.

Considered together, these tools comprise a suite that is interoperable with many popular industry tools and industry-standard file formats and the suite minimizes risk by providing foundry support. The tools are intuitive, easy to use, and accessible from anywhere because they are available for both Windows® and Linux®.

FEATURES AND BENEFITS:

- Complete, full-flow analog/mixed-signal IC design suite
- OpenAccess native database
- Simulate combined netlists at various abstraction levels: behavioral models, block-level RTL, gate- and transistor-level blocks
- Debugging and advanced verification with SystemVerilog, Verilog, Verilog-AMS, Verilog-A, and VHDL
- Rule-aware layout editor
- Run Calibre® nmDRC™, nmLVS™, RVE™, xRC™, xACT™, 3DSTACK™, PERC™, DFM™ directly From L-Edit
- Full digital flow with Oasys™ synthesis and Nitro™ place and route
- Static timing analysis with Optimus™
- Flexible revision control interface, including direct integration with ClioSoft®
- Foundry PDK support
- Available on Windows and Linux
- Intuitive and easy to use; quick learning curve

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Complete IC Design Capture Environment

Tanner S-Edit is an easy-to-use design environment for schematic capture and design entry. It provides the powerful features necessary to handle the most complex mixed-signal IC design capture, including:

- AMS simulation integration and waveform cross-probing

- Direct viewing of operating point simulation results in the schematic

- Cross-probing between schematic, layout, and LVS report with net/device highlighting

- Configurable schematic Electrical Rule Checks (ERC)

- Advanced array and bus support

- Integrated with Tanner L-Edit IC to speed the layout and ECO process

Complete IC Physical Design Environment

Tanner L-Edit IC is an AMS IC physical design environment that provides all the features necessary to quickly and efficiently finish the layout of the design, including:

- Fast rendering

- Rule-Aware Layout to quickly create a compact layout

- Parameterized layout generators for fast device layout that is DRC correct

- Schematic Driven Layout (SDL) capability that automatically generates parameterized cells and instances in the layout from the schematic including flylines and assisted manual routing

- Node highlighting for connectivity visualization

Fast, Accurate Simulations for AMS IC Designs

Tanner T-Spice AMS simulation provides fast and accurate simulation for AMS IC designs. T-Spice AMS not only simulates circuits quickly and with a high degree of accuracy, but it is also compatible with industry leading-standards and it integrates easily with the Tanner S-Edit schematic capture tool and Tanner Waveform Viewer.

Co-simulation combines the high speed of event-driven digital simulation for the digital portions of the design with detailed continuous-time analog modeling in the SPICE engine for maximum mixed-signal performance.

Complete Digital Design Flow

Tanner Digital Implementer (TDI), powered by the Oasys Synthesis and Nitro Place and Route engines, is integrated into L-Edit IC to address the physical implementation of the digital portion of "Analog on Top" designs.

TDI provides a cost-effective, easy to use digital synthesis and place & route solution with powerful features including:

- Intuitive and quick learning curve for synthesis and place and route

- Oasys optimizes RTL partitions for placement, timing, power, area, and congestion with fast run time. Its power-aware synthesis and power analysis can achieve comprehensive power management solutions, including clock gating and multi-threshold leakage optimization

- Nitro Place and Route provides high-capacity architecture and timing-driven and best-in-class physical implementation engines

- The Optimus static timing analysis tool validates all timing violations in full-chip, gate-level designs and checks all path timing violations using static timing analysis

For the latest product information, contact us at: www.mentor.com, (800) 547-3000