DESIGNING THE WORLD'S FIRST INSTANTANEOUS LOCK LOOP USING THE TANNER DESIGN FLOW

A M S D E S I G N & V E R I F I C A T I O N

C A S E S T U D Y

INTRODUCTION

Instantaneous Technologies is an integrated circuit (IC) design company that leverages decades of high- profile analog IC design and physical layout experience to overcome well known limitations of existing circuit architectures and to innovate huge leaps in performance. These quantum advances are offered as intellectual property in the form of GDSII stream-out files, netlists, documentation, and one-on-one consultation to ensure optimal integration into existing projects.

"The flexibility, apt simulation, and graphical features of Tanner tools have allowed us to rapidly design, verify, and document our novel phase tracking phase lock loop (PLL) with quantum advances. The ease of use, simplicity, and yet comprehensive set of exactly-what-is-needed features in S-Edit, T-Spice, the Tanner Waveform Viewer, and L-Edit facilitated the fast development of wholly-new circuit architectures. These same tools allow us to easily port into new process nodes. Subsequently, Instantaneous Technologies offers quantifiably large benefits to practically all ICs through advanced IP blocks," according to Jed Griffin, Chief Technical Officer.

INHERENT PLL LIMITATIONS

Most IC designers grapple with PLL designs and learn to deal with:

- Stability issues of typical PLLs.
- The large footprint needed for large loop filtering.
- Simulation times of a week or longer necessary to get PLLs with millisecond lock times to converge, if they even have the resources and time to do a typical full loop simulation, let alone simulate skew corners.
- The back and forth iterations between tradeoffs that also stretch out the design cycle.

The joke within a large engineering team at a well-known semiconductor company, about a microprocessor PLL that sold hundreds of millions of units, was that there were only a few things one could see from space: the Great Wall of China, the Great Barrier Reef in Australia, and this particular microprocessor's PLL (with large loop filter). The joke was not appreciated at the time by the team. With the help of the Tanner design flow, Instantaneous Technologies now has the only PLL that cannot be seen from space, that entirely eliminates the need for loop filter capacitors and the very large capacitors required for PLL stability. This PLL attains nearly instantaneous acquisition/lock time (8 ns), which is millions of times faster than other implementations and is indicative of the wide tracking bandwidth (100s of MHz) of an ideal PLL. The new instantaneous lock loop (ILL) improves both system price and performance and enables new applications previously impossible due to PLL limitations. No company has been able to accomplish this before now, despite considerable effort and numerous attempts.

AN IDEAL PLL

An exciting new and revolutionary phase tracking, ultra phase coordination (UPC), enables quantum leaps in PLL performance in a new ILL. One advantage this provides is that development time is a small fraction of that for typical PLLs. The ILL can be simulated from startup to lock in less than half an hour using T-Spice, versus longer than a week for typical PLLs. Typical PLLs are often not even simulated as a full loop due to the prohibitive run times required to achieve lock. The ease of use of the Tanner tools and T-Spice numerical methods help this improvement, but this simulation speedup is mostly a function of the very fast ILL acquisition time. The Tanner Waverform Viewer readily displays simulation results in a useful set of frequency-specific plot features, including a frequency-to-time plot that is not readily available in other simulation environments. Additional advantages of the ILL design relative to typical PLLs are:

- Dramatic reduction in design and simulation time.
- 8 nanosecond acquisition/lock time, with power savings proportional to system size.

- Elimination of jitter peaking and jitter accumulation, resulting in 100 times less phase noise.
- 1/50th the die area, leading to negligible implementation cost.
- Ideal phase tracking, to pass through low phase noise or modulation of reference.
- Rapid porting to new process nodes.

Figure 1 shows the ideal phase coordination of the ILL versus the inherently and severely-hampered phase tracking of existing methods. As loop gain increases for the ILL, ideal phase tracking and ultra-phase coordination is achieved while eliminating jitter peaking. Any shift, δ, at any frequency on the reference phase replicates exactly the same on the tracking phase. As loop gain, G, increases to improve phase tracking in typical PLLs, the loop becomes proportionally unstable, leading to jitter peaking. To avoid this instability, loop gain in typical PLLs is kept extremely low, typically by using a large loop filter capacitor. By keeping loop gain low, the reference phase is essentially not being tracked, and the loop takes seconds or milliseconds to converge. This makes the PLL more susceptible to jitter accumulation and unpredictable jitter throughout the loop caused by device noise or power supply noise entering the loop. In the case of frequency synthesis, the low phase noise of the reference phase from a crystal is blocked by the loop filter, imposing the higher phase noise from jitter accumulation and the voltage controlled oscillator on the output clock.

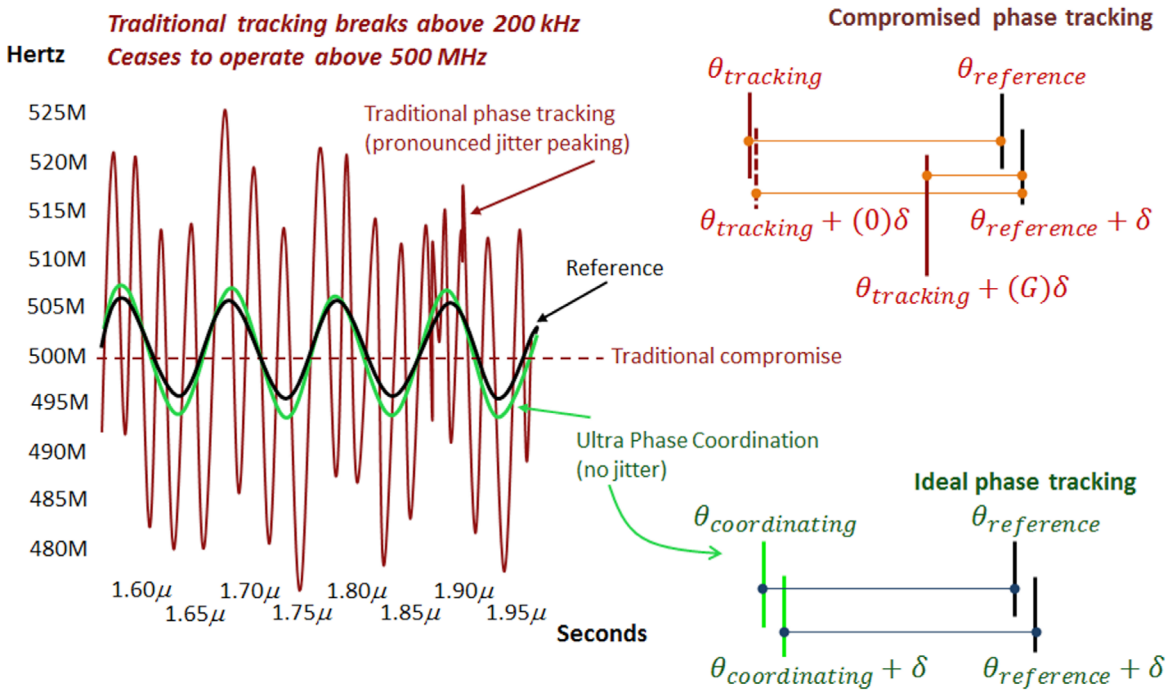

Figure 1: UPC, ideal phase tracking.

Jitter transfer function (JTF) plots more succinctly convey the advantage of the ILL (Figure 2). As loop gain, α, increases, UPC phase tracking improves, in contrast to the decreasing phase tracking of traditional methods. Thus, the ILL eliminates the tracking bandwidth to loop stability tradeoff and the multiple design iterations needed for optimization around this tradeoff. This results in a huge time reduction in the design cycle.

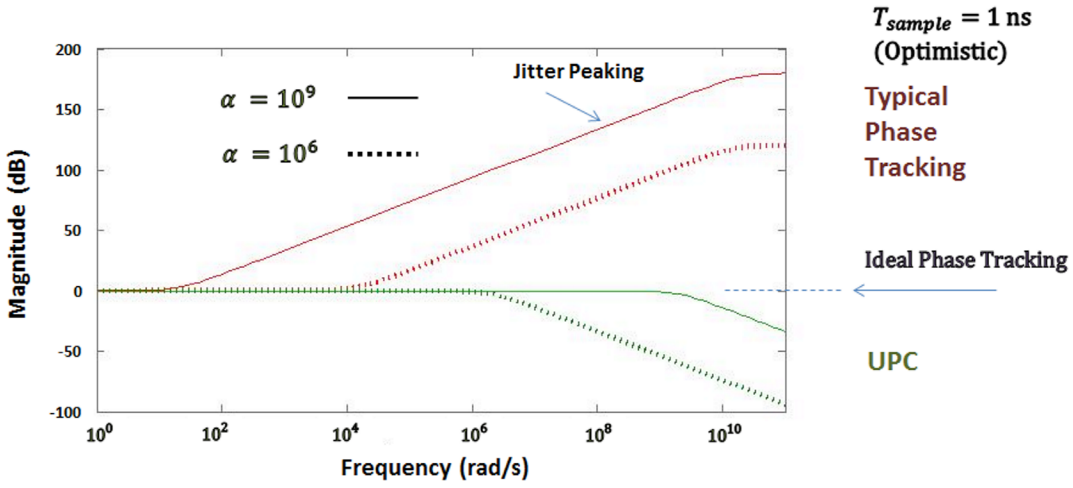

Figure 2: UPC improves tracking as loop gain increases, opposite of typical PLL.

Figure 3 shows the coordinating bandwidth of the ILL in very useful direct plots of frequency available within the Tanner Waveform Viewer. In particular, the direct frequency-to-time plot makes ILL development easier.

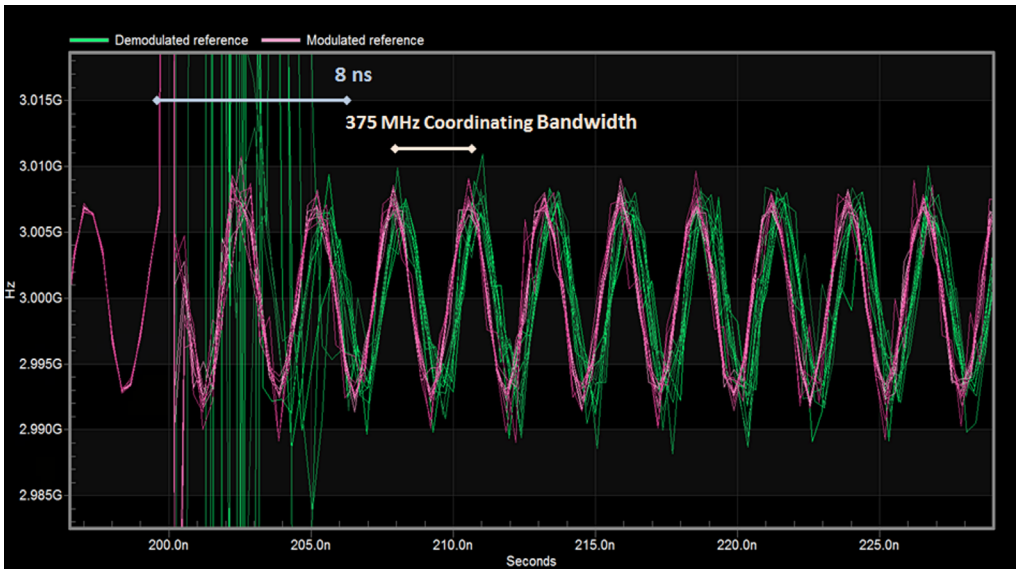

Figure 3: ILL acquisition time and coordinating bandwidth showing orders of magnitude improvement.

Simulations at 55 nanometers of an ILL locking were performed across temperature ranges for military specifications and 3-σ skewed material to validate robustness and to show convergence in 8 nanoseconds, which is millions of times faster than typical PLLs. Normal simulation times for PLLs take weeks to lock, if these full loop simulations are even performed due to prohibitive run times for low nanosecond time intervals across high millisecond of second converge times. The coordinating (tracking) bandwidth can readily be seen to be 375 MHz, which is 2500 times greater than a typical PLL. This is possible due to UPC. The tracking bandwidth scales with the reference frequency and it can exceed 1 GHz in more integrated process nodes.

Phase noise (Figure 4) was measured from non-optimized but identical loops, except for separate phase detection, for both the ILL and a typical PLL. A fast Fourier transform (FFT) integrated into the Tanner Waveform Viewer expedited the generation of phase noise plots by reducing the data size by orders of magnitude which allowed easy data extraction for further processing. The ILL shows 100 times less phase noise which allows designers to increase timing margins for clock distribution or to allow for increased clocking frequency.

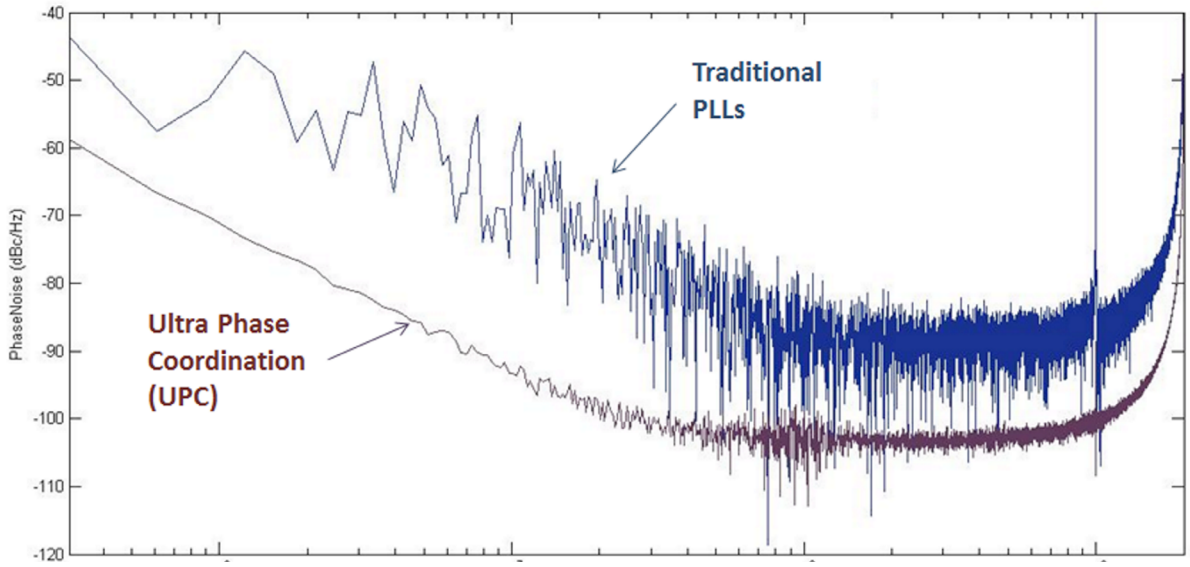

Figure 4: ILL reduces phase noise.

While frequency aliasing is a problem with conventional PLL designs, the ILL is free from aliasing by design. In addition, the related harmonic distortion can be an impediment to some PLL applications because the first and second harmonics are often as high as $1/10^{th}$ the power of the reference signal. The ILL eliminates harmonics by design.

IP PORTABILITY

The absence of the typical large loop filter in the layout for a 55 nanometer ILL from the L-Edit plot is evident (Figure 5). L-Edit, along with the tools used for circuit design and simulation, proved to be straight-forward and just what was needed to get the task completed expeditiously. The significantly smaller layout size (in the micrometers squared range), also aids in portability and usability. For example, the small size ensures that long routes into the ILL are not needed for high-frequency signals. The less stringent requirements on the device matching and routing in physical layout translate into much faster implementation into new process nodes (portability) with the easy to use features of L-Edit aiding as well.

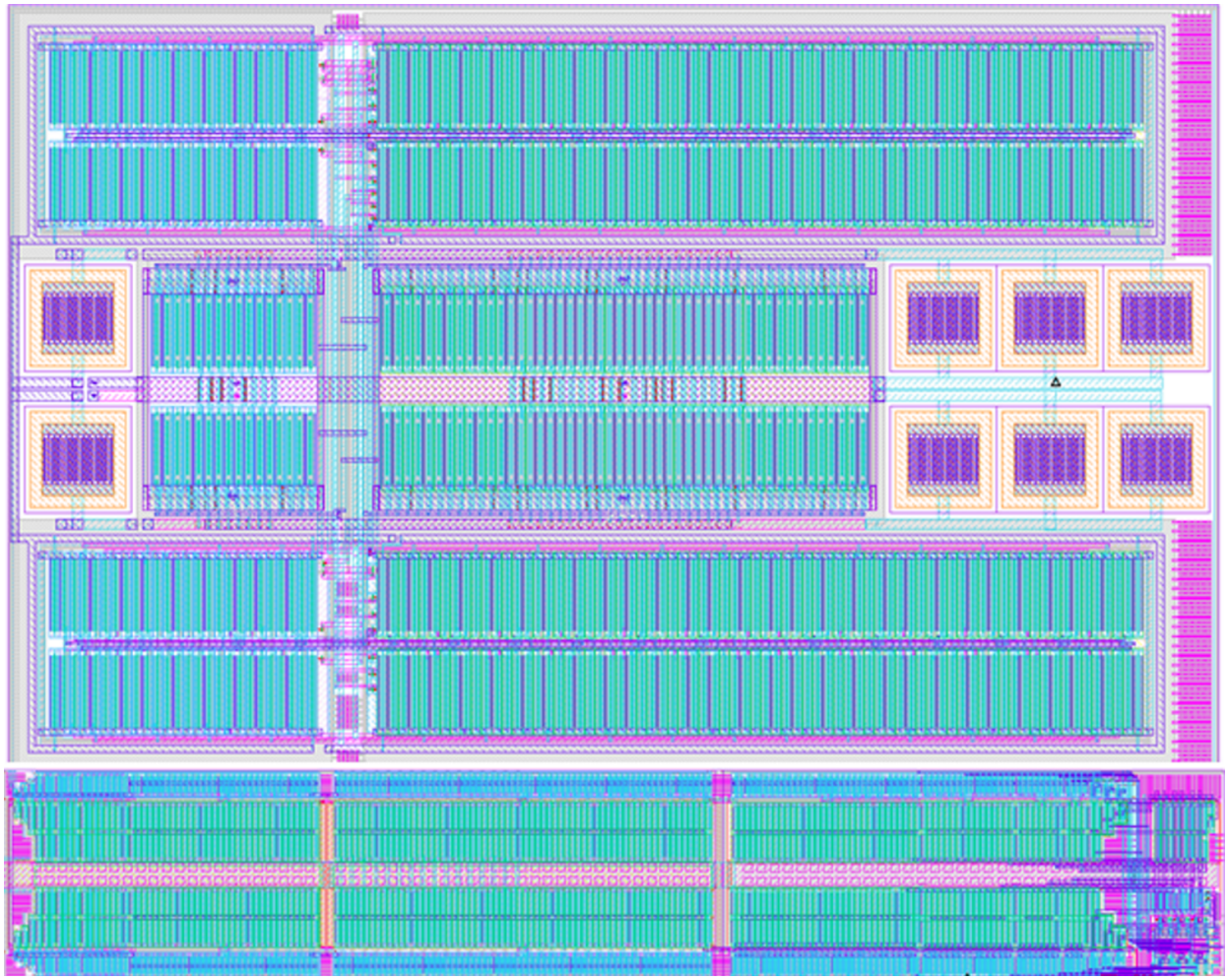

Figure 5: ILL physical layout.

Given the 8 nanosecond acquisition time of the ILL, full loop simulations can be performed 100,000 times faster using T-Spice and the Tanner Waveform Viewer, as demonstrated in 180 and 55 nanometer processes. The millions of times shorter run times of the ILL allows for even more comprehensive functional verification across more robust skew corners than is currently possible with existing PLLs. Because of the quick acquisition time, the ILL can also be simulated with entire clock distribution and system blocks simultaneously, with more a comprehensive view of interfaces and performance. Also, given the much greater loop stability, less attention to detail and time has to be spent on physical layout than that required by traditional PLLs. These two key features, unique to the ILL, also allow very rapid portability of IP to any target process node which reduces production costs. The low cost coupled with ideal phase tracking and subsequent performance advances, make the ILL an ideal replacement for traditional PLLs in ubiquitous use now, that define the clocking of almost all integrated circuits in use, for radios, telecommunications, and computers.

MATCHING THE MATH

Oscilloscope JTF measurements were performed on silicon that showed 0.02% jitter across 200 kHz, but ironically existing test equipment can only measure to 200 kHz, nowhere near the 600 MHz that the ILL is capable of (3000 times slower than the ILL). Test equipment manufacturers did not anticipate ILL. Other measurements demonstrated that there is a good match between silicon and modelling.

Overall test results confirm that the best control of jitter for clocking applications is a loop with high gain that most accurately tracks the lowest jitter of all, that coming from a crystal. Why should designers use a relatively expensive crystal with low phase noise if they are just going to block it (negate the key advantage of the crystal) with an expensive large loop filter that is much more susceptible to noise from power supplies and CMOS devices in the loop? A much more elegant solution is to use the ILL, which can actually track the low phase noise of the crystal, eliminate the large capacitor in loop filter, and thus define tighter clocking. In other applications requiring tracking modulation on a reference signal, the ILL is the only solution. Add in 50 times or less die area, far less development time, and an 8 ns acquisition time (save power at startup) and the ILL, as an ideal PLL, is a superior solution for PLL applications everywhere.

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