ANALOG-TO-DIGITAL CONVERSION IS KEY FOR DEEP SPACE EXPLORATION WITH THE JAMES WEBB SPACE TELESCOPE

CASE STUDY

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Reflect back to your last design project. Did it have leading-edge requirements that seemed impossible at the time to fulfill? Now think about a design that needs to live in the harsh environment of space. A device that has to sip power and function flawlessly for over a decade because there is no opportunity to service it if anything goes wrong. That is the set of requirements that faced Dr. Lanny Lewyn, founder of Lewyn Consulting Incorporated (LCI), when his company was selected to design a key piece of the James Webb Space Telescope: an analog-to-digital converter (ADC) for an image system.

The next-generation successor to the Hubble Space Telescope (HST) is the James Webb Space Telescope (JWST). One of the two competitors for the JWST main near-infrared camera (NIRCAM) onboard electronic imager and signal processing system was Rockwell Science Center (RSC – now Teledyne). RSC selected LCI for the electrical design of the x36 19-bit ADC array included in its SIDECAR (System for Image Digitization, Enhancement, Control, and Retrieval) IC that will be mounted on the back surface of the imaging sensor array. Because of the extremely short development schedule, LCI was subsequently selected to also perform the physical design (layout) of the x36 ADC array.

By meeting performance and tight schedule requirements, the RSC SIDECAR chip with the LCI x36 ADC array was the winner of the NASA JWST competition and it has passed all acceptance tests in preparation for the 2018 launch.

While construction of the JWST was underway, a failure occurred in the electronics system for the Hubble Space Telescope's Advanced Camera for Surveys (ACS) on January 27, 2007. The RSC-LCI SIDECAR chip set was selected to replace the original image processing system for the Servicing Mission SM-4 in May 2009. This Space Shuttle mission was successful and the x36 ADC array in SIDECAR currently processes all the image content from the 2 working channels of the ACS imager with lower noise and higher image fidelity than the previous electronics. Recently, the 25th HST Anniversary picture (Figure 1) was composed of images primarily from the ACS.

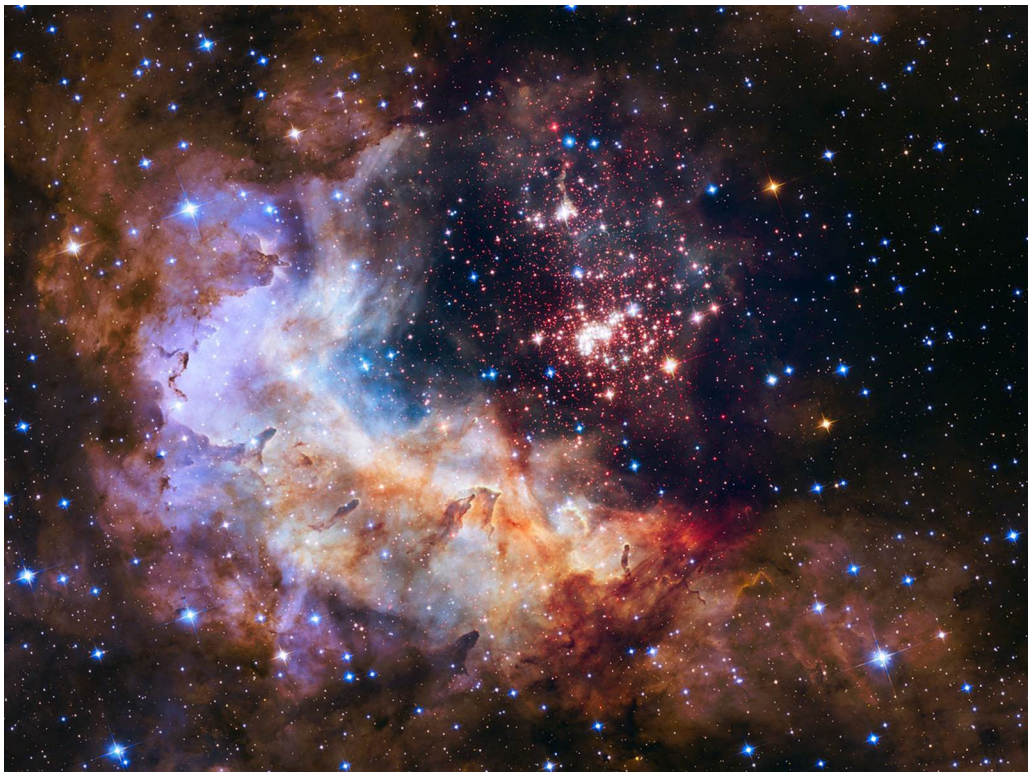

Figure 1: the Hubble Space Telescope's 25th Anniversary picture of Westerlund 2 in the Carina galaxy. The image's central region, containing the star cluster, blends visible-light data taken by the Advanced Camera for Surveys and near-infrared exposures taken by the Wide Field Camera 3. The surrounding region is composed of visible-light observations taken by the Advanced Camera for Surveys (Source: SpaceTelescope.org).

As a result of the excellent performance of the RSC SIDECAR chip, it will perform the image signal processing for 3 of the 4 instruments on the JWST (Figure 2). The JWST includes a 6.5 meter, segmented reflection mirror with a near-infrared camera (NIRCAM) that is optimized to operate in the 1-5µm wavelength region. Unlike the HST ACS, the near-infrared operation of the NIRCAM allows it to peer substantially farther through the dark-matter clouds of the extra-galactic universe. It can see farther in time to the epoch of 'first light' and to the birth of the very first stars. Because the JWST will be placed in a gravitational balance point, approximately a million miles from Earth, it cannot be serviced after launch. To avoid undue consumption of imaging detector cryogenic coolant for a 10 year mission, the ADC array must operate at extremely low power levels.

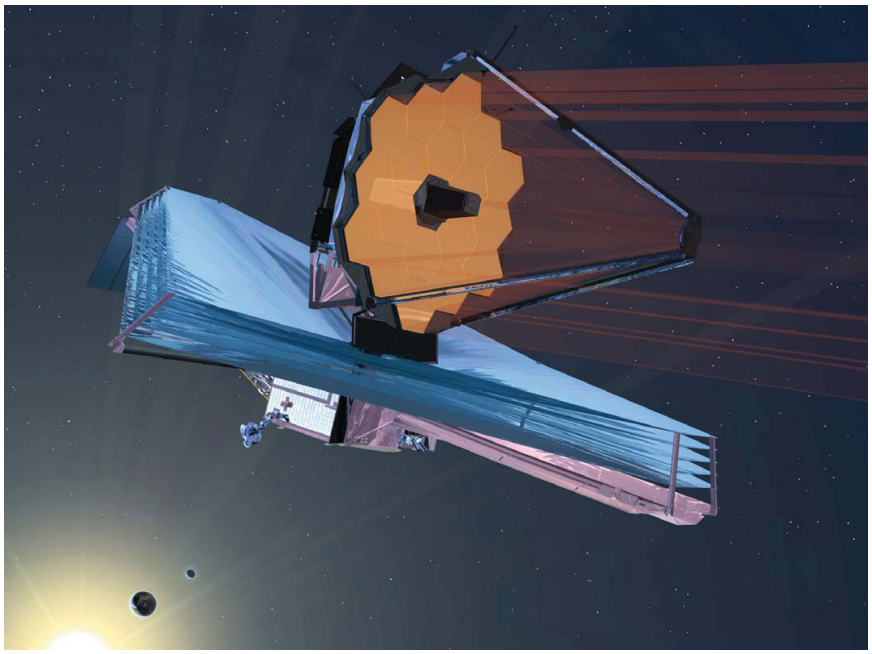

Figure 2: an artist's impression of the deployed JWST in L2 orbit showing the 6.55 m segmented telescope mirror and matching sunshade (Source: Northrop-Grumman).

A BRIEF HISTORY

LCI has developed a complete set of dimensionless schematic capture and layout techniques to rapidly port existing and new circuit elements to the fabrication technology selected by RSC for the JWST project.

"I believed that our dimensionless methodology would be the key to LCI completing the circuit and physical design within the timeframe needed by RSC to win the JWST sensor competition," said Dr. Lanny Lewyn, principal LCI engineer. "In the early days of LCI, we found that the Tanner L-Edit™ layout tool was especially suitable for our dimensionless layout technique."

It is no coincidence that the original developer of the L-Edit tool, Dr. John Tanner, and Dr. Lewyn, shared a common interest in dimensionless design. Both worked under the same advisor at the California Institute of Technology (CIT), Professor Carver Mead. At CIT, Professors Conway and Mead developed a dimensionless design and layout approach using a simple metric: Lambda - a dimension equal to 1/2 the minimum gate width. The Mead–Conway methodology enabled graduate students and engineers at Stanford and Xerox PARC in the 1980s to create the foundation system on a chip (SOC) technology for the computer market leaders at the time – Sun Microsystems, Silicon Graphics, Apollo Computer, and MIPS Computer Systems.

Following graduation, Dr. Tanner created the first generation of Tanner layout tools with dimensionless physical design capability based on either Lambda or micron dimensions. A key goal in the development of the Tanner

layout tools was to implement intuitive controls that could be easily operated by engineers with no previous layout experience.

The LCI dimensionless design methodology is based on Gamma rules that use a dimension equal to 1/4 minimum gate width. As a result, this methodology has evolved to meet the stringent gate pitch requirements of DUV lithography and it allows area-efficient physical designs created using L-Edit to cover a wide range of processing line widths from 180nm to 28nm.

CIRCUIT AND PHYSICAL DESIGN CONSIDERATIONS FOR THE ADC

The performance requirements for an ADC that processes signals from an exceptionally wide dynamic range sensor are much different from typical telecommunications signal processing. Telecommunication ADCs must achieve high differential linearity (DL) and integral linearity (IL) accuracy near mid-range, where the signal spends most of its time.

ADCs designed for image processors must have high accuracy at the low (black) end of the dynamic range. For space telescope applications, the linearity requirements are extreme. While a +/-2bit IL requirement for 16-bit resolution is sufficient to assure adequate performance near mid-range, the DL requirement for the JWST application was a maximum of ½ LSB at the low end of the range. Achieving high image fidelity with the extremely dark background of deep space requires that the ADC has a high DL accuracy (low noise) when the input signal from the imaging detector is just a few electrons. Overall DL inaccuracy contributors include:

- Preamp and ADC input noise
- DL channel width (quantization "q" step) variations
- ADC resolution-limited quantization noise

Because the ADC quantization noise contribution is equal to approximately 1/3 "q" step [specifically q/sqrt(12)], the ADC must be designed to a resolution specification of 19-bits in order to keep the 16-bit-equivalent quantization noise well below the level of the other contributors.

Unfortunately, foundry-supplied precision capacitors in process design kits available for most technologies do not have the precision required to achieve 16 +/- 2 bit IL without using digital calibration. Dynamic digital calibration methods for signals with Gaussian distributions will not work with the asymmetrical characteristics typical of deep space image signals. These methods also require extra area and power. For a 10 year mission without cryogenic re-supply, the maximum power allocated for each ADC in the x36 array is 1.5mw. Most analog CMOS ADCs with resolutions beyond 12-bits require digital calibration throughout the dynamic range. The physical design of the capacitor MSB weighting network elements to achieve the 16-bit IL accuracy requirements without dynamic calibration requires careful attention to every small detail.

According to Dr. Lewyn, "In order to achieve a suitable physical design for the precision capacitor, LCI relied on the simplicity of graphic and array-control features in L-Edit to layout the complex structure of the capacitor plate layers, external shields, and interconnects. In addition, several layers ancillary to the basic capacitor layout (such as implants) could be generated using the Boolean layer generation features in L-Edit to perform a variety of AND/OR/NOT functions along with the layer resize functions to comply with foundry technology-scale design rules and manufacturing grid constraints at the mask level."

An important aspect of the physical design was the requirement to minimize the effect on precise capacitance value from lithographic variations local to the individual capacitor layout patterning as well as first and second order effects from process variations across the chip. In order to satisfy all of the design constraints, it was necessary to develop both precise capacitor and MOS device patterns that could allow placement of each in uniform pitch patterns in both X and (as much as possible) Y directions. To satisfy the uniform pitch requirement, a

precise capacitor pattern including capacitance layers, shielding, and interconnect, was developed that had a recurrence of precise, multiple of 4 MOS device patterns. In order to fit amplifier, switching, gating, and logic subcircuits into the regularity of the capacitor patterns, a uniform subcircuit width was maintained equal to the pitch of 4 capacitors, or 16 devices (Figure 3).

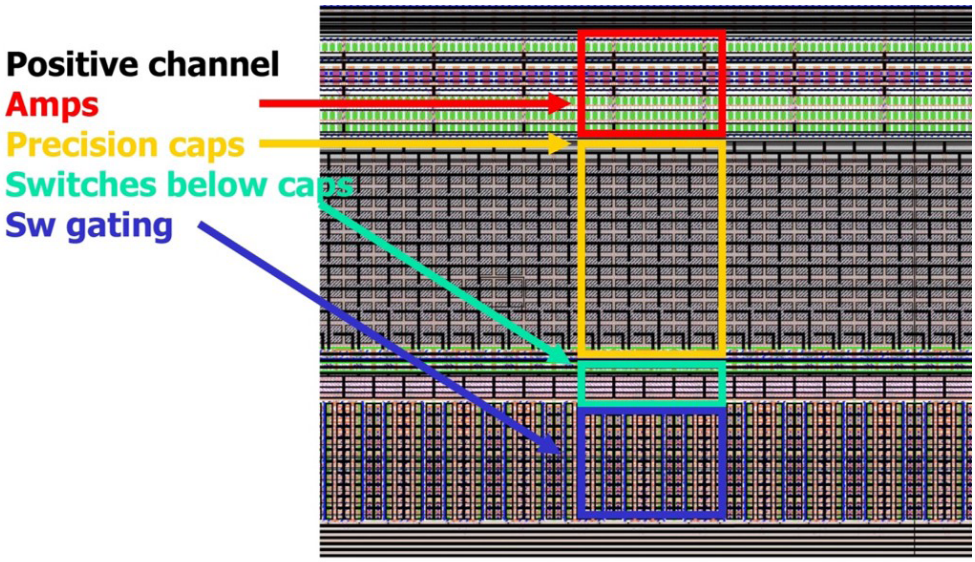

Figure 3: a section (approximately 20% of the total X-dimension) of the HST-JWST ADC with precise capacitor selection in the X direction.

DIMENSIONLESS PHYSICAL DESIGN AND SPECIAL TOOL REQUIREMENTS

"Any design project is bound to encounter some unusual problems along the way to completion. In this case, the physical design of the standard amplifier, capacitor, switch gating, and logic subcircuit cells in an overall cell pitch of several devices can create some interesting, but solvable, problems at the metal wiring connections joining each cell," stated Dr. Lewyn.

While L-Edit scale setting can easily place the physical design captured in Gamma units precisely on the foundry manufacturing mask grid, the scale setting invariably has a value far less than unity. The Scale command assures the application of a uniform 'magnify' value across the database. However, subsequent to the magnify operation, it is necessary to resize some individual layers with commands that either expand or shrink the layer. If metal layers must be shrunk by a small amount, small gaps in the database might be created. While it is no problem to expand the polygons in individual layers to overlap, and subsequently shrink the overlapped polygons that would be then connected, such operations usually require the database to be flattened. Flattening greatly increases the size of the database as much as a factor of 10 in very hierarchical designs, such as the ADC.

For large ADC designs that are implemented in one physical location and transmitted to verification tools located in another location, the flattened data transmission time took several hours. In order to solve this problem Tanner stepped in to help.

"The solution provided by Tanner is an example of one of the best customer support experiences LCI had ever experienced," said Dr. Lewyn.

Tanner devised a code patch that allowed the gaps to be identified in the flat version of the data and then re-composed to the hierarchical version with only the problem layer gaps flattened and added to the top level (Figure 4). This reduced the size of the layout database, resulting in data transmission time reduction by nearly an order of magnitude.

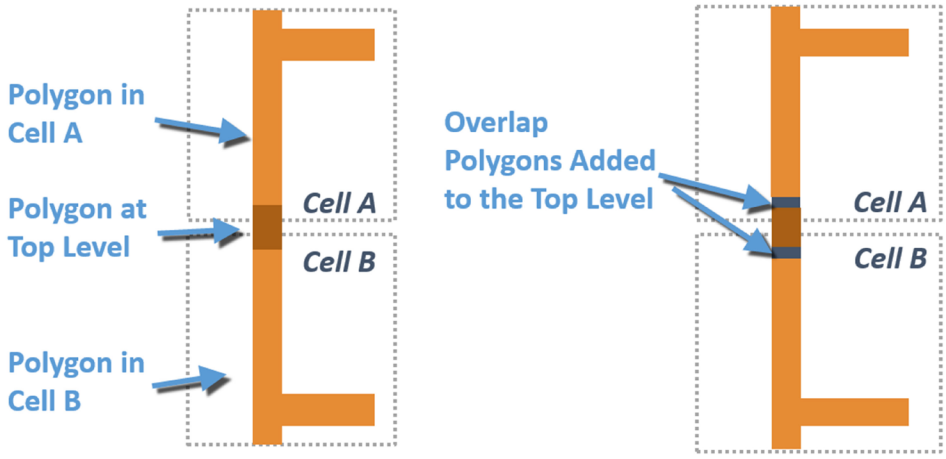

Figure 4: Tanner solution to the hierarchical database generation problem.

PERFORMANCE OF THE PRODUCTION ADC ARRAY

For an ADC targeting astronomical research imaging applications, the test results on the production version of the ADC array were outstanding. In order to preserve image quality at the low (black) end of the dynamic range, it was important to achieve a DL of +/- 0.5 LSB at 16-bits. The ADC DL performance was better than +/- 0.3 LSB over the entire dynamic range (Figure 5a). IL exceeded the +/- 2 LSB requirement by 0.5 LSB, but only beyond the lower ¼ of the brightness scale (Figure 5b). At this signal level, the quantum statistics of the detector electron collection exceed the ADC IL variation, making the extra 0.5 LSB error at ¼ scale insignificant.

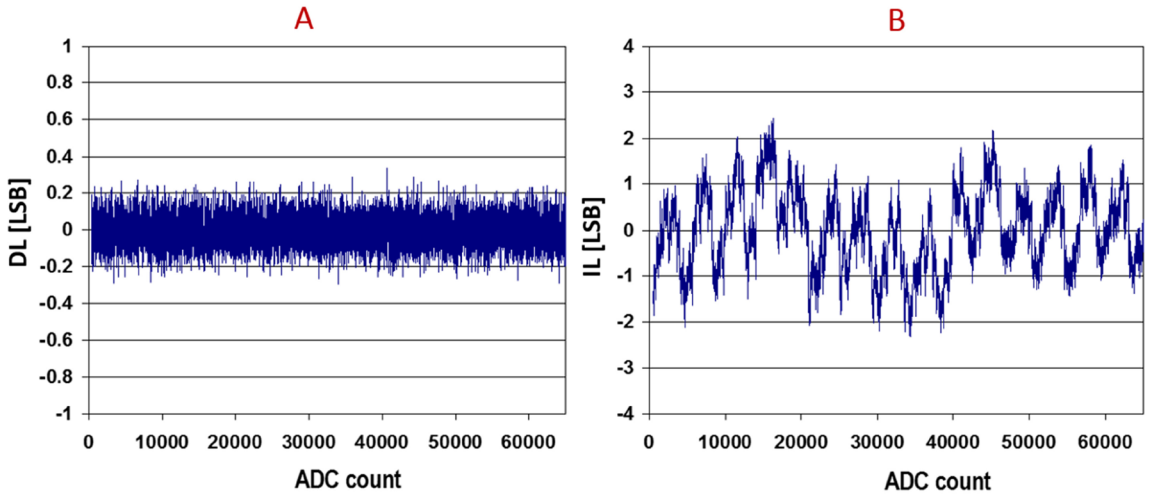

Figure 5A and 5B: Differential linearity (DL) and integral linearity (IL) of the LCI ADC measured at 16-bit "q" intervals.

The ADC was integrated into the RSC SIDECAR IC in an x36 array (yellow boundary in Figure 6). In conjunction with the preamp imager electronics, it performed within the image quality noise specification of 5 rms electrons. When the ADC was used to replace the failed Hubble ACS electronics in May 2009, the result was lower noise and improved image quality. Because the JWST mission constraints do not allow cryogenic re-supply over the 10 year mission lifetime, achieving a 1.5mw per-ADC power level was important. At present, the SIDECAR ADC array and

image processing system has been qualified to NASA Technology Readiness Level 6 (TRL-6) for the 2018 JWST mission.

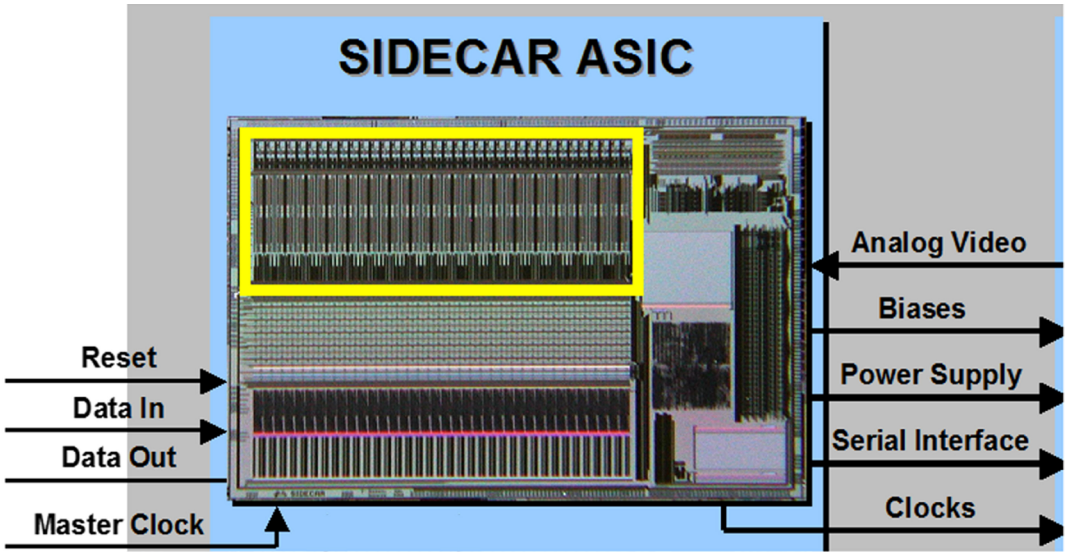

Figure 6: the RSC (now Teledyne) electronic image and signal processing IC including the LCI x36 ADC array (in the yellow boundary).

The SIDECAR ADC array has also been qualified for European Space Agency Euclid mission scheduled to fly in 2020 to map the geometry of the Dark Universe (Figure 7).

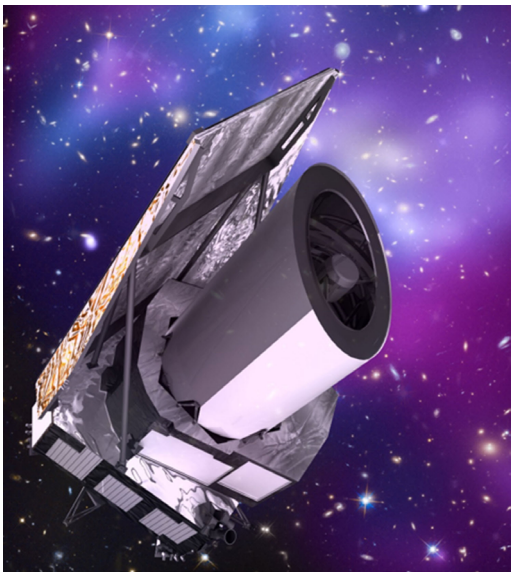

Figure 7: an artist rendition of Euclid exploring the Dark Universe (Source: Euclid-EC.org).

GROUND-BASED ASTRONOMICAL OBSERVATION APPLICATIONS

As a result of the excellent overall performance of the SIDECAR signal processing system, it is currently deployed in conjunction with an array of 2048×2048-pixel HgCdTe HAWAII-2RG detectors in several ground-based telescope applications. It has been integrated into the HiCIAO (Coronagraphic Imager with Adaptive Optics) of the Subaru 8.2m telescope at Mauna Kea, Hawaii. The Subaru belongs to a new class of 8-10m ground-based telescopes that use an array of separate, guidable optical elements to reduce the effects of atmospheric distortion to begin the direct exploration of exoplanets.

The system is also used in the SWIMS (Simultaneous-color Wide-field Infrared Multi-object Spectrograph), one of the first-generation instruments for the TAO (University of Tokyo Atacama Observatory) 6.5-m telescope in Northern Chile, which is scheduled for completion in 2018. This observatory is the highest, permanent astronomical observatory in the world (18,500 ft.). It is being tested with the Subaru Telescope on Mauna Kea prior to the completion of TAO. The detector signal processing chain test results indicate that a noise level of 4 rms electrons has been achieved. When installed in TAO, SWIMS will facilitate detailed red-shift measurements in the extra-galactic universe.

The SIDECAR is being incorporated into other new instruments for ground-based observatories:

- The Carnegie Observatory 'Four Star' wide field imager instrument is under construction for the Magellan Baade 6.5m telescope at the Las Campanas Observatory, Chile. It is intended to provide deep extragalactic survey capability.
- The MOSFIRE (Multi-Object Spectrometer for Infra-Red Exploration) 3rd-generation instrument for the Cassegrain focus of the 10-m Keck 1 telescope at Mauna Kea, Hawaii. MOSFIRE is used to study young stars, galactic center objects, high red-shift galaxies, and star formation in obscured galaxies.
- The Gemini Planet Imager instrument developed by UCLA for the Gemini Southern Observatory 8.1m telescope in Vicuna, Chile. The Gemini Planet Imager Exoplanet Survey (GPIES) is a 3 year study dedicated to imaging young Jupiter-type exoplanets and debris disks around nearby stars. The first Jupiter-sized exoplanet was announced in an article published in ***Science*** on Oct. 2, 2015.

NEXT-GENERATION ADC DESIGN

The combination of 4 different MOS CAP-DAC centroiding and switching algorithms enabled LCI to design a successive approximation register (SAR)-configuration ADC capable of meeting the JWST power and resolution specifications. However, the maximum ADC conversion rate was limited to 5 MSPS. Consequently, the SIDECAR required a second, lower resolution (12-bit) ADC to operate at 20 MSPS for rapid image data collection that consumed higher power with lower image quality.

"We had discussions with developers of very-large diameter ground-based telescopes that revealed a need for an image processing ADC that could operate with very high resolution and low power over a much wider operating range (from low rates up to 50 MSPS)," said Dr. Lewyn.

The next-generation LCI ADC developed for astronomical imaging applications has the following requirements:

- Preserve high resolution (lowering input noise)
- Increase the dynamic range
- Operate at an extremely wide range of sample rates up to 100 MSPS in older technologies and 1 GSPS at 28nm

The ADC employs a new, proprietary pipeline-type architecture to significantly reduce power in comparison to high-resolution, industry-standard SAR or pipeline ADCs constructed in equivalent process technology nodes. High speed performance beyond the usual technology limitations is enhanced by an amplifier topology that achieves wide bandwidth and high gain, even with low DC gain in deep-nanoscale MOS devices.

One design challenge for the new LCI ADC is to port the dimensionless data (Gamma) database to a wide range of technology nodes down to 28nm and obtain layout versus schematic (LVS) results only after porting. If LVS could be performed first in dimensionless Gamma units, edits to correct LVS problems at the technology node scale would only affect the final choice of L-Edit programmable micron-scale resize values. The original, dimensionless database would then require LVS verification only one time.

"To implement LVS in dimensionless Gamma units, we decided to use the Tanner Hi-Per-Verify™ tool which has the ability to use standard Mentor Graphics Calibre® commands for layout parameter extraction," explained Dr. Lewyn.

Two important references were used: the ***Calibre Verification User's Manual*** and the ***Calibre Command Standard Verification Rule Format (SVRF) Manual***. LCI completed the Calibre-compatible LVS-extraction command file by writing approximately 500 lines of code. Tanner provided valuable assistance to LCI by writing the batch file scripts to control the assembly of the resulting circuit, extracted layout, and pre-match files within the L-Edit LVS environment.

The 'PRE-NANOSCALE DESIGN' flow shown in Figure 8 requires minimal feedback from DRC-clean layout to circuit design, as the problems are primarily in the physical design space. In the 'CURRENT 28nm DESIGN FLOW,' LFD-DRC errors and foundry applied CAA+DFM checks can result in circuit design changes affecting parameters, such as circuit bandwidth, that result in re-layout, re-extraction, and re-simulation. Occasionally looking at a layout designer's screen, or check plots does not close the design-layout feedback loop soon enough to prevent substantial verification schedule slips. The resulting verification phase of an analog IC design schedule can now easily be 2 months instead of 2 weeks.

The nanoscale analog CMOS circuit designer is now required, in some large IC-SOC companies, to do the analog physical layout at the 45nm and beyond. The circuit designer needs to be deeply involved in the layout phase by prototyping the layout of critical matching structures or engaging in extensive subcircuit layout pre-planning, and having daily interaction with the physical design team. The goal is to develop blocks that rely on layout constructs that minimize parasitics, achieve pattern regularity, or have substantial similarity to patterns that have previously proven to be 'correct by construction.' The resulting 'DFM CONSTRUCTION-CORRECT' design flow shown in Figure 8 shortens the feedback loops in the design flow and also incorporates the use of tools such as Calibre YieldAnalyzer to perform CAA+DFM checks.

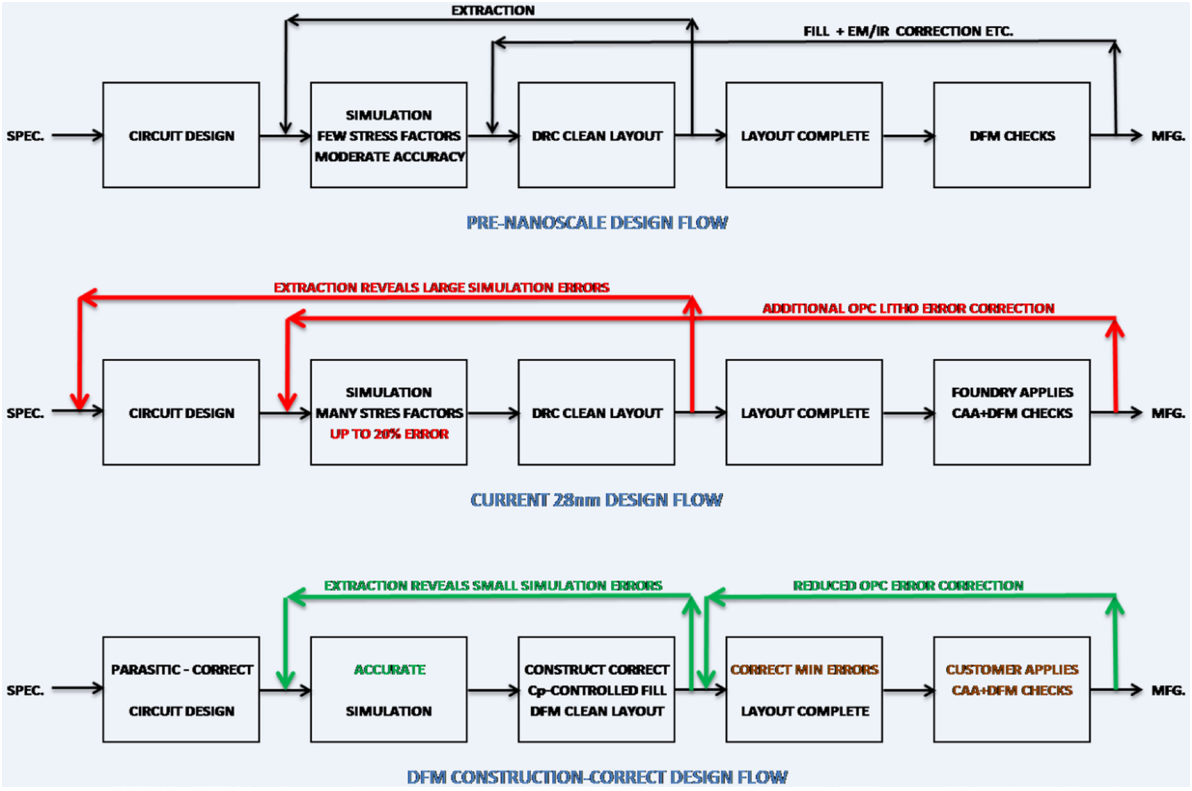

Figure 8: previous, current, and future deep-nanoscale DFM construction-correct design flow.

Dr. Lewyn said, "Using L-Edit for physical design during, not following, the circuit design phase of the project has been invaluable in achieving an extremely hierarchical system design of the new ADC."

Each stage of the ADC is assembled from 7 base cell blocks that are configured using only metal mask options to perform all variants of the functions required from the front-end to the last (LSB) MDAC block. As a result, any parasitic, DRC, or LVS errors corrected in the verification of one of the base structures, will correct the same error in all of the MDAC blocks of the ADC.

POTENTIAL OBSTACLES AHEAD FOR DEEP-NANOSCALE ADC DESIGN

The ability to meet increasingly severe design rule restrictions resulting from the limitations of DUV lithography is an important aspect of migrating dimensionless physical designs from the pre-nanoscale 180nm node (astronomy imaging applications), to the 90nm node (high-resolution video applications), and to the 28nm node (high-speed telecommunication applications). Yield loss from systematic errors are overtaking random error loss in deep nanoscale analog CMOS. Calibre layout verification tools were developed to deal with the issue that DRC-correct is no longer a guarantee of high yields at advanced technology nodes. Developing Gamma design rules to fit the most advanced CMOS line-widths is a challenge.

To address the gradual degradation of DUV lithographic image fidelity with process line-width, several new concepts have been introduced into the design space by several different contributors. These include using relaxed design rules ('RDRs'), separating single layers into 2 or 3 different patterns ('2 or 3 color decomposition'), and standardizing subcircuit patterns ('correct-by-construction'). These concepts push the circuit designer even more in

the direction of becoming heavily involved in the physical design of devices and cells. Physical design-fabric regularity and circuit design width/length choices are no longer independent variables. A row of devices with irregular W dimensions results in Y-dimensional layout pattern non-uniformity.

Even with rapid advances in the power levels of EUV illumination sources and higher production throughputs for EUV lithography, the view of SOC-IC companies with large product volumes is that 2 or 3 color decomposition will be a physical design requirement for some time (Figure 9). Whether EUV is ready for mass production at 7nm or at 5nm is still being debated, but decomposition (multi-patterning) will be with us for some time.

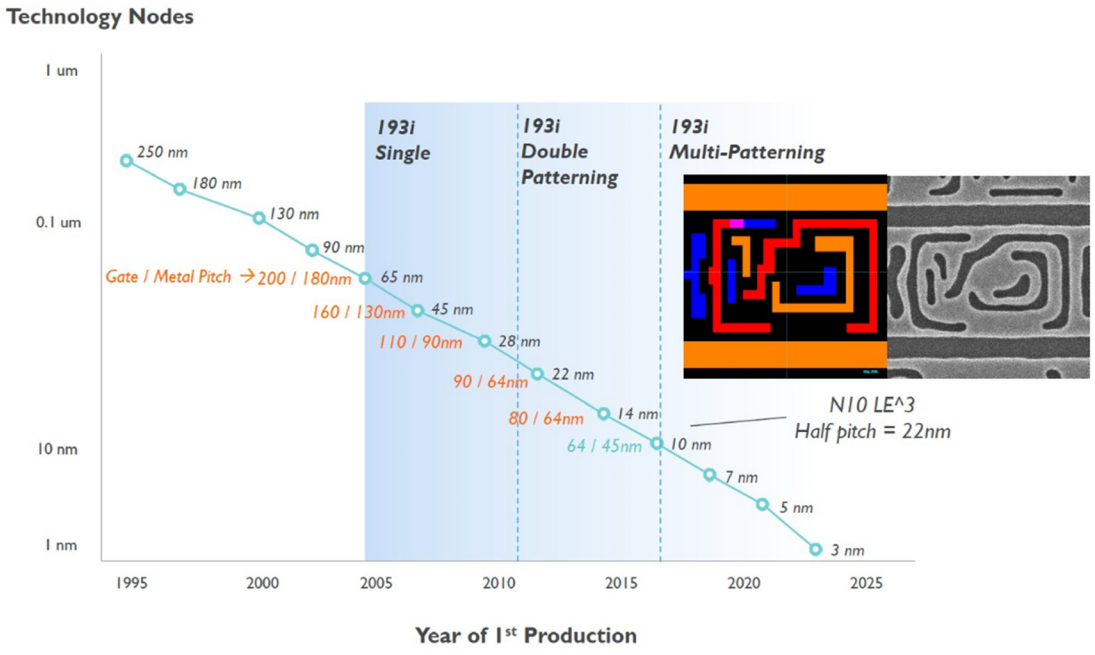

Figure 9: Next-generation multi-patterning (Source: An Steegen, imec).

When a layout pattern is created that cannot be decomposed by CAD tools, it is called an 'odd cycle.' Unfortunately, an odd cycle error causes the design flow to feedback from the end of physical design all the way back to the beginning of the design flow. To correct an odd cycle error, the device or interconnect patterns of the primary cell must be re-designed, extracted, and re-simulated.

Referring to Figure 10:

- In the top pattern, the prohibition restricting two adjacent polygons of the same structure from being adjacent is fixed by the 'stitch' between two different color polygons as they are decomposed on the right.
- The decomposition can also be fixed using a more complex 3 color decomposition.
- However, if the original layout in the bottom structure can only be composed using 2 color decomposition, the odd cycle error (cross-hatched region) cannot be fixed by CAD tools and the layout feedback loop goes back to the start of the design flow.

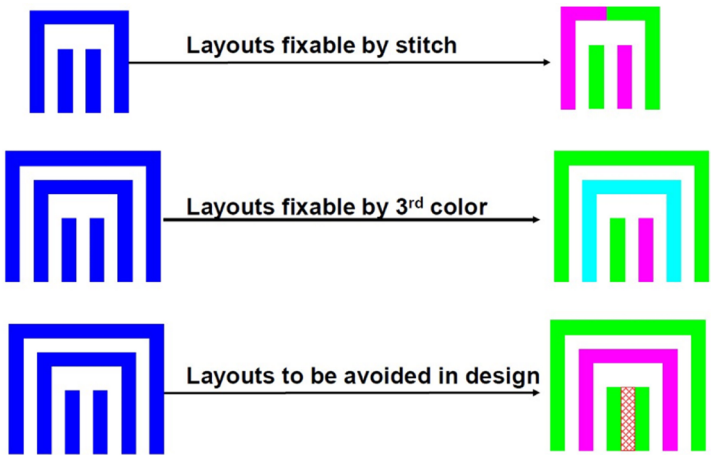

Figure 10: Litho-Etch LE3 decomposition errors (Source: L. Liebmann, IBM).

Layouts decomposed using 2 colors can be easily decomposed into 3 colors, but as Figure 10 shows, the reverse is not true. This can result in a feedback loop from the foundry all the way back to re-layout. Using L-Edit allowed the ADC physical design to easily incorporate 2-color decomposition from the outset. The overall goal was to provide a substantial shortening of time to market and increase yield in the final product.

Dr. Lewyn stated, "The ability to meet the lithography and yield-related physical design challenges of deep nanoscale high-resolution CMOS ADC design is becoming as, or more important, than the circuit design."

CONCLUSION

The original challenge faced by LCI in the development of an ADC for JWST was to come up with a circuit and physical design suitable for a space telescope that had to meet rigorous performance specifications and achieve power low enough to allow 10 year operation without cryogenic re-supply. The challenge was met with a novel SAR architecture and a dimensionless circuit and layout design approach that assured timely completion of the project. Project success has resulted in an ADC that is utilized in the next-generation space telescopes planned by NASA and ESA, as well as in most of the new class of large, ground-based telescopes being used, or under construction, world-wide.

The demands of the next-generation large telescopes and high conversion rate imaging systems require a next-generation ADC design with an order of magnitude power reduction and more than two orders of magnitude speed increase. In addition to those new requirements, there is a need to provide rapid porting over a wide range of technology nodes from 180nm to 28nm. This pushed LCI into the development of a proprietary, pipeline-like ADC architecture and wideband amplifier topology to achieve high gain in deep nanoscale technology. A re-formulation of the LCI Gamma rule set was also required in order to overcome several DUV lithographic challenges. DUV is being pushed by industry demands well beyond the Rayleigh limit where computational lithography enhancements (such as OPC, PSM, and DP) are no longer sufficient for mask making without the use of multi-patterning (decomposition) in physical design.

Dr. Lanny L. Lewyn has a B.S. Eng. (with honor) and an M.S.E.E. degree from California Institute of Technology, Ph.D. E.E. Stanford (CIS), and is a Life Senior Member of the IEEE. His work at Stanford in physical limits of VLSI circuits resulted in publication of the first closed-form solution of the transcendental equation for the MOS device surface potential. It enabled the first construction of a MOS model that was continuous from weak to strong inversion. Another result was the first solution of the dRAM alpha particle soft error problem using the combination of particle range data, separation of bits, and Hamming error-correcting codes.

His high resolution ADC and DAC work relies on litho-friendly-design without autocalibration. This work includes an 18-bit CMOS DAC IC that was licensed to Toshiba for high volume production in early 4x OS audio disc players, a 14-bit CMOS ADC IC first used for DSL in the U.S. and Europe by industry-pioneers PairGain and Alcatel, and the 1.5mw 19-bit CMOS ADC x36-array in an image processing ASIC (SIDECAR) discussed in this paper.

His current circuit design work includes overcoming headroom problems resulting from device voltage limitations in nanometer analog CMOS circuits. That work includes a new algorithm for high speed, high resolution CMOS pipeline ADCs, precision comparators, amplifiers, and low-jitter clock distribution. Physical design work is focused on overcoming stress, lithography, and reliability limitations in deep submicron processes. This work also includes the development and refinement of dimensionless schematic capture and layout techniques to port designs from um to deep-nanoscale technology nodes.

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