HIGH-PERFORMANCE ADC SIMULATION USING ANALOG FASTSPICE FOR THE ATLAS EXPERIMENT AT THE CERN LARGE HADRON COLLIDER

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WHITEPAPER

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INTRODUCTION

The Columbia University experimental particle physics group has a long history of developing custom electronics to read out signals from particle detectors. One current focus is the readout circuitry of the ATLAS experiment's liquid argon calorimeters. ATLAS is one of the experiments operating at the CERN Large Hadron Collider, and the liquid argon calorimeters played a crucial role in the recent Higgs boson discovery. The requirements on the electronics are stringent: The calorimeter signals need to be read out at 40 MHz while maintaining a 16-bit dynamic range with 12-bit precision—all at low power in a difficult radiation environment. The current electronics use analog pipelines and only signals corresponding to events of potential interest are digitized, allowing for a rate reduction from 40 MHz to 100 kHz. However, to improve the selection of signals of potential interest, the electronics will be upgraded and all signals will be digitized at 40 MHz, which requires the design of a custom analog-to-digital converter (ADC), because commercial devices do not offer sufficient radiation tolerance.

CUSTOM ELECTRONICS FOR READOUT CIRCUITRY: PIPELINED ADC

The ADC developed for this application is a dual-channel 12-bit ADC test chip, in which each channel consists of four pipeline stages to resolve the four most significant bits, followed by an 8-bit successive-approximation-register (SAR) ADC. The outputs are serialized over scalable-low-voltage-signaling (SLVS) links. The chip layout of the pipelined ADC is shown in Figure 1.

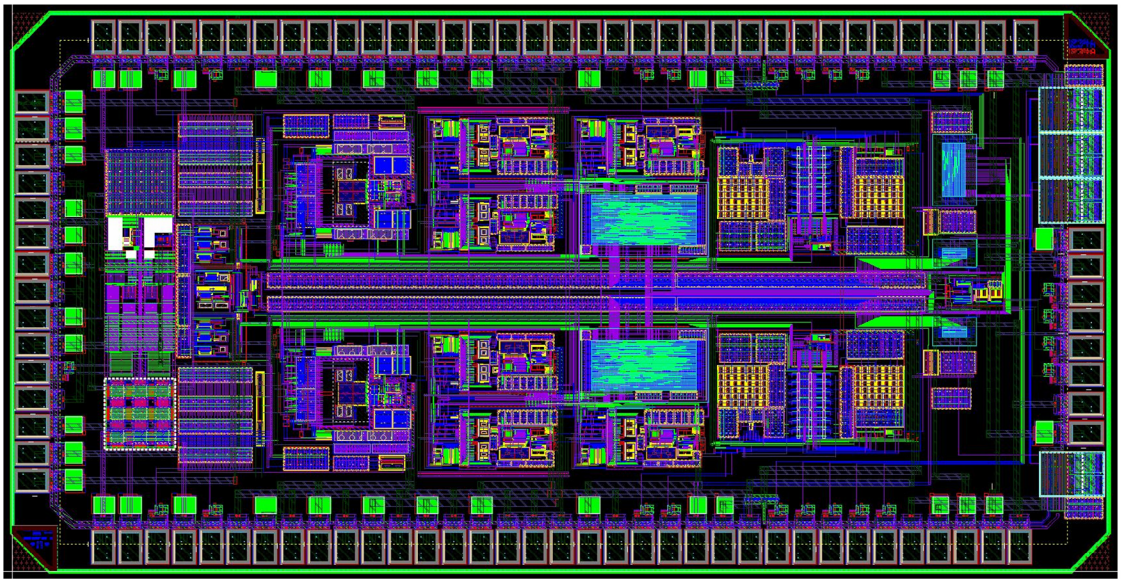


Figure 1: Dual-channel 12-bit ADC layout

The data flow is left to right: the input circuitry and voltage reference are on the left, followed by the pipeline stages, digital data processing unit, SAR, control unit, serializer, and clock distribution. The chip is implemented in 130 nm CMOS technology and it measures 3.7 x 1.9 mm^2.

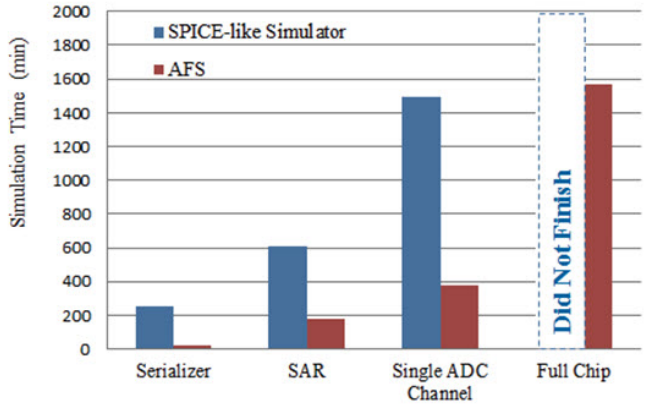
CIRCUIT SIMULATION

Given the time and costs involved in the production of test chips during the development phase, extensive simulation of the chip sub-blocks is required to ensure maximization of each chip's yield, and to obtain relevant information towards the development of the final device. Simulation of ADC circuits is notoriously time-consuming, and an accurate, fast simulator is crucial in limiting the bottleneck of chip simulation in the design cycle. We used the Analog FastSPICE™ (AFS™) Platform from Mentor Graphics to simulate the various sub-blocks and the top-level. We present a performance comparison between a SPICE-like simulator and the AFS Platform.

The results of a comparison between a SPICE-like simulator and the Analog FastSPICE™ (AFS™) Platform from Mentor Graphics® are presented here for different elements. The comparison between the SPICE-like simulator and AFS is performed for the following sub-blocks:

- The digital data serializer with three SLVS drivers for data, clock, and frame signals. This sub-block is mainly digital circuitry, but because it runs at 640 MHz, transistor-level simulation is necessary.
- The 8-bit SAR part of the ADC, where detailed simulation is needed to get an FFT characterization of the circuitry.
- The full 12-bit ADC channel with four pipeline stages and the 8-bit SAR, where again a detailed simulation is needed to get an FFT characterization of the circuitry and to verify the 12-bit precision.
- The full ADC chip functional simulation (using liberal precision) to verify the correct full-chip functionality.

Figure 2 shows the simulation comparison results. For the mainly digital serializer circuit, AFS is almost 20X faster than the SPICE-like simulator. For the SAR and ADC analog circuits, AFS is approximately 4X faster. The full chip simulation with the SPICE-like simulator failed after 67 ns of simulation. Finally, despite the significant speed gains, no difference in simulation accuracy was observed between the two simulators.



Simulation Times		
	SPICE-like Simulator	AFS
Serializer	4h 15m	13m 30s
SAR	10h 7m	2h 59m
Single ADC Channel	1d 0h 52m	6h 14m
Full Chip	Failed	1d 2h 12m

Figure 2: Comparison of required simulation times.

CONCLUSION

The ATLAS Experiment at the CERN Large Hadron Collider required the design of a custom ADC. The use of Mentor's Analog FastSPICE Platform allowed extensive chip simulations during the design phase, and thus led to high confidence of success at the tape-out stage. This was a crucial aspect given the time and costs involved in the production of test chips.

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