PDKs FOR ANALOG/MIXED-SIGNAL (AMS) DESIGN AND VERIFICATION

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WHITEPAPER

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INTRODUCTION

With the pervasiveness of wireless technology and the inevitable shift towards higher levels of integration, integrated circuits today increasingly feature analog/mixed-signal (AMS) elements. The sudden demand for the Internet of Things (IoT) devices creates unique requirements for a full flow, AMS design environment that is affordable and easy to use, but powerful enough to create the widely diverse range of products for deployment for the edge of IoT. More than ever, designers, foundries and EDA vendors are having to get to grips with the 'black magic' of AMS design.

In the purely digital world, design automation tools are challenged to keep pace with the complexity of designing with huge numbers of transistors available on today's process nodes. In stark contrast, analog design is difficult and slow, and as complexity increases, is fast becoming a serious bottleneck in the mixed-signal IC design flow. Although AMS design tools exist, this type of design is far harder to automate. To complicate matters further, AMS design requires detailed knowledge of the target fabrication process.

WHAT IS A PDK?

Here is where Process Design Kits (PDKs) come into the picture. Over the years, a number of misconceptions have built up concerning what PDKs contain, and what they do not; who produces them; how much they cost and what support is needed. Essentially, a PDK is a set of data files used to model transistors for a specific process technology at a specific foundry. Typically, the PDK includes a schematic symbol library, parameterized layout cells (P-cells), Spice models, and technology files related to the design automation flow.

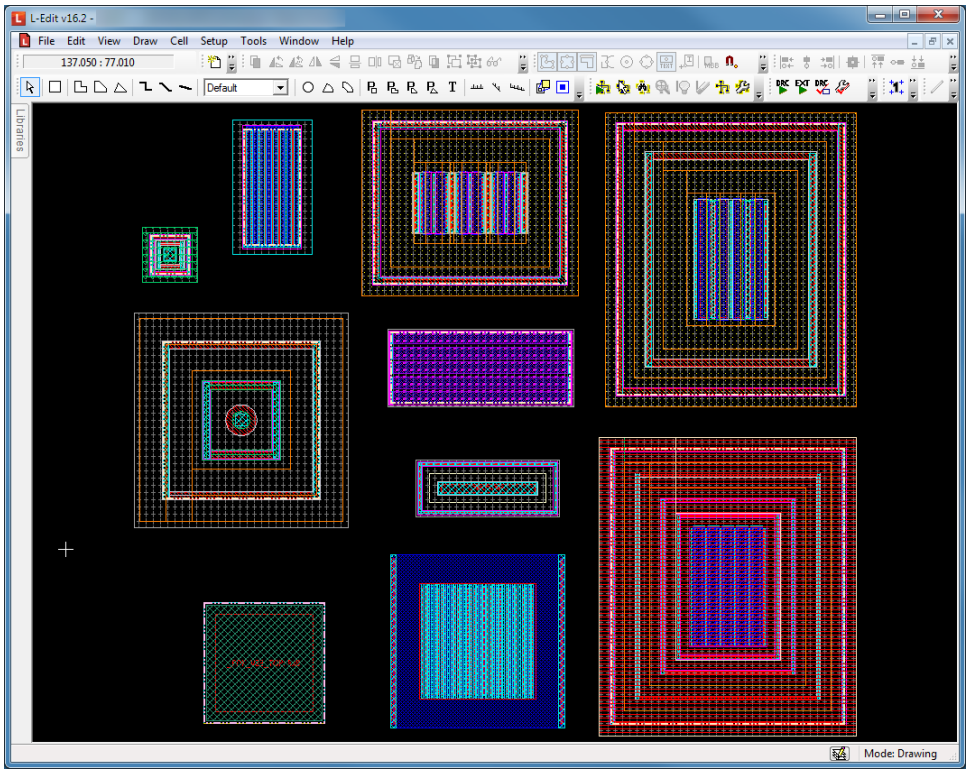

Figure 1: PCells can greatly speed up analog layout, especially for complex devices such as HV DMOS.

A library of parameterized layout cells (P-cells), are used to automate device generation and are an integral part of the PDK. P-cells are not to be confused with digital standard cells. P-cells are the very basic device-level building blocks of analog/ mixed-signal design that embody the process-specific design rules. They reduce the number of DRC (design rule checking) iterations in the design verification process, significantly increasing the likelihood of the final design being correct on the first manufacturing pass. P-cells can also be tailored to suit the LVS (layout vs schematic), ERC (electrical rule checking) and DFM (design for manufacture) features of specific EDA tools.

PDKs are also different than the Reference Flow or Reference Tool Flow (RTF). RTFs are foundry-suggested combinations of design tools that have been proven on a particular process, and may be optimized for speed, area, low power or other parameters. Foundries may highlight specific tools—even specific releases of tools—that have proven interoperability and generate the required result on the target process. Alternatively, RTFs may illustrate a more generic recommendation of the sequence and types of tools that can be used. Increasingly, RTFs are becoming available with reference designs, demonstrating how detailed, and sometimes complex, circuitry has been created and verified using a particular tool flow.

Most EDA vendors offer support for both PDKs and RTFs, and they may even be bundled together. Some tool vendors may integrate these both with their schematic design suites for example, or with a physical verification technology flow. Such instances of bundling PDKs with RTFs and other technology files and even the tools themselves, have led to confusion over what precisely is included in a PDK.

CLEAR BENEFITS

Essentially PDKs are an interface between EDA tools and the semiconductor manufacturing process, describing the electrical, yield and performance aspects of the process. Importantly, PDKs are not only process specific, but also tool flow specific. Generally, they can only be developed as a collaborative effort between foundry and EDA vendor. It is essential that a design manager ensures that the PDK (from a foundry) supports the tools, or the PDK (from an EDA vendor) supports the specific process from the target foundry.

There are clear advantages of working with EDA tools that support the PDKs for the target foundry process. The primary benefit is to reduce overall design time. The design set-up time can be significantly reduced, but principally, PDKs save considerable time and effort at the back-end by ensuring that designs are consistent with specific process rules. PDKs that support advanced routing tools, for example, and interactive automation techniques, such as rule-driven design, can boost productivity tremendously. Globally, PDKs contribute to improved design quality, greater design consistency and ultimately, higher yields.

The investment made by foundries and EDA vendors in creating PDKs is significant. For a foundry with many process options (CMOS, BiCMOS, low or high voltage, low or high power, and each on a different geometry) and with customers using tools from different vendors, the effort involved can be huge. Similarly, for EDA vendors to support or develop a PDK for every process used by every customer can be a daunting task.

INTEROPERABILITY INSPIRES INNOVATION

TSMC, the largest independent foundry, has thrown its weight behind the IPL (Interoperable P-Cell Library) initiative, and has announced interoperable PDKs for its 65nm and smaller processes for analog and mixed-signal design. In principle, TSMC only has to develop one iPDK per process, which is then easily adopted by the many EDA vendors supporting the IPL initiative.

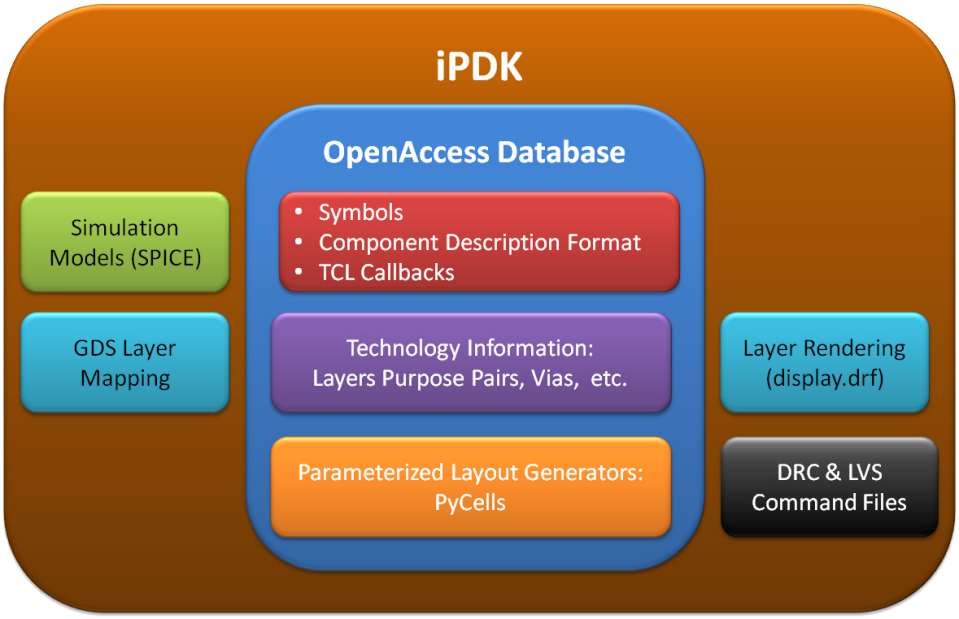

Figure 2: Elements of a PDK.

TSMC's iPDK is said to support a full custom design flow from schematic entry to final layout verification, including technical files for layout creation, pre-layout simulation, layout verification (DRC, LVS, and ERC) and post layout simulation.

Several other foundries have also adopted the iPDK concept such as X-FAB and TowerJazz. iPDKs are based on the OpenAccess common database from Si2 and open source P-Cell development tools (PyCells). The critical factor is that for the first time, P-cell libraries developed for a specific process can be used by IC designers using tools from multiple vendors.

The additional benefits that iPDKs bring to the designer are many. Open P-cell libraries mean that full design re-use will be greatly facilitated. The ability to mix and match 'best of breed' tools from different vendors will be much easier. As a result, it will spur innovative development of new AMS design automation capabilities. New tools could be adopted more swiftly, helping the designer adopt advanced, more automated methodologies and at higher levels of design integration. This will be particularly important as when moving down from 65nm to smaller feature sizes.

PDK SUPPORT PACKAGES

Until such time as iPDKs become the norm, AMS IC designers can continue to gain the advantages of standard PDKs. However, it is always important to check that the chosen EDA vendor provides PDK support for the target process.

From a foundry perspective, major players like TSMC are moving into the AMS arena, but more characteristic of this sector, are smaller, analog specialist foundries. They also provide PDKs and in addition, look to support customers using tools from other suppliers.

Foundries are finding that often, a significant proportion of their analog/ mixed-signal business is coming from users of tool suites from a variety of EDA providers including Tanner EDA by Mentor Graphics. In fact, since supporting Tanner PDKs directly, more than a third of all submissions to Europe-based X-FAB for example, are from customers using the Tanner EDA suite. Tanner tools are also supported by other foundries both directly and indirectly via Mentor Graphics. Furthermore Mentor Graphics provides PDK support for foundries such as TowerJazz, Dongbu HiTek, AMS, TSMC, UMC, SMIC and others, via organizations such as Europractice and Mosis.

Developing a new PDK sometimes is only a matter of days or weeks. Some PDKs may be relatively straight forward to create, especially as Tanner EDA by Mentor Graphics is accustomed to collaborating with most foundries. Much depends on the complexity of the customer's design, the nature of the target process, whether extra library elements and optimization options are included.

The Tanner EDA by Mentor Graphics PDK service is offered to customers under maintenance and typically includes the provision of symbol libraries with callbacks; Spice simulation models; layer, GDSII and rendering definitions; P-Cells; verification set-ups; and parasitic extraction decks. When used with the Tanner EDA IC design tool suite, the PDKs provide customers with a design flow from schematic entry and simulation through schematic-driven layout to full DRC and LVS verification that is tightly matched to the target process.

With the shift to iPDKs, support for different foundry processes will be much faster and simpler to provide. Interoperable P-cells will mean that customers can truly benefit from design re-use, and innovative new tools, delivering a timely boost in design productivity as yet higher silicon integration puts pressure on designers. Tanner EDA's design suite currently supports both OpenAccess and iPDKs.

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