TANNER EDA BY MENTOR GRAPHICS: FULL-FLOW TOOL SUITE FOR BOTH CUSTOM ANALOG AND MIXED-SIGNAL DESIGNS

NICOLAS WILLIAMS, PRODUCT MARKETING MANAGER, MENTOR GRAPHICS
JEFF MILLER, PRODUCT MARKETING MANAGER, MENTOR GRAPHICS

WHITEPAPER

AMS DESIGN AND VERIFICATION

www.mentor.com

INTRODUCTION

Tanner EDA by Mentor Graphics is a suite of products for custom IC, analog/mixed-signal (AMS) and MEMS design. The sudden demand for Internet of Things (IoT) creates unique requirements for a full flow, mixed-signal design environment that is affordable and easy to use, but powerful enough to create the widely diverse range of products needed for deployment of IoT. While a number of EDA tool providers offer software for AMS designs, such tools either come at high cost (low price-performance ratio) or are custom made point solutions requiring unwieldy amounts of data manipulation and manual integration. The Tanner EDA AMS IC design flow is uniquely positioned. It offers a cohesive, integrated mixed-signal design suite that is ideally suited to IoT and project-based design with its extremely short cycle times and sensitivity to cost.

FRONT-END DESIGN

Design challenges associated with AMS ICs are as diverse the number applications and market segments served by these devices: power management, displays, image sensors, photovoltaics, life sciences, automotive, aerospace and consumer electronics. But it is the IoT that will have greatest impact going forward on AMS design.

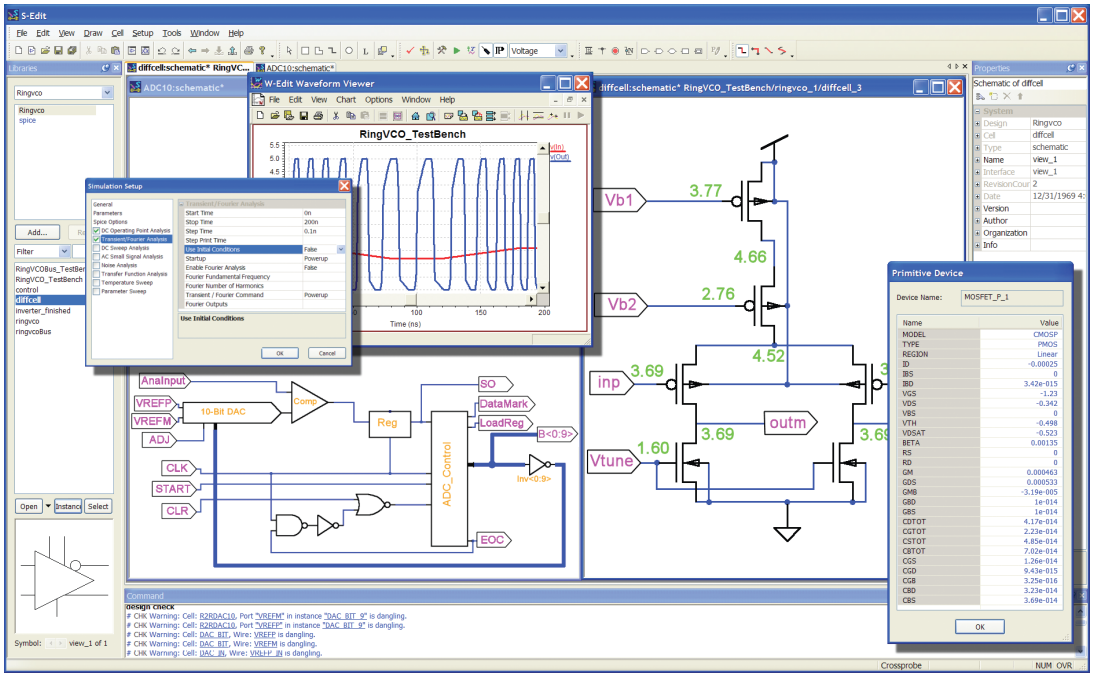

Figure 1: Tanner S-Edit Schematic capture design and simulation cockpit, showing schematics, simulation waveforms, model parameters, and simulation settings.

When creating an analog/mixed-signal design, designers need to be able to work in both domains to explore tradeoffs. The faster a designer reaches an optimal solution, the more time can be spent on tough corner cases. In particular, Tanner T-Spice AMS supports Verilog-AMS modeling, enabling top-down design of complex mixed-signal ICs using high level equation-based modeling for analog blocks mixed with behavioral Verilog digital blocks. Designers can quickly explore mixed-signal architectures, then use the abstract Verilog-AMS models as an executable specification during detailed design of the individual blocks.

Tanner S-Edit schematic capture is a front-end design tool with an easy-to-use design environment for creating the multiple-view-per-cell needed in analog/mixed-signal design. S-Edit's support for drawn schematic views, as well as SPICE, Verilog, Verilog-A and Verilog-AMS views, allows designers to easily swap in abstract or detailed models on a cell-by-cell basis. S-Edit imports schematics via Open Access or via EDIF from Cadence, Pyxis, Laker, ORCAD and ViewDraw with automatic conversion of schematics and properties for seamless integration of legacy data. Using S-Edit's schematic design checks, designers can quickly uncover common errors such as undriven nets, unconnected pins and nets driven by multiple outputs. Catching errors early before running simulations boosts efficiency and speed, particularly essential in AMS design.

Next comes simulating the design with a high degree of accuracy. This is no small task in a mixed-signal design, given the increasing size and complexity of circuits, and the challenge of supporting various transistor and behavioral models. Tanner T-Spice Simulation meets these challenges with broad standards support, market-proven reliability, and high performance and scalability. T-Spice offers HSPICE and PSpice compatible syntax and supports the latest industry models, including PSP, BSIM3.3, BSIM4.6, BSIM SOI 4.0, EKV 2.6, MOS 9, PSP, RPI a-Si & Poly-Si TFT, VBIC, and MEXTRAM models to allow easy simulation of both modern and legacy designs with the full range of foundry models. T-Spice lets designers precisely characterize circuit behavior using virtual data measurements, Monte Carlo analysis, and parameter sweeping. It also supports Verilog-A for analog behavioral modeling, allowing designers to prove system level designs before doing full device level design.

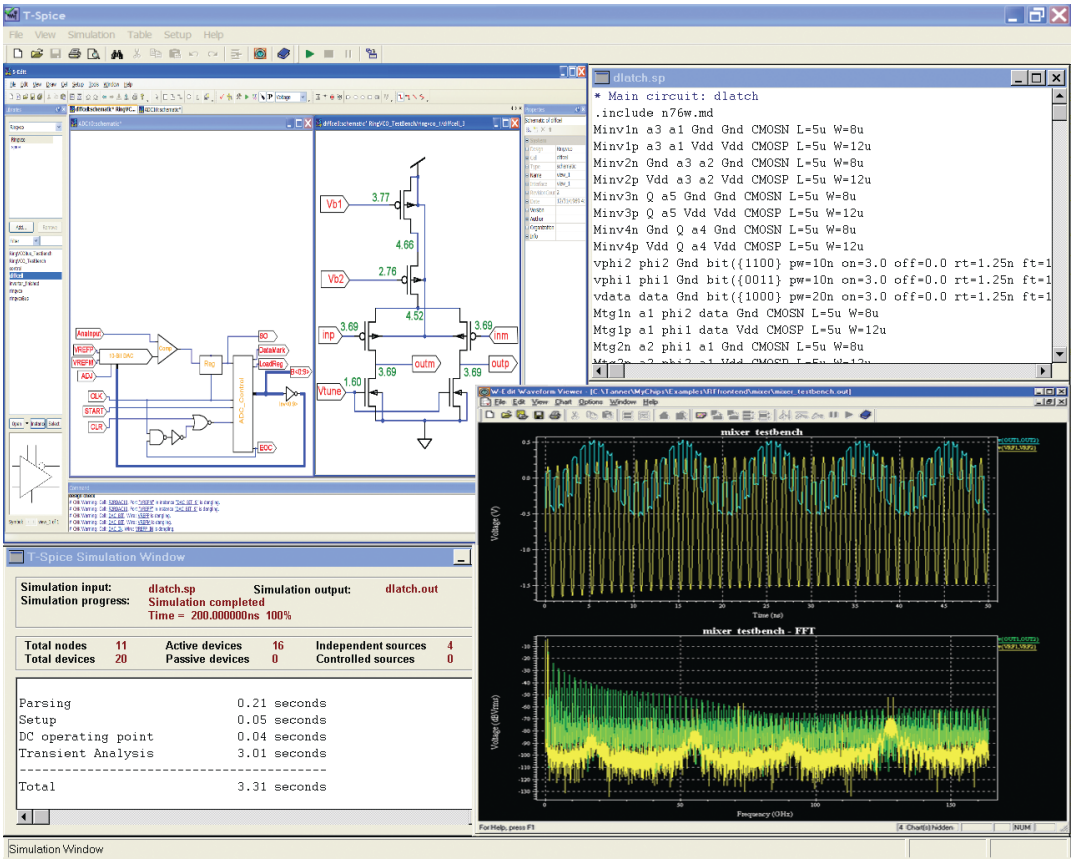

Figure 2: Tanner T-Spice Simulator UI, with schematic, spice netlist, simulation logs and waveform data.

T-Spice is also capable of high performance mixed-signal simulations by leveraging the capabilities of the Mentor Graphics ModelSim digital simulator. Designers can load netlists with combinations of Verilog, Verilog-A, Verilog-AMS and transistor-level SPICE. T-Spice automatically partitions the netlist and initiates an AMS co-simulation, sending any digital blocks to ModelSim while handling any SPICE or Verilog-A portions of the design. T-Spice and ModelSim then co-simulates and communicates with each other whenever a signal change happens across an analog/digital boundary.

FULL PHYSICAL LAYOUT CAPABILITIES

Once the front-end design and verification work is done, physical layout is next. Designers must again balance competing priorities—especially for the analog portion of the design. Here again, Tanner provides an optimal mix of powerful capabilities that are easy to learn and use, all on a PC platform. The Tanner L-Edit IC Layout tool is a complete hierarchical physical layout editor, combining fast rendering and built-in productivity tools to let designers maximize efficiency when creating the layout for their designs. The tool's optimized editing allows for editing layout with fewer mouse clicks than any other layout editor. Built-in productivity features include object snapping, alignment tools, automatic guard ring generation, complex Boolean operations on objects with polygons of arbitrary shape and curvature, and cross-probing between schematic and layout.

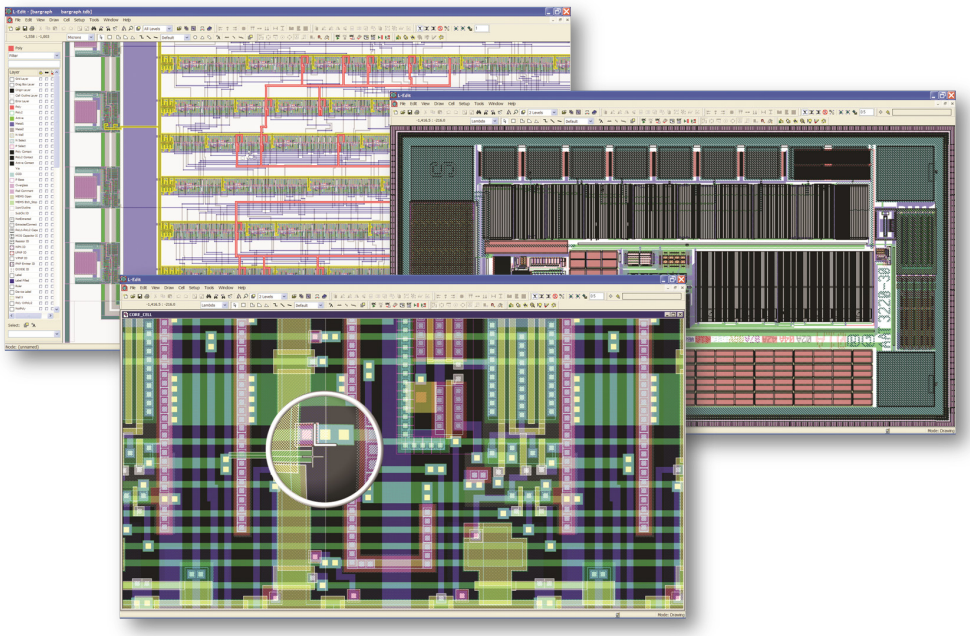

Figure 3: Tanner L-Edit IC Layout tool displaying layout data for three designs.

L-Edit supports parameterized cells, allowing designers to create automatic custom layout generators or use DevGen to easily setup layout generators for most common devices such as MOSFETs, resistors, or capacitors. The tool's interactive design rule checking (DRC) displays violations in real time while layout is edited, helping designers create compact, error-free layouts the first time. Moreover, L-Edit's node highlighting capability allows for highlighting all geometry connected to a node in order to quickly find and fix LVS problems such as shorts and opens.

L-Edit increases physical design productivity by supporting multiple users working on the same layout. And designers can use foundry-provided files directly, eliminating the need for manual set up. All of this reduces the CAD support burden during physical design tools, enabling designers to focus on the design.

Layout teams can maximize their productivity and consistency with a full schematic driven layout flow. S-Edit and L-Edit communicate and stay in sync, including cross probing and automatic ECO flagging. Automatic instancing of primitives, subcells, and parameterized cells save time and prevent errors, while real-time flylines and assisted manual routing help get designs placed and routed quickly and optimally.

PHYSICAL VERIFICATION

Tanner Verify DRC and LVS tools offer a comprehensive, yet affordable physical verification solution. The tools performs analog/mixed-signal IC design rule checking (DRC) and netlist extraction. The hierarchical rule checking engine finds violations in the cell where they occur, enabling a designer to correct a violation once, rather than sorting through many duplicate violations. And the tool is integrated with Tanner L-Edit IC Layout, allowing for precise location of errors, quick turnaround of corrections, and faster debugging.

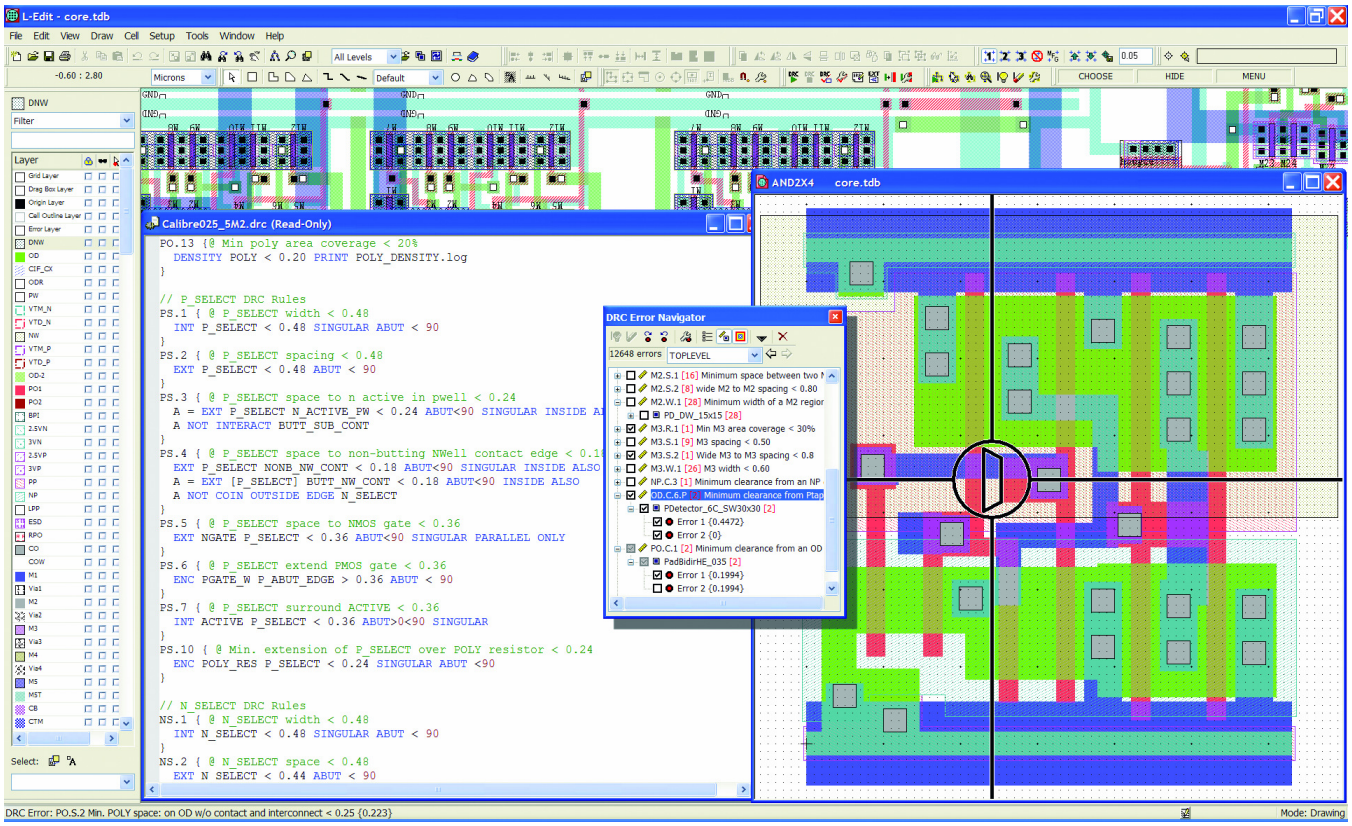

Figure 4: Tanner L-Edit IC Layout displaying the design rule deck in a syntax highlighting editor, the results of a DRC run, and an error marker for a specific rule violation.

MODELING LAYOUT EFFECTS

Interconnect parasitics become a big challenge at smaller process nodes (and associated higher frequency, lower voltage circuits). As process size becomes smaller, interconnect thickness increases to offset the increase in resistance due to the interconnect width getting smaller. This makes the effects of lateral coupling capacitance much more significant than vertical coupling capacitance. Lateral coupling can lead to different timing behavior and including it in simulations is required to accurately calculate delay and circuit behavior.

Tanner Parasitic Extraction is a high performance parasitic extraction tool that is offered as an optional add-in. The tool is integrated with Tanner L-Edit IC Layout for easy and rapid extraction of parasitics. It quickly extracts simulation-ready SPICE netlists from layout, including devices (MOSFETs, bipolars, etc) and interconnect parasitics. Tanner Parasitic Extraction also extracts accurate, complete parasitic networks for each node, including vertical and lateral coupling capacitance and interconnect resistance. And the tool can simplify the parasitic RC network without reducing simulation accuracy up to a user-specified frequency with the built-in netlist reduction algorithm.

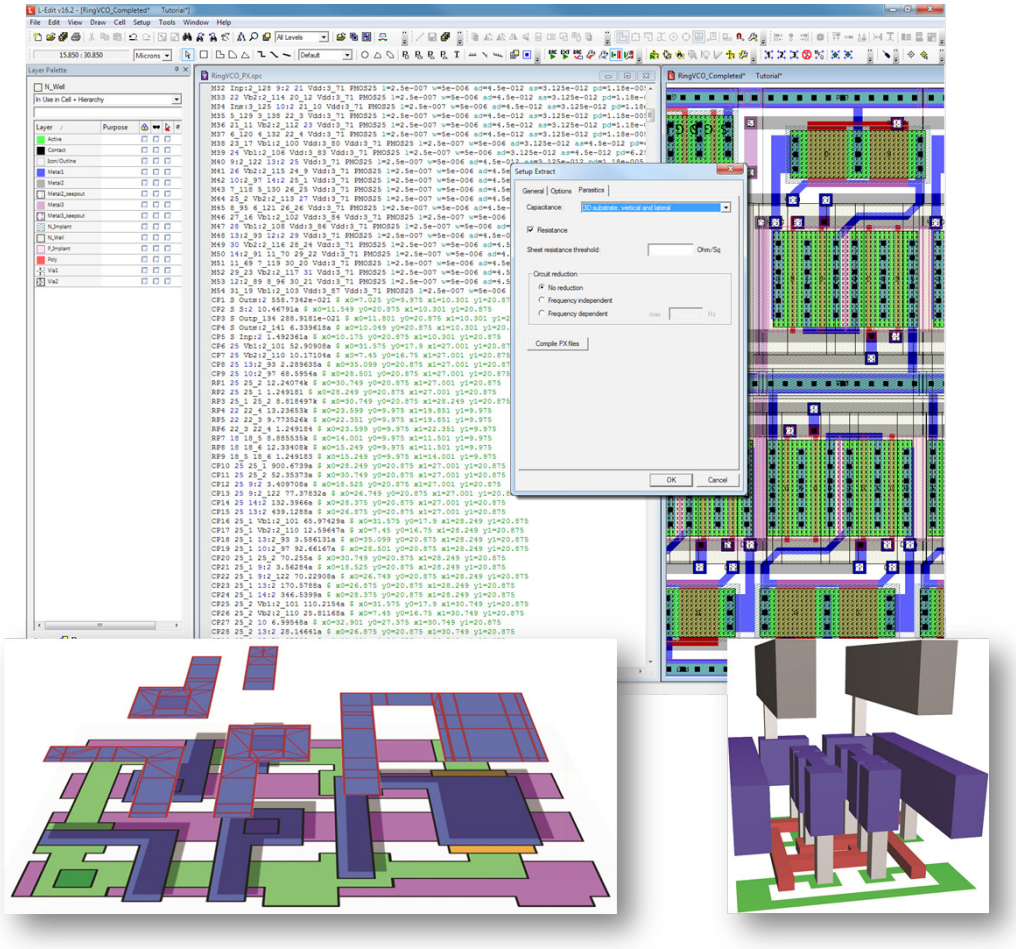

Figure 5: Simulating a ring oscillator with back-annotated interconnect parasitic modeling.

STREAMLINED DIGITAL PHYSICAL DESIGN

Analog designers face number of challenges when creating a mostly analog circuit that also includes some digital—the so-called 'Big A/little D' designs. At the conceptual level, analog design teams initially struggle with the overall top-down design for mixed-signal devices. Then throughout the design process, they are challenged in multiple areas. For example, in designers can have trouble catching edge cases or problems in digital circuits with internal states or hidden states in digital logic. And designers often struggle with full-chip timing analysis, finding it difficult to complete full timing analysis if there is a sizeable digital section. Lastly, when it comes to physical verification, there can be problems with the digital logic generating too much noise for analog circuitry sharing the same substrate.

The Tanner suite is specifically crafted to address and resolve these challenges. Analog designers who use mixed-signal tools greatly benefit from the increased automation, improved accuracy, lower NRE costs, and reduced time to market. That is why Tanner's solutions incorporate a complete RTL to GDS flow specifically tailored for the big-A/little-D AMS market. It is a complete logic synthesis tool with integrated capability to synthesize and optimize for area, power, timing, and design-for-testability (DFT). Tanner Place and Route is highly integrated with L-Edit giving you full control over every step of the place and route process. TimeCraft is a high-speed, big-capacity, static timing analyzer (STA) for nanometer timing analysis and sign-off. (And note that dynamic timinig analysis using post-layout routing information is available via ModelSim.)

FULL CHIP ASSEMBLY

Any comprehensive analog/mixed-signal flow also will include full-chip assembly, the process of placing the major functional blocks into the padframe and routing the top level signals and buses.

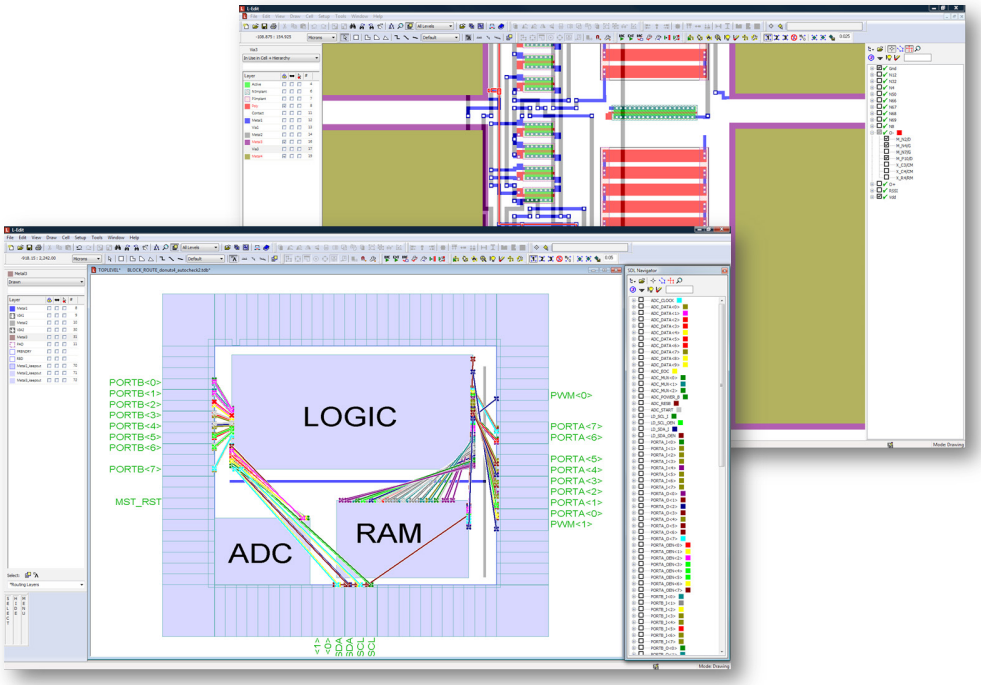

Figure 6: Schematic driven layout in Tanner L-Edit IC Layout shows real-time flylines and supports manual, manulally-assisted, and fully automated routing modes.

Tanner's full-chip assembly solutions are driven through the SDL interface in S-Edit and L-Edit. Top-level blocks are instanced, and designers place blocks using SDL's real-time flylines to minimize routing congestion. Designers also can very quickly check for connectivity issues using SDL's Short and Open Checker, which can run in the cell's context and highlight errors without having to run a full LVS.

SDL Router is an automatic routing engine integrated with SDL that speeds layout of analog cells and top-level chip assembly routing. The tool allows the designer to focus on routes that require hand craftsmanship—either for performance or addressing analog-sensitive nets or parts of nets. For all remaining circuitry, the SDL Router automatically routes the non-critical nets, routing different nets with different user specific widths with support for multiple vias used for layer transitions. It also allows designers to mark existing geometry as part of a specific net allowing selection, highlighting, and rip-up of geometry by net to capture the designer's intent.

CONCLUSION

In March 2015 Tanner's business assets were acquired by Mentor Graphics, which is helping leverage its extensive technology leadership and global footprint for the benefit of designers working on mixed-signal projects, from ICs to MEMS to IoT devices. These designers face a slew of challenges, most related to the fact that ICs continue to add increasing functionality and capability, and grow in complexity. At the same time, business pressures are requiring designers to shorten time to market and reduce re-spins. The Tanner suite has been built from the ground up with the needs of the designer in mind. While a number of EDA tool providers offer software for creating AMS designs, they either come at high cost (low price-performance ratio) or are custom made flows of point tools, requiring much data manipulation and manual integration. The Tanner suite can offer AMS designers a cohesive and comprehensive tool suite that delivers productivity, usability and price-performance that is unmatched in the industry.

For the latest product information, call us or visit: www.mentor.com

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

MGC 7-15 TECH13110-w