ANALOG FASTSPICE PLATFORM CMOS IMAGE SENSOR VERIFICATION

APPLICATION BRIEF

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CMOS image sensors (CIS) are widely used for imaging in smart phones, tablets, cameras, industrial, medical, and automotive applications. High-level CIS architectures are array-based, similar to memory architectures. The CIS block diagram in Figure 1 shows the pixel array, the column readout and analog-to-digital converter (ADC) circuitry. The image sensor captures an image with an array of identical pixels, reads the contents of the array, and converts the analog voltages to a digital code for each pixel [1].

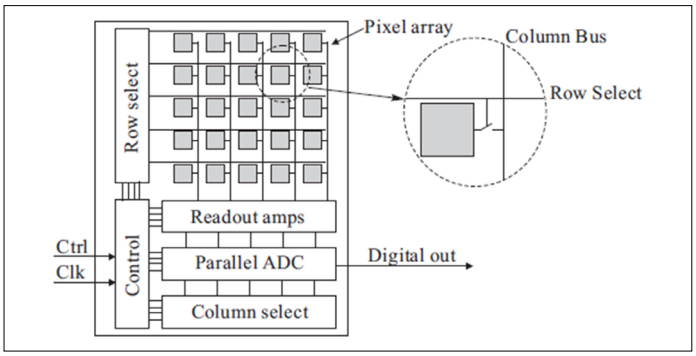

Figure 1. CIS with On-Chip ADC and Control Circuitry

SIGNAL PROCESSING

The image array is made of active pixels that include a photodiode. The photodiode gathers photons and converts them to electrons that control the pixel circuitry to produce an analog voltage signal. Most image sensors use a column-parallel approach to read the analog voltage signal from the pixel array. The analog signal is amplified, and then an ADC converts it to a digital code. Typical CIS ADC architectures include flash converters, sigma-delta converters, successive approximation, single-slope ADC, and pipelined ADC [2]. Figure 2 illustrates the single-slope ADC, column-parallel readout approach.

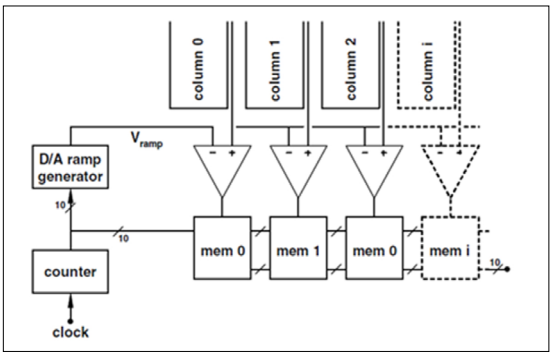

Figure 2. CIS Column-Parallel Readout

CIS PERFORMANCE CRITERIA

Mobile applications require CIS devices that have a low signal-to-noise ratio (SNR), low power, small area, high resolution, high dynamic range, and high frame rate. CIS imaging performance is noise limited. Thus optimal CIS design requires accurate noise analysis on the pixel array electronics and column readout circuitry.

Image sensor noise sources can be categorized as spatial and temporal noise sources. Spatial noise sources include dark fixed pattern, light fixed pattern, column fixed pattern, row fixed pattern, defect pixels, dead and sick pixels, scratches, and so on. In the case of a dark fixed pattern, the dark current becomes very small in deep nanometer processes, and its effect is typically not noticeable during normal pixel operation.

Temporal noise is random in nature and fundamentally limits image sensor performance. Temporal noise includes kT/C noise, flicker noise (1/f), dark current shot noise, photon shot noise, power supply noise, phase noise, ADC quantization noise, and so on. Temporal noise dominates the pixel random noise floor and is the main source of noise in the readout circuitry.

Another type of temporal noise source is random telegraph signal (RTS) noise, which introduces "blinking pixels" from which the output exhibits three discrete levels. However, RTS noise does not appear to be a limiting factor on the performance of today's image sensors.

CIS VERIFICATION REQUIREMENTS

Accurate noise analysis and characterization, including the effects of random device noise (thermal and flicker), is necessary to ensure that the CIS design meets its specifications. Noise analysis is further complicated because of the following factors:

- Nonlinearity in the charge-to-voltage conversion in the pixel circuitry
- Time-varying nature of the circuit and 1/f noise
- Thermal and flicker noise for pixel and column circuitry

Intensive block-level circuit characterization is required to ensure functionality across operating conditions, environmental conditions, and process variations. Designers should include post-layout parasitics and characterize the circuit for global process variation and device mismatch—ideally using statistical techniques with sufficiently high confidence levels. Of particular interest is pixel array column-to-column variation. Pixel verification techniques are unique to each CIS supplier since they depend on special, foundry-specific photodiode and follower transistor devices and models.

In addition to block-level characterization, design teams must verify the CIS top-level performance and functionality to ensure that noise, performance, and power specs will be met in silicon. Given a pixel array's large size, design teams typically approximate top-level performance simulation using a pixel array that has a subset of the rows, columns, and associated control and readout circuitry. They simulate such circuits through multiple frames of image sensing operation.

CIS VERIFICATION WITH THE AFS PLATFORM

Because device noise is a key limiter in CIS performance, Analog FastSPICE™ Transient Noise analysis (AFS TN) is ideal for transistor-level verification of CIS blocks. AFS TN is the industry's only full-spectrum device noise analysis for non-periodic circuits like ADCs, enabling it to uniquely deliver silicon accurate results. It is also parallelizable for maximum simulation throughput.

With AFS TN, designers can verify the impact of random device noise on the readout circuitry, including ADCs and comparators, with nanometer SPICE accuracy. In addition, designers can include post-layout parasitics and characterize the circuit for process variation and device mismatch.

For comparators, AFS TN quantifies absolute jitter in the trigger point with nanometer SPICE accuracy. This accuracy is important, because the comparator is a sharp transition circuit where a small amount of noise can cause large waveform perturbations. Figure 3 illustrates comparator jitter analysis, showing the five-period eye diagram time window and the detail of the output jitter histogram. Jitter needs to be minimized, resulting in a clean edge when Vin equals Vramp, in this case 1.5V. Parallelizing the AFS TN run in this case speeds up the simulation an additional 6x versus a sequential run.

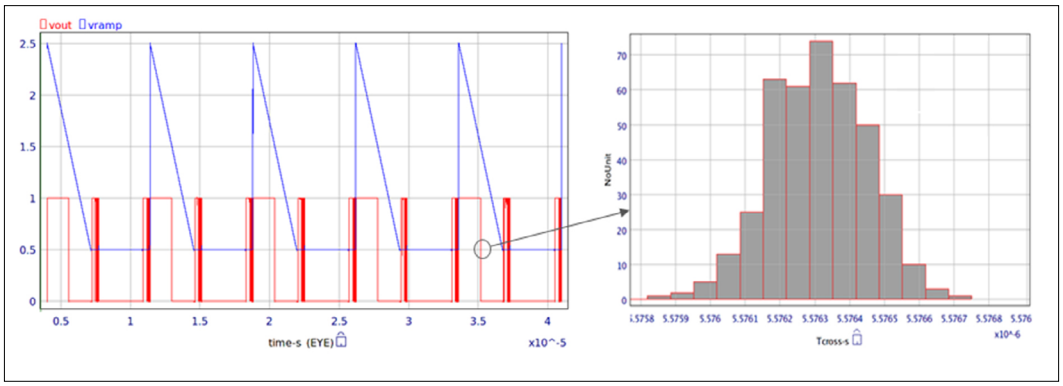

Figure 3. Comparator Output (Eye Diagram Window = 5 periods) and Jitter Histogram

For ADCs, AFS TN full-circuit verification includes the impact of random device noise and circuit noise, such as quantization noise. Designers can also include post-layout parasitics and characterize the circuit for process variation and device mismatch. Figure 4 shows the transient analysis power spectral density (PSD), the transient noise analysis PSD, and the actual silicon measurement demonstrating AFS TN's accuracy [3].

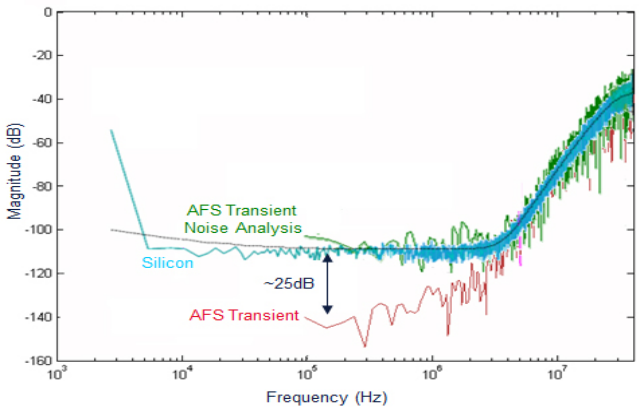

Figure 4. ADC Power Spectral Density Plot

For full-circuit, functional verification of CIS devices, the AFS platform has the performance and capacity to handle multiframe verification of a representative subset of the full array and readout circuitry with nanometer SPICE accuracy. AFS features unique capabilities to handle pre-layout and post-layout, large-scale arrays robustly, accurately, and quickly, while providing silicon-accurate time, voltage, frequency, and power resolution, and it does so faster than legacy, digital FastSPICE tools that trade off accuracy for performance.

REFERENCES

[1] Leif Lindgren, "Topics on CMOS Image Sensors," Linköping Studies in Science and Technology, ISBN 91-85299-91-X, ISSN 0280-7971, July 2005.

[2] Albert J.P. Theuwissen, "CMOS image sensors: State-of-the-art," Solid-State Electronics 52 (2008) 1401–1406.

[3] "ADC Performance Signoff with Analog FastSPICE™ Transient Noise at Qualcomm," Mentor Graphics White Paper, 2009, www.mentor.com/products/ic_nanometer_design.

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