COLLABORATIVE IC DESIGN MANDATES INTEGRATED DATA MANAGEMENT

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Over the last decade, design teams have encountered increased competition due to globalization (requiring the best available engineers irrespective of location), an exponential increase in design complexity, and shrinking market windows. This results in teams of engineers with different skill sets (for example analog, digital, MEMS, and RF), spread across multiple sites, managing complex flows, and sharing a large volume of constantly changing data. Unstructured design files with multiple copies and versions, along with associated verification results, cannot remain unmanaged if a design team wants to avoid mistakes and tape out successfully while meeting schedules.

In order to be efficient and to avoid mistakes, design teams need quick answers when something is wrong in the design or verification cycle of a project. Some of the questions they need to answer are:

- Why is simulation failing today when it was perfect yesterday?
- Do we have all the correct versions of the files for system simulation?
- Do we have knowledge of all the design changes made this week before we build a design for testing today?
- Are we all working from the very latest version of the requirements?
- What happened to all the design work that the testbench team completed last week?

Efficient collaboration is becoming an essential ingredient to meeting tight IC design schedules. In analog and mixed-signal (AMS) design, collaboration has many facets. Design tools are usually specific to roles and handoffs are numerous, especially when moving a design to a foundry. This often poses a challenge for companies hoping to keep design teams synchronized while ensuring that time-to-market windows are met.

It is a common perception that design data management tools are only for big teams working on large digital projects that employ a range of IP blocks. Here, team roles are assigned to designers using familiar EDA tools and expertise is distributed across people at multiple sites. Benefits of design management tools are well established for these situations where complexity is a given and collaboration is a must. The proposition becomes even more compelling when face-to-face interaction between team members is infrequent.

Analog and RF designs are different than traditional digital flows. Expertise is often concentrated within a small group of people. Sharing within these teams often takes the form of handoffs. For example, a designer finishes a schematic and hands it off to a physical layout designer. Unfortunately, in global environment, it is very rare that a design flow actually works with a simple handoff between team members. There are several other factors to consider, such as communication with a third-party foundry, accounting for mixed-signal designs that integrate with digital IP blocks, and addressing feedback from the test team. This means that team members are likely share more data than expected and a design can be handed back upstream at any time in the development cycle. Without a design data management solution, when a problem is found, the downstream team essentially stops, hands the entire design back to an upstream designer to investigate, and they wait for the revised design before proceeding. Employing a data management tool is also important for small design teams because:

- Teams can roll back the design if changed file(s) cause issues.
- Team members can lock blocks of the design to avoid overwrites.
- Designers can see and analyze differences between files.
- The team has a complete record of the lifecycle and changes of the design.
- It is easy to tape out the design with all the correct files.

Recognizing the critical value of data management, Tanner EDA teamed with ClioSoft® to interface their SOS data management solution with the Tanner custom IC design flow, to ensure that all IC team members collaborate within a managed design data environment.

UNDERSTANDING THE VALUE OF CLIOSOFT'S SOS7

The SOS7™ platform from ClioSoft enables local or multi-site design and verification teams to efficiently collaborate on any IC design project, from concept to tape out. Specifically designed for hardware design teams, it enables them to streamline their development cycle and manage design handoffs and changes throughout the flow. SOS7 covers three key aspects of SoC design data management (Figure 2).

Figure 2: The key aspects of design data management.

SOS7 was built from the ground up for performance, security, network storage optimization, and customizability in order to meet the demanding requirements of modern IC design environments. Figure 3 provides an overview of the platform's capabilities that support the key concepts from Figure 2.

Figure 3: An overview of the SOS platform.

Interfacing to SOS7 within the Tanner IC design and verification flow allows teams to focus on getting the IC completed on time, instead of worrying about if everyone is operating with the correct data. Figure 4 presents some of benefits of employing the SOS platform within the Tanner flow.

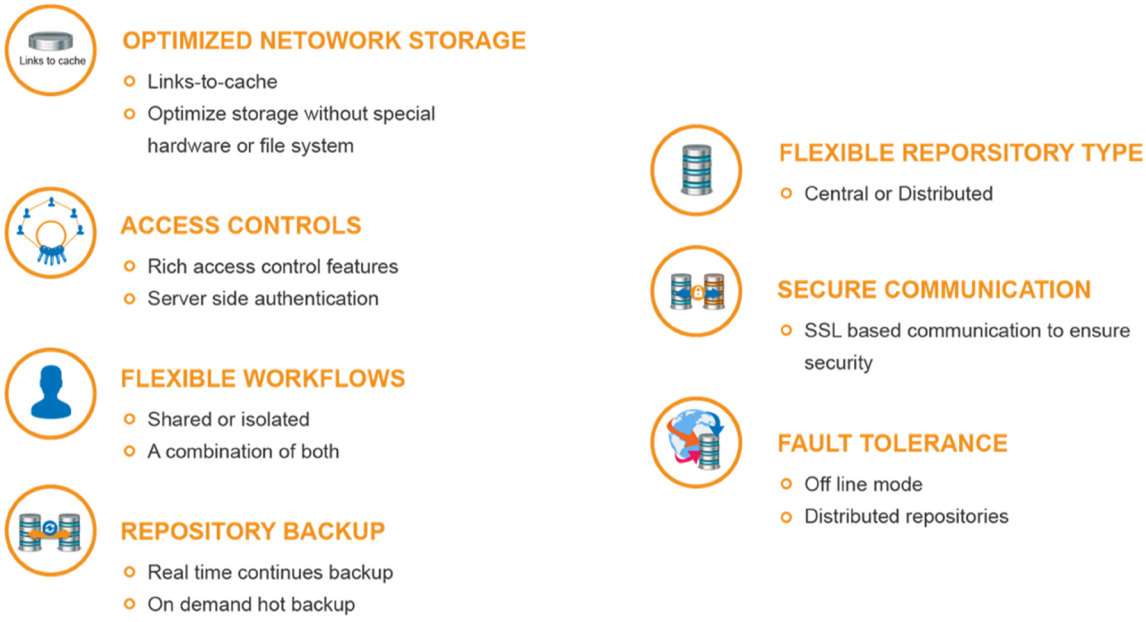

Figure 4: Benefits of using the SOS platform.

UNDERSTANDING DATA MANAGEMENT WITHIN THE TANNER FLOW

Tanner provides an integrated, top-down flow (Figure 5) for analog/mixed-signal design and verification.

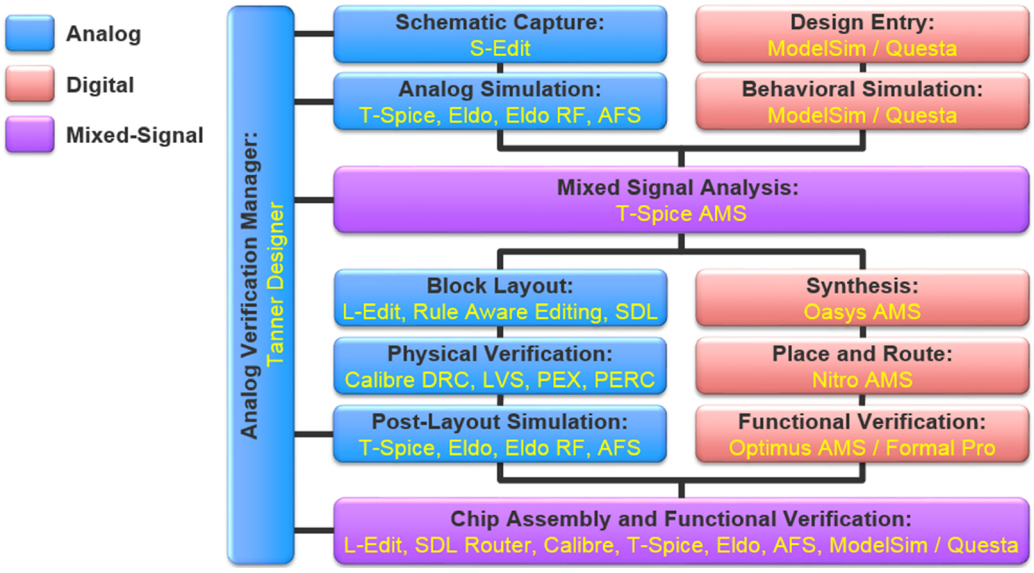

Figure 5: The Tanner top-down design flow for analog/mixed-signal design and verification.

As design and verification teams move through this design flow, they use libraries and PDK data as inputs and then generate data files and reports that should be under data management control. The best way to demonstrate this idea is by using a simple example. Figure 6 shows a successive approximation analog to digital convertor (ADC), with separate teams working on the ADC blocks, and the associated design files (and directories) created.

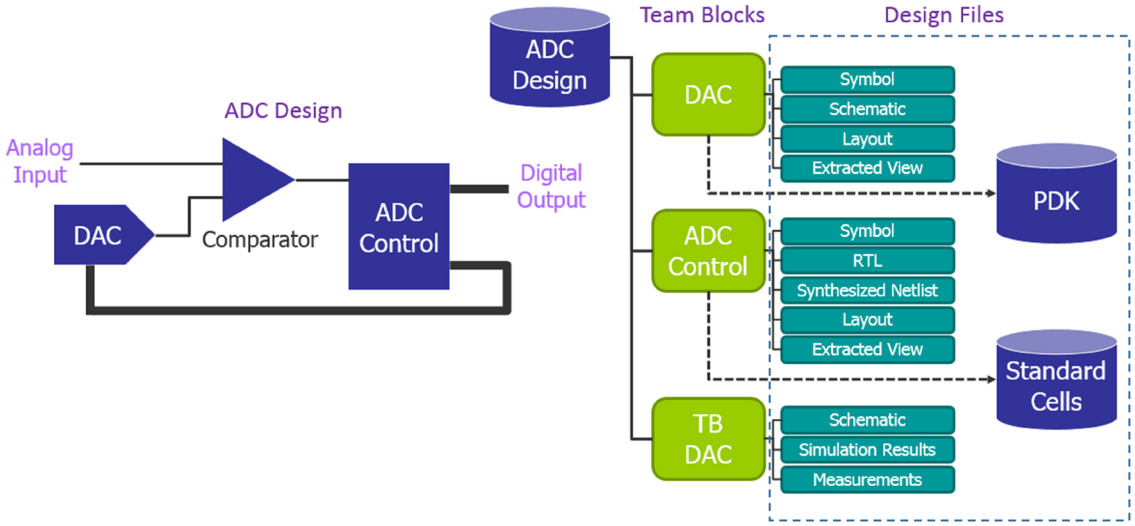

Figure 6: An ADC example divided between three teams.

The ADC design is divided between three teams working on three elements:

- The digital to analog converter (DAC) is an analog block that is comprised of a symbol, a schematic, the layout, and extracted view (including parasitics). A foundry PDK provides supporting data for this block.
- The ADC control is a digital block that is comprised of a symbol, the RTL description, synthesized gate-level netlist containing standard cells from a target library, the layout, and extracted view.
- Testbench (TB) for the DAC that is comprised of the schematic with measurements and the simulation results output.

As the teams work through their flows, the tools they run can use PDK, standard cell, or IP in a block library as inputs on the way to creating output data files. These inputs and outputs are design files that should be managed under SOS7.

SOS7 uses a repository to manage design data (Figure 7). A repository is an on-network-storage data structure that stores multiple versions of design files that the team can access from a server anywhere in the world.

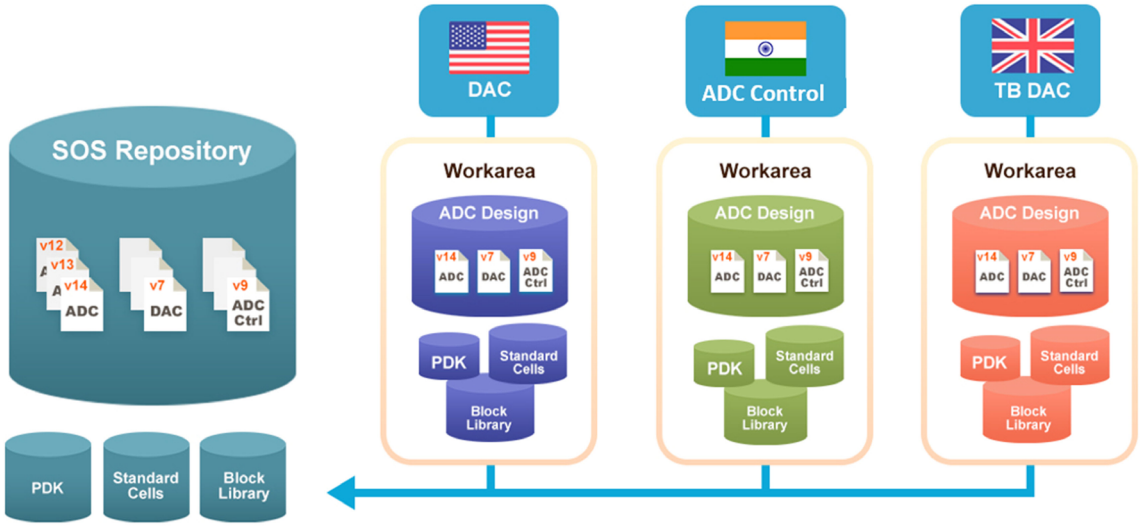

Figure 7: Team members interact with the repository.

Each version of the design file resides in the repository. When the designer wants to work on a block, he/she reserves a copy of the latest revision of ADC design which is placed into their own local ***Workarea***. After making a design change, the designer commits any changed files into the repository and the version number increments. The only network traffic to the repository for the commit process are the changed files. SOS7 manages the reservation and commit process so that team members do not overwrite their work.

AN EXAMPLE WALKTHROUGH

Let's take a look at walking through some of the design flow for the ADC. Within the S-Edit schematic tool, the DAC designer asks SOS7 for a reservation to work on the schematic view of the Comparator (Figure 8).

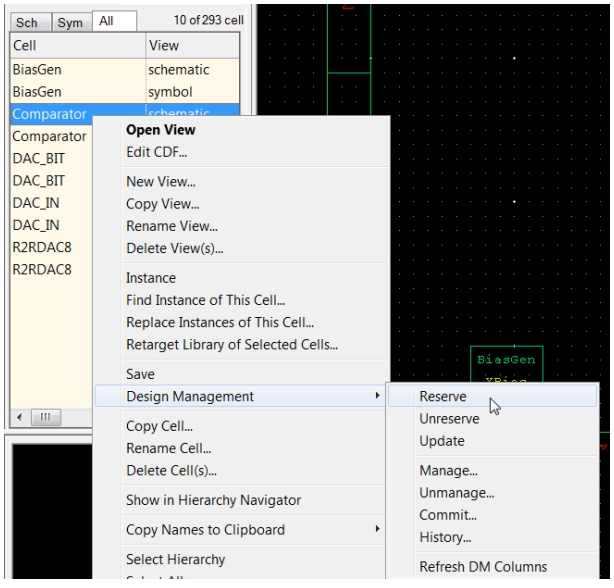

Figure 8: Making a reservation.

This explicit reservation locks the schematic view in SOS7 for editing, as long as someone else does not already have a reservation for it, which means they are working on it. If the designer just starts editing the Comparator schematic, this triggers an implicit reservation with SOS7, but the designer will be prevented from reserving the schematic if the view is already reserved by another person.

After the designer makes a change to the view and saves it in the local Workarea, he/she then commits the view back to the repository (Figure 9). The designer can add a message when the view is committed that indicates what changes were made. SOS7 automatically increments the revision number for the associated files.

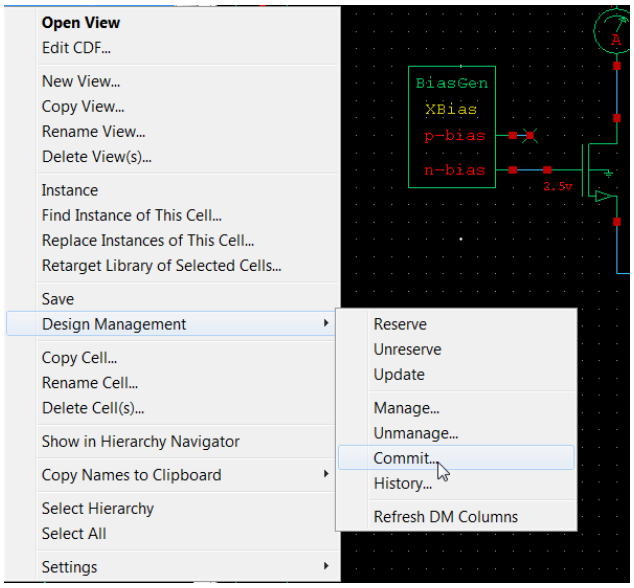

Figure 9: Committing the changed design to the repository.

At any given time, the designer can browse the entire design within the SOS7 user interface (Figure 10).

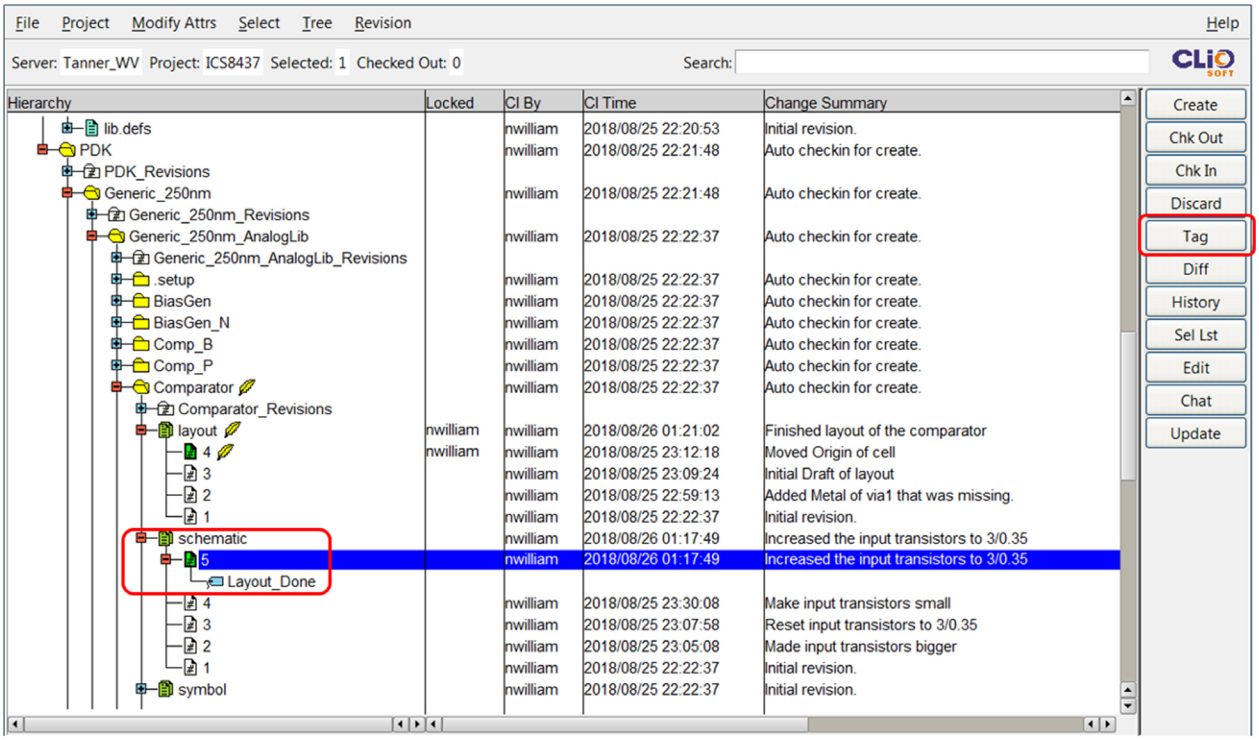

Figure 10: Interacting with the SOS user interface.

Within this user interface, the designer can tag a version of the design in order to notify the team of its status. For example, the designer could tag the schematic with a ***Design Done*** tag, which lets the layout designer know that work can begin in L-Edit (layout editor) using schematic-driven layout.

The design team then works its way through the flow by committing design revisions and using the tagging feature to indicate status (Figure 11).

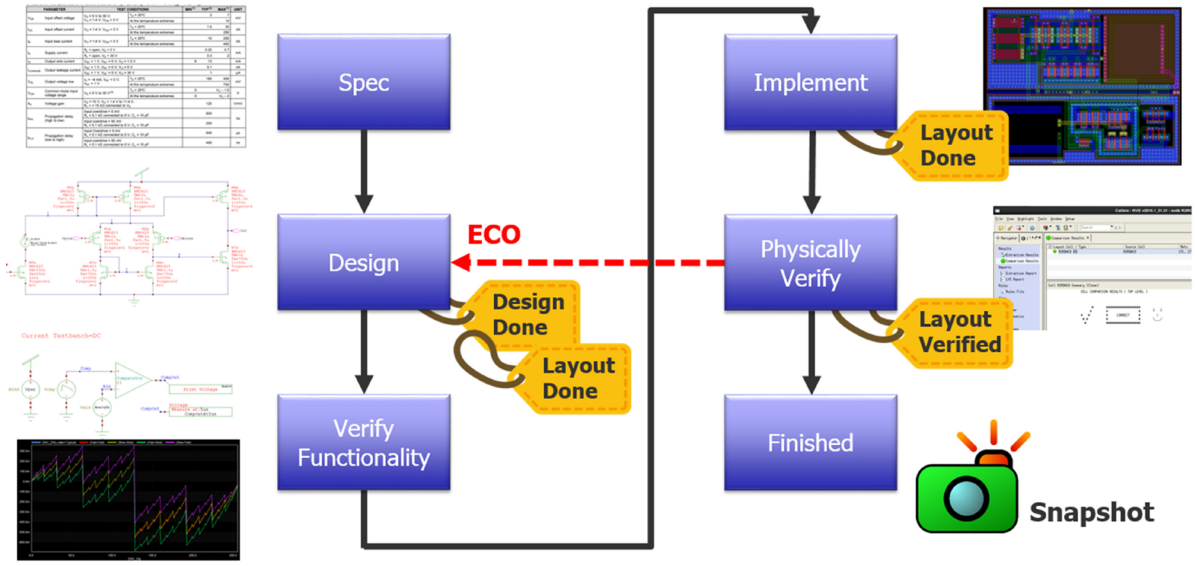

Figure 11: A typical design flow driven by the state of the project.

When the design is stable, or when tape out or a handoff needs to be made, the team can take a snapshot of the entire project. This allows them the flexibility to revert back to the exact set of files for that point in time as well as track what snapshots were used for handoff. This becomes useful when addressing issues found by a downstream team or if the team tapes out the design and then starts working on a variant, they can easily revert back to the snapshot taken at the time of the original tape out.

DECIDING WHAT DESIGN DATA TO MANAGE

Moving an IC design through a flow of tools means accumulating many files. But, not all files should be placed into the data management repository. Good design management practice recommends placing these files under data management:

- Design files, such a schematics, symbols, layout, and RTL descriptions.
- PDK, standard cell, and IP block libraries used in the project.
- Intermediate versions of design data to allow experimentation and rolling back versions that do not work for the project.
- Testbenches and stimuli files for simulation to track verification status.
- Simulation netlist, logs, measurement results, and plots for audit, review, and documentation purposes.
- Physical verification files, such as the DRC summary log, DRC run set, and waiver files; LVS summary log and run set.
- Place and route logs and reports for audit purposes.
- Documentation, including requirement specifications and any documents that record useful information about the design.

Files that should not be placed under data management include:

- Temporary or scratch designs, because they are not part of the project.
- Actual simulation results or DRC and LVS results databases, which are easy to recreate and are typically very large files.

CONCLUSION

Complex, multi-domain IC design coupled with tight schedules means that teams cannot afford to spend time tracking down problems due to using the wrong version of design files. Managing design data efficiently is a critical component for successfully taping out the design and managers need to know if the team is hitting critical milestones for the project. The integration of ClioSoft SOS7 within the Tanner custom IC flow ensures that all team members collaborate within a managed design data environment.

LEARNING MORE

- To learn more about data management with ClioSoft SOS and the Tanner IC design flow, view this seminar.
- To explore the Tanner IC design solution, view this web page.

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