IMPLEMENTING AN IOT EDGE DEVICE WHILE MINIMIZING NRE

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WHITEPAPER

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AMS DESIGN & VERIFICATION

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INTRODUCTION

A new breed of designers has arrived that is leveraging inexpensive sensors to build the intelligent systems at the edge of the Internet of Things (IoT). Hardware design is on the rise. One designer in a garage, a small startup, small to mid-size companies, and even small groups within large companies with a "startup attitude" are designing IoT edge devices (Figure 1). These designers need to keep non-recurring expense (NRE) down by using affordable design tools that are easy to use to quickly produce results and by minimizing IP and fabrication costs. Their goal is to deliver a functioning device to their stakeholders while spending as little money as possible to get there. They require a proof-of-concept in order to make a fast go/no-go decision and then they rapidly implement solutions using integrated tool flows that allow them to quickly develop hardware, embedded software, and unique form-factor PCBs.

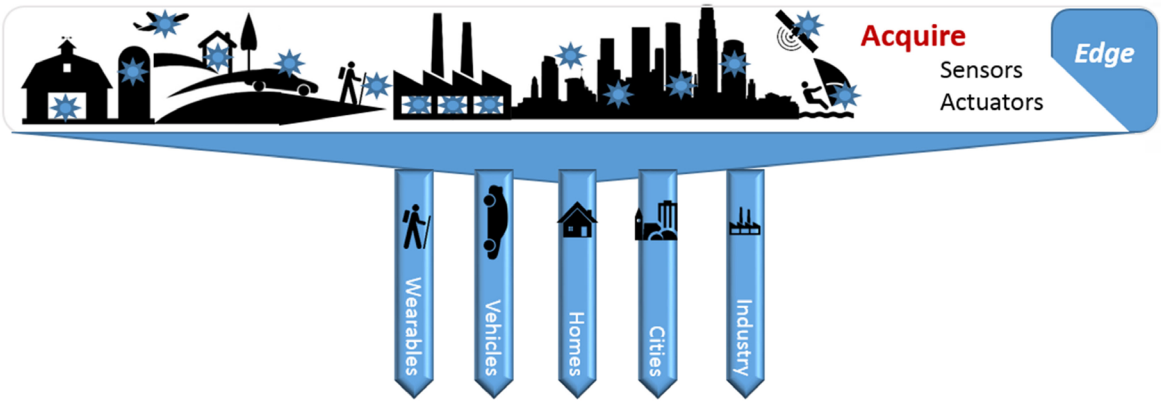

Figure 1: Edge devices for the Internet of Things.

The electronics industry believes that the IoT is the next big market wave. How big is the opportunity in IoT edge design? The IC Insights – IC Market Drivers 2017 (June update) report shows that in 2016, the estimated market was $74.6 billion, growing to a forecasted $124.1 billion by 2020 (Figure 2) in wearables, connected vehicles, connected homes and cities, and industry IoT (IIoT). And this is purely the IoT edge market that does not include products such as gateways, servers, computers, smartphones, or tablets. It obviously does not include the actual cost of a home, vehicle, buildings, or industrial equipment either.

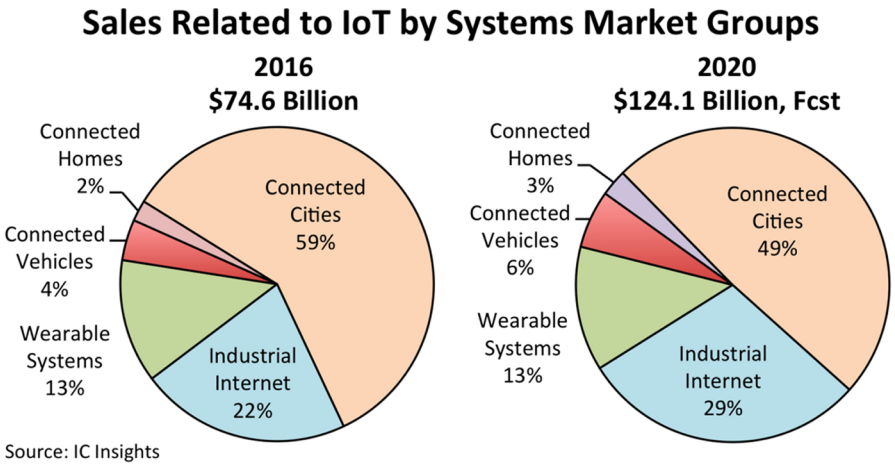

Figure 2: IoT device market data present and future.

In addition to IoT devices, the same IC Insights report shows that the IoT edge semiconductor market grew 18% in 2016, to support the growth in IoT edge product design. Figure 3 shows the 2016 semiconductor revenue split based on market segments.

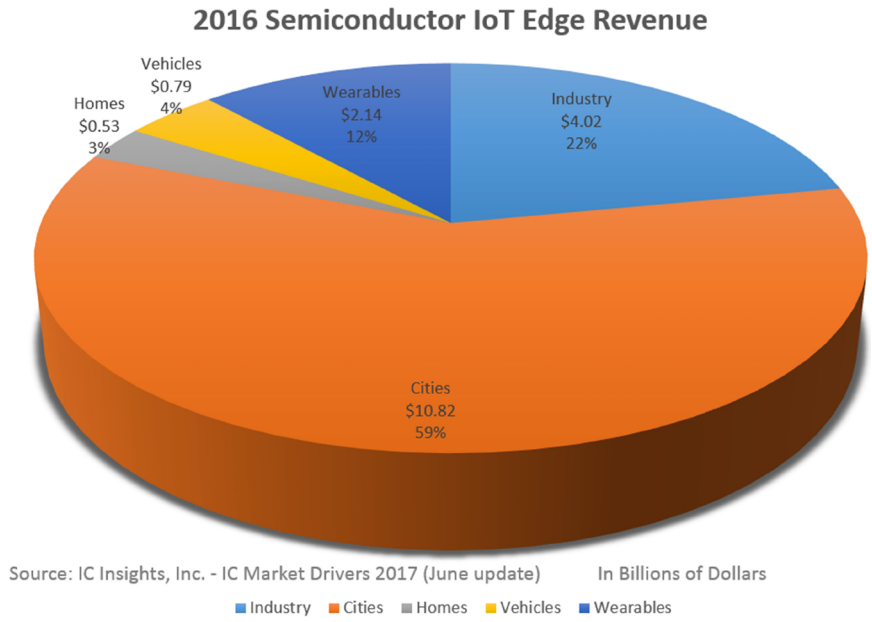

Figure 3: IoT edge device semiconductor market in 2016.

The investment in connected cities is currently the driver of IoT edge semiconductors, followed by the IIoT and the consumer wearables market. Analysts believe that both IIoT and connected vehicles segments are the next growth markets.

Given the size of the IoT edge market and projected growth, the new breed of designers are driven to create their products as efficiently as they can to get to market quickly. It might not be intuitive when companies first think about it, but these designers are exploring and implementing custom SoCs for their products.

WHY CREATE A CUSTOM SOC FOR IOT EDGE DEVICES?

Reading reports and articles stating that many millions of dollars are required to create a custom SoC, one would think that this new breed of designers is simply putting discrete components on PCBs to keep costs down. However, this is not the trend. imec IC-link reported last year that SoC design starts at their organization grew at 15% CAGR, for example.

Creating a custom SoC for IoT an edge device versus using discrete components for the product can offer these benefits:

- Reduction in the bill-of-materials (BOM) cost
- Size reduction
- Lower power consumption
- Greater performance

- Increased reliability
- Defense against discrete component obsolescence
- Protection of intellectual property (IP)
- Greater barriers to entry for prospective competitors

But, there are many factors that must be evaluated before committing to designing a custom SoC, including:

- Cost to design and fabricate, profit/loss projections, breakeven point, versus current costs
- Target market size and target market share
- Time to market
- Production volume and life cycle
- Competition
- Fabrication technology

This paper assumes that the designers have weighed these factors, done the math, and have come to the conclusion that the next IoT edge project will employ a custom SoC.

The choice of the fabrication technology is a key consideration for the project. An IoT edge device, by definition, requires a communications block with analog subsystems to connect with the Internet. Leading-edge technologies are not optimal for this type of design. For example, at 180nm, designers have access to 3.3v supply voltages which allow good dynamic range and noise margins for creating efficient RF antennas. The cost of fabricating a design at 180nm is orders of magnitude cheaper than 28nm.

GETTING A PROOF-OF-CONCEPT FOR ZERO DOLLARS

IoT edge designers initially focus on keeping NRE as low as possible, not on lowering the unit cost of the device. If the product is successful, they can reduce unit cost as they move forward into the market. The goal is to get a working product to demonstrate to management or to venture capitalists in order to prove that the project should continue to the next level.

The working definition of NRE in the context of this paper is: the cost of EDA tooling, third-party IP, and an initial fabrication run to obtain SoC samples. Because designer salaries are recurring, that cost is not included.

The whitepaper here discusses how to create proof-of-concept SoC that includes a sensor, analog and digital logic, a processor, and software for zero cost. Mentor offers a 30-day, free evaluation of the Tanner EDA tools that designers can use to design and simulate a proof-of-concept SoC. Tanner provides a complete AMS IC solution in a highly-integrated end-to-end flow. For a proof-of-concept project, designers can create the AMS schematic using S-Edit to integrate an Arm® Cortex®-M0 or Arm Cortex-M3 processor and simulate the entire design using T-Spice and ModelSim.

IMPLEMENTING AN IOT EDGE DEVICE

After creating the proof-of-concept, it is time to move into the actual implementation stage. This requires allocating budget for EDA tooling, IP, and the fabrication of the SoC (Figure 4).

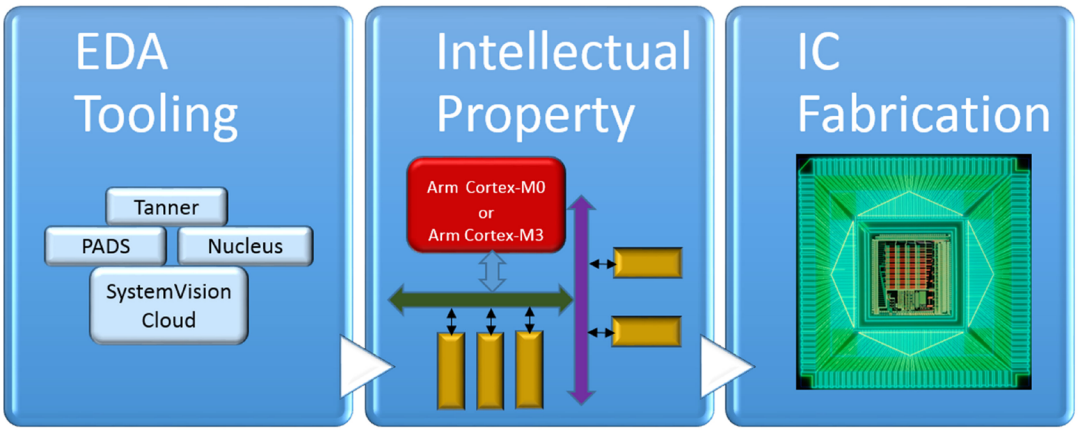

Figure 4: IoT edge design implementation cost.

EDA TOOLING

The IoT edge design team needs to capture a mixed analog, digital, RF, and sensor design, lay out the chip, and perform both component and top-level simulation and verification. The embedded software engineer writes and tests programs for the IC and the team explores the system in order to prove their concept within the context of the overall product. Then, a designer creates the custom PCB and a team member documents the design. Mentor offers a complete solution to IoT edge device design teams (Figure 5).

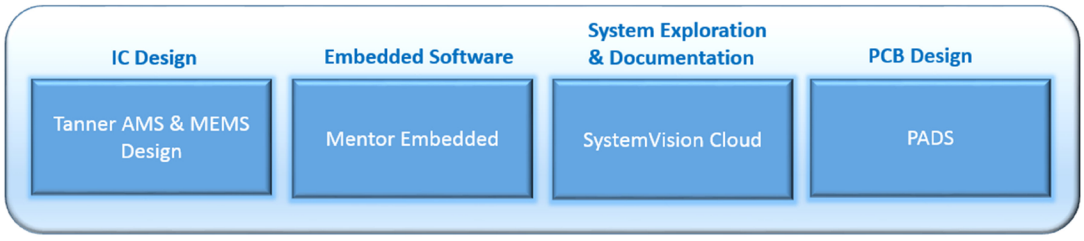

Figure 5: The complete IoT edge solution.

AMS IC DESIGN

IoT edge IC design requires that all four design domains (analog, digital, RF, and MEMS) are designed and work together, especially if they are going on the same die. Even if the components are targeting separate dies that will be bonded together, they still need to work together during the layout and verification process. The Tanner solution delivers a top-down flow (Figure 6) for IoT IC design, unifying the four design domains and providing a complete, integrated AMS design flow that is flexible and easy to use, speeding time to working silicon.

Figure 6: The Tanner AMS IC design flow.

The IC and MEMS design flow includes the tools in Figure 7, providing a complete design and verification environment for IoT edge devices.

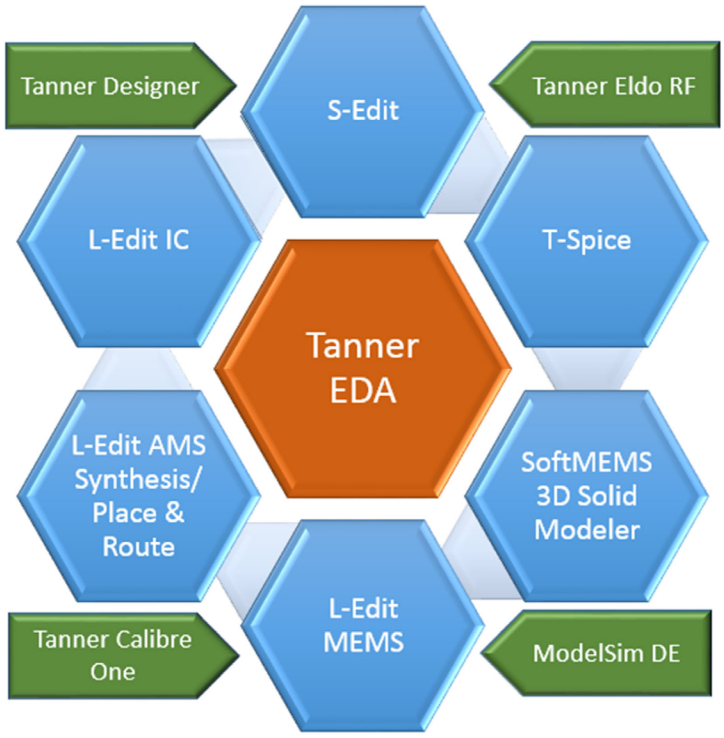

Figure 7: AMS and MEMS IC tools.

Whether the team is designing a single die or multiple die IoT device, they can use this design flow for creating and simulating the device:

- **Capturing the design**. S-Edit captures the design at multiple levels of abstraction for any given cell. Each cell can have multiple views such as a schematic, RTL, analog behavioral, or SPICE and then choose which view to use for simulation.
- **Digital implementation.** The L-Edit AMS digital implementation solution is optimized for big analog/little digital designs and it includes RTL synthesis, timing-driven placement and routing, clock tree synthesis, and timing extraction and reporting.
- **Simulating the mixed-signal design**. S-Edit creates the complete Verilog-AMS netlist and passes it to T-Spice. T-Spice automatically adds Analog/Digital connection modules and then partitions the design for simulation. T-Spice simulates the analog (SPICE and Verilog-A) and sends the RTL to ModelSim for digital simulation. Both simulators are invoked automatically and during simulation the signal values are passed back and forth between the simulators whenever there is a signal change at the analog/digital boundary. This means, that regardless of the design implementation language, designers drive the simulation from S-Edit and the design is automatically partitioned across the simulators. Then, they can interact with the results using the ModelSim and T-Spice waveform viewers. Behavioral models of MEMS devices can be created in Verilog-A or as equivalent lumped SPICE elements that are simulated along with the digital models for system-level verification.
- **Simulating the RF block**. Tanner Eldo® RF provides RF verification for the IoT device by employing a set of dedicated algorithms to accurately and efficiently handle the low-power signals in these devices. The tool

provides a wide range of analysis capabilities, a set of RF-dedicated functions, and a powerful set of optimization algorithms suitable for various types of circuits. Analysis modes include:

- Shooting Method/Periodic Steady State (PSS);
- Modulated Steady-State Analysis with RF/Baseband Partitioning;
- Multi-Tone Steady-State Analysis (Harmonic Balance).

- **Managing analog verification**. Tanner Designer aggregates simulation results and presents results in a dashboard throughout the lifecycle of the project.
- **Laying out the design**. The physical design is completed using L-Edit IC which allows designers to create the layout of the analog components for the IoT design and to utilize schematic-driven layout (SDL) to automatically place parameterized cells. The parameterized layout library of common MEMS elements and true curve support simplify the MEMS layout (covered the next section).
- **Performing physical and circuit verification.** The Tanner Calibre® One verification suite in the IoT flow includes the following capabilities:
  - DRC (hierarchical design rule checking) ensures the physical layout can be manufactured. This industry-leading tool provides fast cycle times and innovative design rule capabilities.
  - LVS (hierarchical layout versus schematic) checks that the physical layout is electrically and topographically the same as the schematic. It improves productivity by providing actual device geometry measurement and sophisticated interactive debugging capabilities to ensure accurate verification.
  - A graphical results viewing environment that reduces debug time by visually identifying design issues instantly and cross-selecting the associated issue in L-Edit and S-Edit tool.

MEMS DESIGN

Teams could create a 3D model of the MEMS device using a 3D analysis tool and then analyze its response to different physical effects. But, to fabricate the MEMS device, they need a 2D layout mask and deriving a 2D mask from a 3D model is error-prone and difficult to validate. A better approach is to follow the mask-forward flow (Figure 8), that results in more confidence that the MEMS device will not only work correctly but that it can be successfully fabricated.

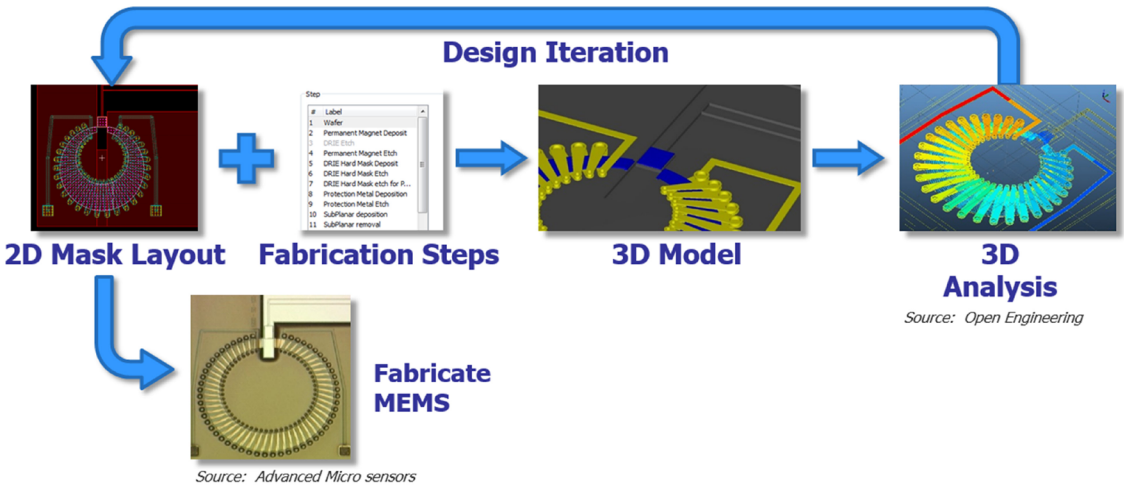

Figure 8: The Tanner mask-forward MEMS flow.

The mask-forward MEMS design flow starts by creating the 2D mask layout in L-Edit using L-Edit MEMS which provides specific support of integrated MEMS and IC design with true curve support. Then, designers use the SoftMEMS 3D Solid Modeler (integrated within L-Edit) to automatically generate the 3D model from those masks and a set of specified fabrication steps. They perform 3D analysis using a 3rd-party finite element tool and then iterate if any issues are discovered. The designer makes the appropriate changes to the 2D mask layout and then repeats the flow. Using this mask-forward design flow, the team can converge on a MEMS device that they are confident can be fabricated correctly because they are creating the 3D model directly from the masks that will eventually be used for fabrication, rather than trying to work backwards from the 3D model.

EMBEDDED SOFTWARE

Mentor Embedded provides a portfolio of real-time operating systems (RTOS) and tools that enable the development of embedded software for IoT edge devices. For resource-constrained and battery-powered IoT edge devices, choose the scalable Mentor Embedded Nucleus® RTOS.

The Nucleus RTOS is deployed in over 3 billion devices and it provides a micro-kernel based real-time operating system designed for scalability and reliability. System reliability is improved using lightweight memory partitioning that can function with or without MMU/MPU assisted protection in IoT edge systems. To meet the power requirements, designers can take advantage of integrated power management that includes support for dynamic voltage and frequency scaling (DVFS), deep sleep modes, and power/clock gating.

For embedded software development, designers can use Sourcery™ CodeBench (Figure 9). This tool provides designers with open source, embedded C/C++ development tools to build, debug, analyze and optimize embedded software in heterogeneous architectures including ARM.

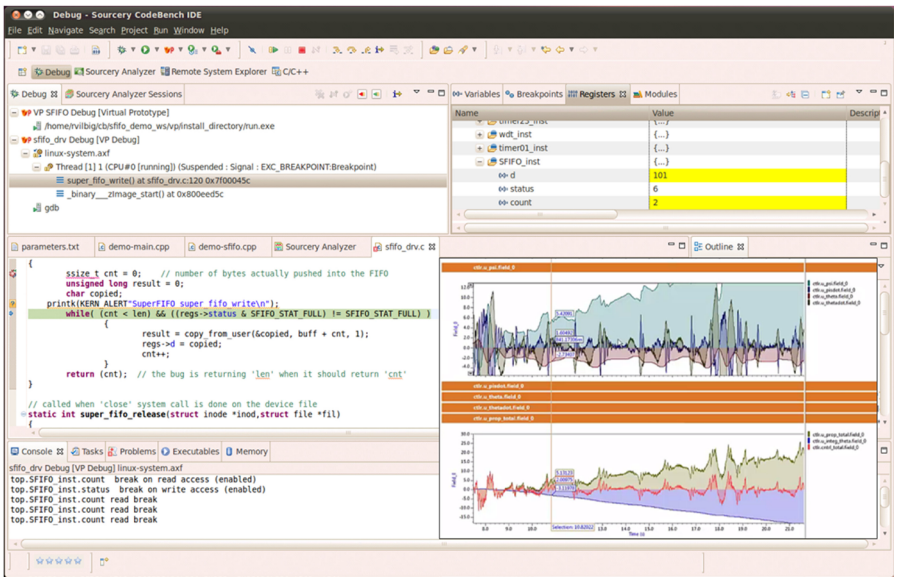

Figure 9: Using Sourcery CodeBench to analyze embedded software.

With Sourcery CodeBench, teams can develop embedded systems on microcontrollers and microprocessors. The growing complexity of embedded systems requires greater insight into system execution and performance and new approaches to debugging applications. Designers can use Sourcery CodeBench to quickly identify and fix functional and performance issues in these embedded systems.

SYSTEM EXPLORATION AND DOCUMENTATION

The SystemVision® Cloud environment (Figure 10) provides an online environment to capture a system using a variety of electronic circuit and mechatronic system building-block models and then use state-of-art simulation technology and in-context results viewing to analyze the system. Designers can use this environment to quickly explore system ideas and prove concepts by seamlessly mixing control system blocks, analog and digital circuits, mechatronics, and multi-discipline sensors and actuators in the environment.

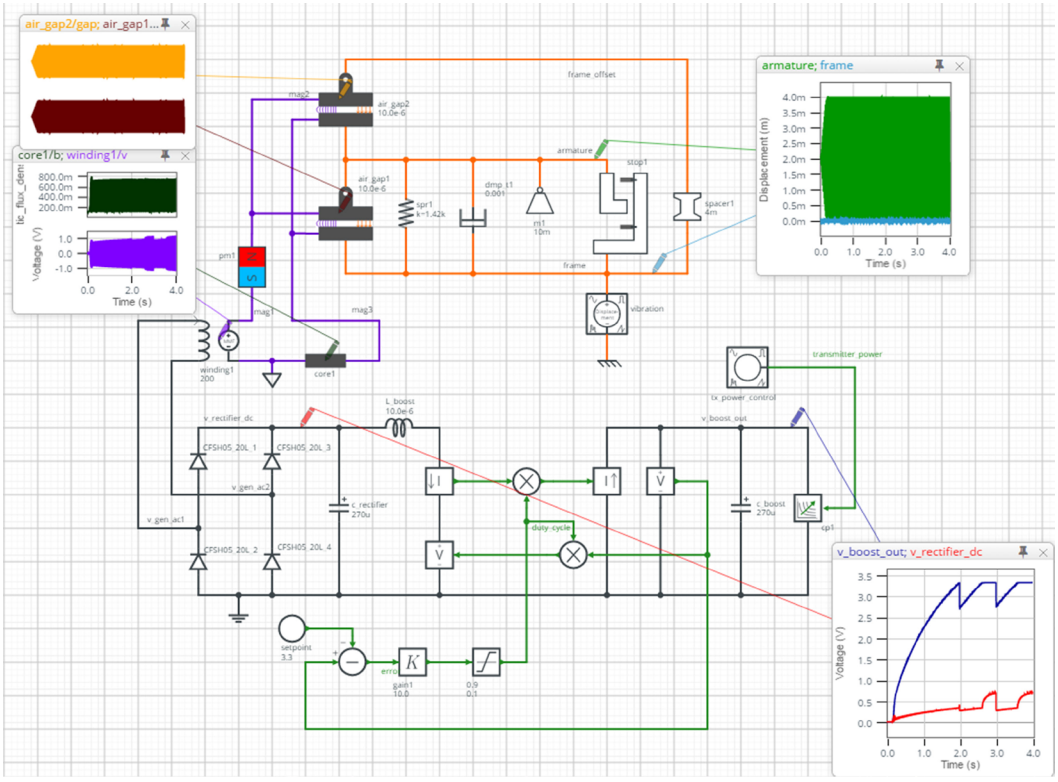

Figure 10: An interactive energy harvesting system in the SystemVision Cloud.

SystemVision Cloud allows teams to embed live designs and waveform results in online documents, similar to embedding a video. The content is live, meaning it can be viewed and manipulated right in the document. By interacting with a live schematic and its simulation results, teams can develop a much deeper intuition about the system concept, design parameters, and performance characteristics.

PCB DESIGN

PADS® Standard (Figure 11) provides schematic capture and board layout capabilities in an intuitive and easy-to-use environment. PADS Standard is geared for designers looking for production-proven tools where low-cost is a high priority.

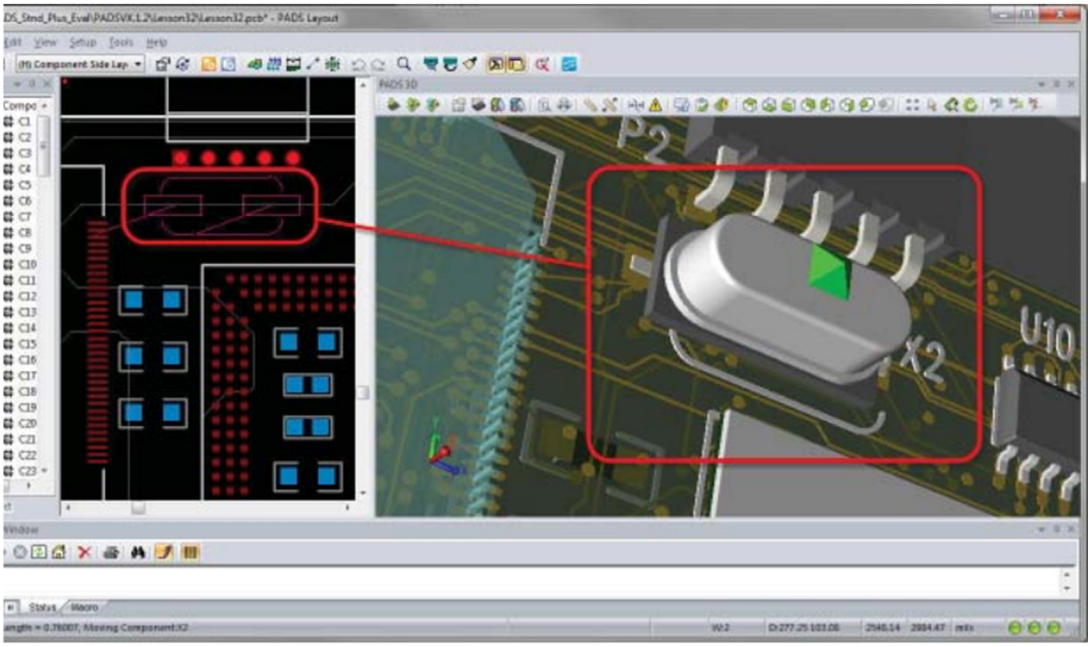

Figure 11: PADS Standard is an easy-to-use PCB design flow for the individual designer.

PADS Standard includes capabilities for system design capture and definition. Intuitive project and design navigation, complete hierarchical support, a starter library, and advanced design attribute and design rules management make it easy to capture and define the schematic. Designers can achieve efficiency and productivity with full forward and backward annotation to layout and routing. PADS includes all design rules and constraints with online DRC.

The advanced layout and routing capabilities in PADS save hours of design time. The combination of design rules with real-time design rule checking and bi-directional cross-probing ensures that boards adhere to design specifications, eliminating costly fixes after prototype and manufacturing. Split and mixed planes are also easy to create and modify, making customized thermal connections simple. RF capabilities include via-stitching for easy creation of co-planar wave guides and the ability to flood a region with vias according to the team's rules.

With PADS Standard, designers have access to photorealistic visualization of the PCB that helps eliminate costly and time consuming errors by viewing the PCB in 3D and identifying conflicts with mechanical objects. Designers can export the 3D assembly into STEP, 3D PDF, JPG, BMP formats.

INTELLECTUAL PROPERTY

Because it cannot be known what IP blocks your project requires, this paper only addresses IP in the context of Mentor's partnership with Arm.

Arm recognizes that there are significant advantages in creating custom SoCs versus using off-the-shelf chips – increased functionality and differentiation, product design protection, and lower bill of materials (BoM), to name a

few. Arm also recognizes that sensor and mixed-signal companies, as well as startups or small teams need to be able get started quickly and easily, and with minimal costs.

To help accelerate innovation, Arm offers the DesignStart™ program (Figure 12) – the simplest, fastest, lowest-risk route to industry-leading Arm IP for no upfront fee. Arm also offers approved design partners, training, and support for SoC development help.

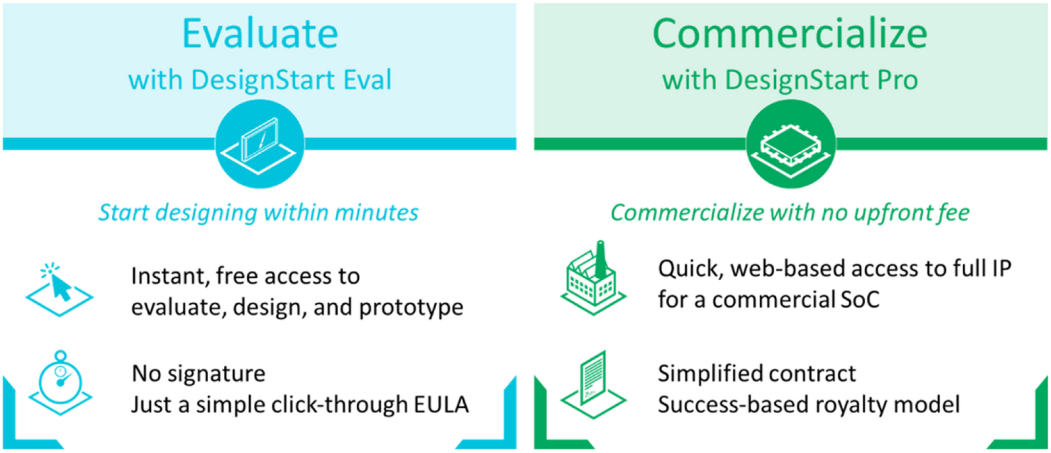

Figure 12: Accessing proven, trusted IP has never been easier with Arm DesignStart Eval and Arm DesignStart Pro (Source: Arm).

There are two ways to access industry-leading processor IP through DesignStart:

- Arm **DesignStart Eval:** anyone can get instant, free, click-through access to Arm Cortex-M0 and Cortex-M3 processors, as well as their system IP. Designers can configure or modify the subsystem, add their own IP and peripherals, and then prototype on an FPGA.
  Key benefits include:
  - Fast start to designing and simulating custom SoCs
  - Simple FPGA prototyping
  - Simple and quick access to EDA tooling
  - Forum-based support
- Arm **DesignStart Pro:** for companies looking to develop their own chip. Companies simply register on the Arm DesignStart website, sign and return a simplified contract, then start building their chip. No upfront fees are required, just a simple success-based royalty once the design is in production.
  Key benefits include:
  - Fast, simplified, no-risk access to Cortex-M0 and Cortex-M3 processors and system IP for commercial chip development
  - Develop a complete IoT or smart embedded solution using Cortex-M3, with a verified subsystem design, and enhanced design services

ADDITIONAL IP CONSIDERATIONS

While the 2016 Semico Research Corporation "Licensing, Royalty, and Services Revenues for 3rd-Party SIP" report states, "It is anticipated that a large portion of IoT SoCs will require low-to-moderate levels of functionality and, correspondingly, lower amounts of IP," a project could require additional IP blocks that can drive up

implementation cost. For example, this report shows that security IP (key generation and encryption/decryption engines) had an average license cost of $89.6K in 2016. This cost does not include royalty fees or services.

IC FABRICATION

To obtain fabricated samples of the custom SoC at a low cost, teams often consider multi-project wafers (MPW). This concept allows multiple companies to share mask costs by grouping multiple designs onto a silicon wafer. Most foundries provide scheduled MPW shuttle schedules and teams can also use 3rd-party MPW services provided by organizations like MOSIS, eSilicon®, and EUROPRACTICE to help. For example, EUROPRACTICE reports that teams can obtain 45 IC samples at 180nm for $16K. They also state that a repeat order of 45 samples costs another $2K. While the 180nm is a mature process, it works well for AMS with RF designs. As the product becomes successful, teams can consider moving to newer processes as requirements change.

ACCOUNTING FOR ADDITIONAL COSTS

The focus of this whitepaper is containing NRE costs while designing, verifying, and fabricating the custom SoC, and designing the PCB and the embedded software to complete the IoT edge product. So, downstream costs such as product enclosures, retail packaging, and marketing are not included. However, there are several actions that can increase costs in the context of flow covered in this whitepaper, such as:

- Including additional IP blocks
- Opting for design consulting services
- Choosing a different process node
- Purchasing additional EDA tools
- Fabricating the PCB[1]
- Performing additional analysis and verification steps in the design process, such as finite element analysis (FEA) for MEMS[2]

While testing the IC samples from the foundry, teams might find that they have a design flaw. This can trigger a re-spin of the MWP, which will add to costs. The project planning should take into account potential problems, such as re-spins or project delays, and provide alternate scenarios and associated costs should these occur.

DECIDING TO MOVE TO FULL PRODUCTION

At this point, the team has a working product to show potential investors or management at the company. Moving to full production typically means working with a foundry to develop a mask, instead of using the MPW technique. There are many equations that companies use to decide when to make this move, with variables such as the technology process node, predicted sales, and fabrication costs. For example, it is estimated that for 180nm when teams reach 2000 ICs, they should consider a dedicated mask, which costs about $150K. By contrast, it is estimated that at 90nm, teams switch over to a dedicated mask at around 6000 ICs and the mask cost is around $500K. However, actual cost is established by foundry partners.

1 There are many companies that will fabricate 10, 2-layer printed circuit boards for under $100.

2 Mentor does not currently offer an FEA tool.

Next Steps

This whitepaper is part of an ongoing series of topics that detail the implementation of IoT edge devices. To learn more about creating a zero cost proof-of-concept, see the whitepaper here. To take the next step, learn how to prepare for an IoT edge project by reading the whitepaper here.

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