Application Note - Parasitic Resistor Models

For applications where the parasitics of circuit components can affect the circuits performance it is sometimes required to simulate the parasitics for devices at the schematic simulation stage. This application note describes how to use parasitic resistor models in your design flow. It includes details on the creation of the model, simulation, layout extraction and LVS. Similar techniques could be applied to other circuit elements, capacitors being one example.

Firstly a parasitic simulation model is described, then the extraction of the device and lastly, running LVS.

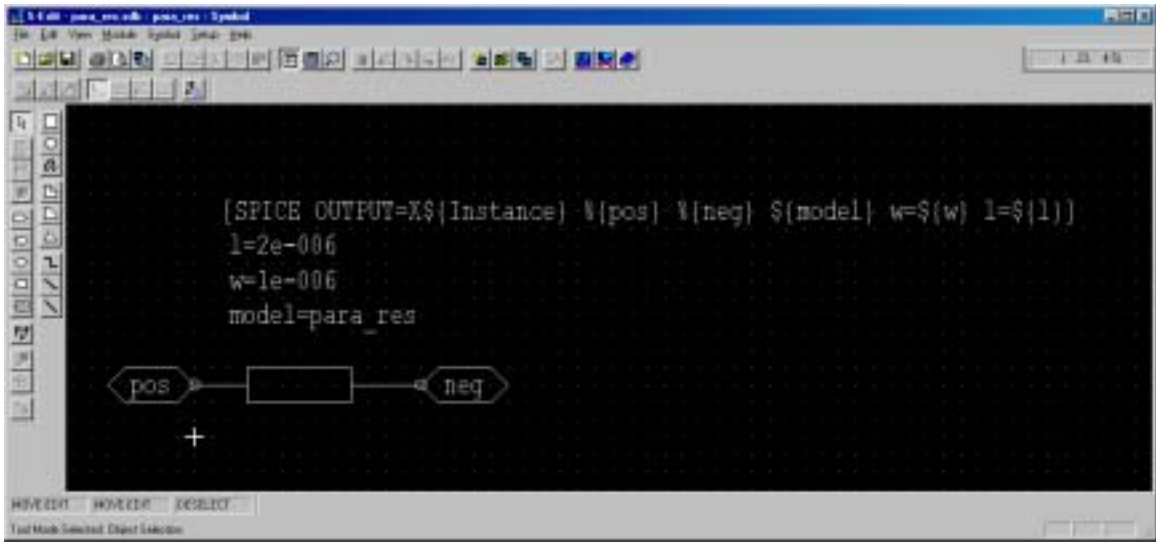
Test Case

A set of example files that demonstrate this flow are available for download. These are based on the technical setup that is used for Tanner training.

Parasitic resistor model

A “PI” model was used as the simulation model for the resistor. This is a simple example that works well. A symbol is required in S-Edit with the required properties for the device. In this example these are width and length. Associated with the symbol is the spice sub circuit for the simulation model.

The S-Edit symbol:



The spice sub circuit for the resistor:

```
**************************************************
*                                                *
*         Example Parasitic Resistor Model       *
*         Chris Pitchford 20th Sept. 2002        *
*                                                *
**************************************************

.param poly_sheet_res=1000
.param poly_area_cap=50E-18

.subckt para_res pos neg  w=1e-6 l=1e-6
R1 pos neg para_res R='(l/w)*poly_sheet_res'
C1 pos 0 c='0.5*l*w*1e12*poly_area_cap'
C2 neg 0 c='0.5*l*w*1e12*poly_area_cap'
.model para_res R
.ends para_res
```

Please note that the .model statement is required so that the device type is the same in the schematic and extracted layout netlists at LVS time.

This file is included in netlist generated by S-Edit by the use of an include statement:

.include para_res.md

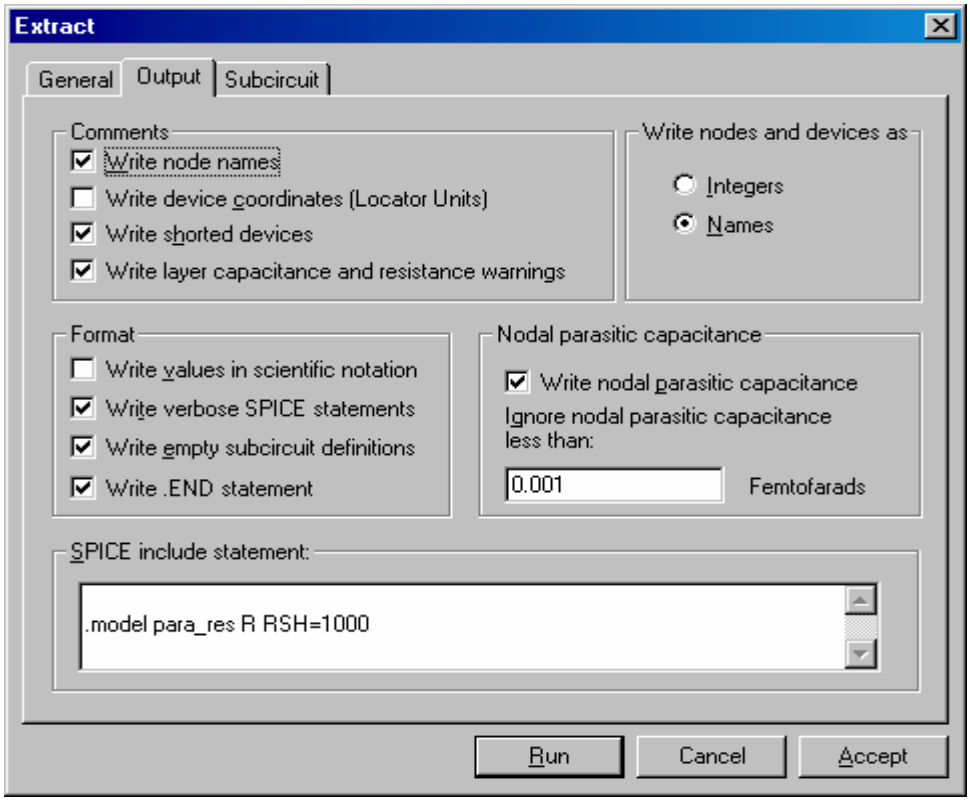
In my case, for convenience, I used a symbol with a SPICE OUTPUT property with a text value set to the above statement.

Layout Extraction:

The resistor is extracted using the “LW” keyword after the device recognition layer is specified in the extraction file:

```
# Poly resistor
device = RES(
      RLAYER=resistor body, LW;
      Plus=resistor contact;
      Minus=resistor contact;
      MODEL=para_res;
      )
```

By doing this the length and width of the device are put into the extracted netlist instead of a resistance value calculated for the device. A .model statement is also required in the extracted netlist. This is used to specify the sheet resistance of the resistive layer used to create the device. It enables the actual resistance of the device to be calculated. The .model statement is included in the extracted netlist by using the output section of the Extract form:

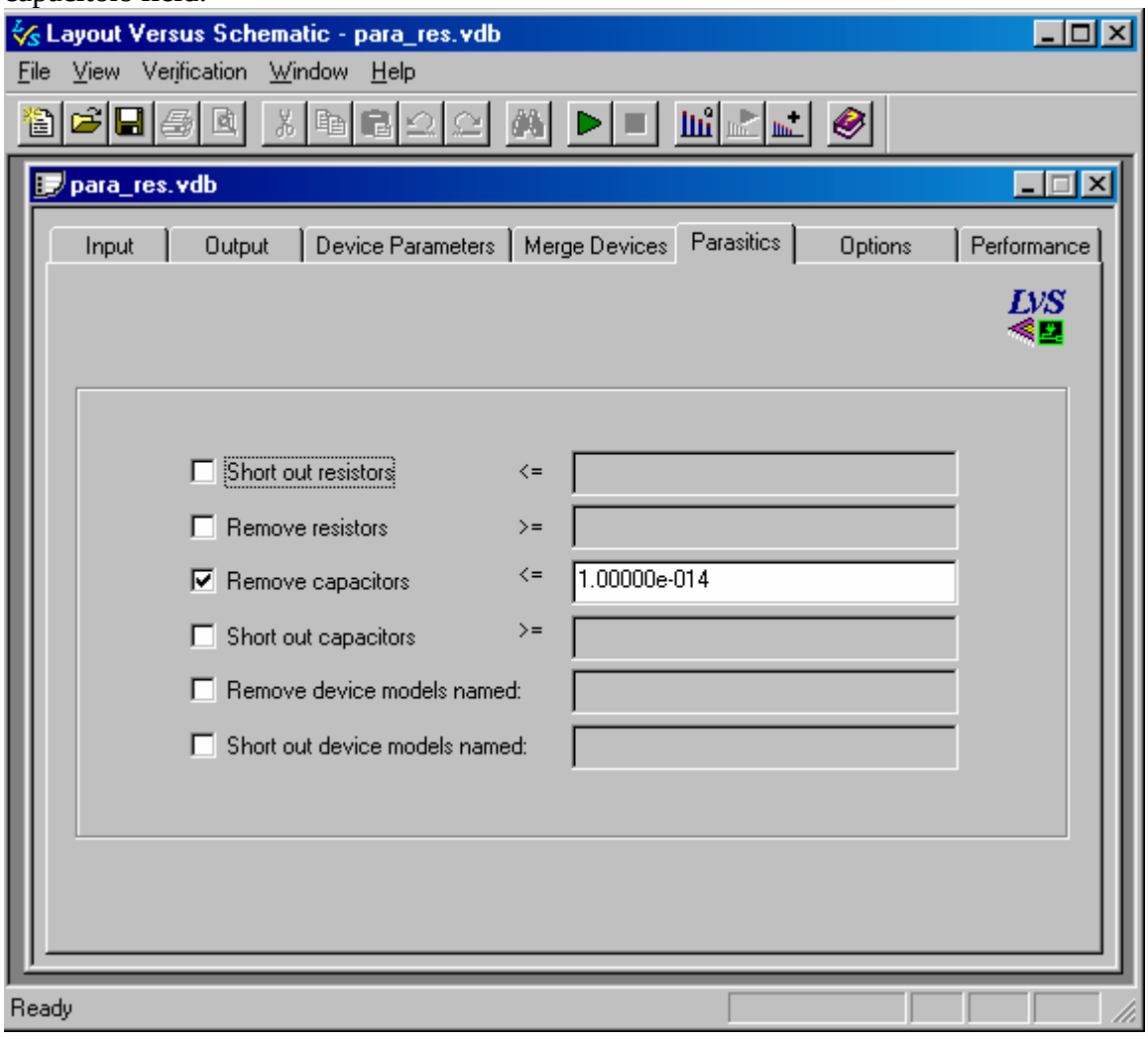


An example resistor that was extracted using the extraction rule and .model statements as shown above:

R1 P3 P2 para_res L=21u W=7u

LVS

The only thing to watch when running LVS is that the parasitic devices are removed from the schematic netlist and from the extracted layout netlist if parasitics have been extracted. To do this select the parasitics tab on the LVS setup form and use the Remove capacitors field:



Please Note: the “Remove capacitors” and “Short out capacitors” fields have their functionality swapped in L-Edit version 9.0. This has been corrected in L-edit version 9.1.