CUSTOMER CASE STUDY

L-Edit puts static protection on the road

Just one electrostatic discharge (ESD) can kill an integrated circuit (IC) and this has become a major headache for manufacturers as they try to shrink their designs to increase performance and reduce costs. Rapid advances in deep submicron technology have led to dramatic reductions in the amount of die space needed for core circuitry. But reductions in IC size are being held back by the size of the I/O ring around the core.

The threat from ESD is always there, and the risk of an IC being destroyed by a discharge increases with the reduction in transistor size. So, IC manufacturers are forced to devote space in the I/O ring to specialised

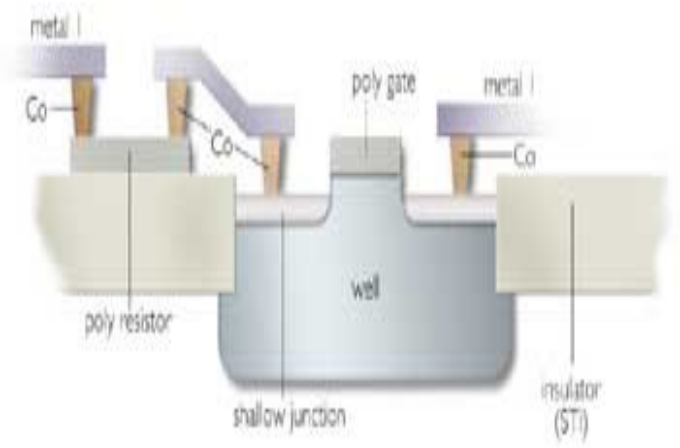

Figure 1

circuits that divert charge from an ESD strike away from delicate transistors. Manufacturers who use traditional approaches to on-chip ESD protection have been therefore unable to take full advantage of the die size reductions promised by process improvements. Not only that, the techniques often used to reduce core damage from ESD can reduce the performance of the I/O circuit and the speed of the IC as a whole.

Some ICs are unable to use any form of ESD protection because traditional techniques would interfere with the high-frequency signals they need to function. “One example is in radio-frequency (RF) circuits, because of the capacitance that ESD protection generally adds”, said Henk De Blaere - Director Business Development, Sales & Marketing - of Sarnoff Europe, a silicon intellectual-property supplier specialising in producing innovative methods of protecting against ESD damage.

“More and more applications are in the real time domain. In order not to interfere with RF signal integrity our customers need very low additional capacitance for ESD protection. As a result, it has not been possible using traditional techniques to have an RF product with good ESD protection,” said De Blaere.

The engineers at Sarnoff have developed a number of layout techniques that result in ESD-protected I/O pads that take up less die area than traditional approaches and which also reduce the parasitic capacitance that reduces I/O bandwidth, making it possible for RF IC designers to adopt on-chip ESD protection. In a typical 180nm CMOS process, the area needed for driver and ESD-protection transistors can be cut by 30%. “In some cases, that has gone up to 70 to 80% reduction,” said De Blaere.

At the same time, ESD performance is increased by 60% and voltage clamping margin by 30%. The Sarnoff TakeCharge technology has been ported to leading edge processes, with a 65nm version already released and a set of cells for the 45nm processes that are expected to arrive later this year under development. Since its launch, TakeCharge has been licensed by many of the top IDM and Fabless IC manufacturers, including Hynix, Infineon, Sony, Toshiba, OKI, New Japan Radio, Altera, PMC-Sierra and Scintera.

The TakeCharge technology relies on a number of custom-designed physical features. A large part of the development process is involved with designing and evaluating test chips. Since 2000, the company has implemented close to 40 individual test chips for a broad range of advanced standard CMOS and specialty process technologies, including pure-play foundry processes. The focus on testing the technology helps Sarnoff make sure its technology works for each customer’s individual process(es). “We guarantee a first-time-right ESD protection solution,” said De Blaere.

To design its test chips, Sarnoff uses the L-Edit layout tool from Tanner EDA. Bart Keppens, who is the lead designer of the test chips at Sarnoff Europe, said the high-end tools have many options that take time to set up and which are not necessary for test chips that contain a large number of simple circuit elements. “We are doing test chips with a limited number of features. The circuits we draw are quite simple: for ESD, simpler is better,” said Keppens.

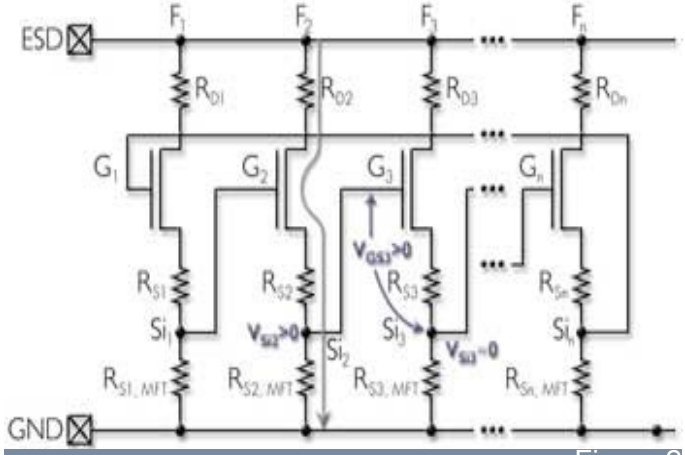

Figure 2

EDA Solutions, 58 Botley Road, Park Gate, Southampton, SO31 1BB, UK
T: +44 (0) 1489 564253 F: +44(0) 1489 557367 E: info@eda-solutions.com W: www.eda-solutions.com

L-Edit has a number of features designed to improve productivity. One of them is its powerful language for defining layout macros and parameterisable shapes. This allows commonly used structures to be set up once and deployed as needed across a test chip. Parameters inserted by the engineer during layout allow the structures to be customised for each instance.

“In the beginning, we were using L-Edit just as a polygon-drawing tool,” said Keppens. The Sarnoff team is now making extensive use of T-cells: “We use them every day. We are trying to make parameterised cells that are almost process independent for all the circuits we put on a test chip,” said Keppens, adding that the time invested to make the parameterised cells is expected to pay dividends as the company designs and builds more test chips. Since Sarnoff started using L-Edit, the company has begun to realise efficiency savings that can be made using the tool.

A further consideration was the ability to travel with the software. “We are often on the road, and we cannot take a Unix workstation with us,” said Keppens. Unlike its more expensive competition, L-Edit is designed to run under Windows, and a notebook PC running Windows is much more convenient for Sarnoff’s engineers to take with them when travelling. On top of these features, L-Edit came with the advantage of having a lower price tag compared with classic and longer established high-end layout tools, but has offered greater efficiency for designing test chips than the more expensive tools would have.”

Sarnoff has a number of projects under way to deploy its innovative ESD protection technology on not just advanced CMOS processes such as 65nm and 45nm, but also on a variety of silicon-on-insulator designs for the high-voltage processes used in automotive applications. Sarnoff will be designing many more test chips using L-Edit as its technology moves into new areas.

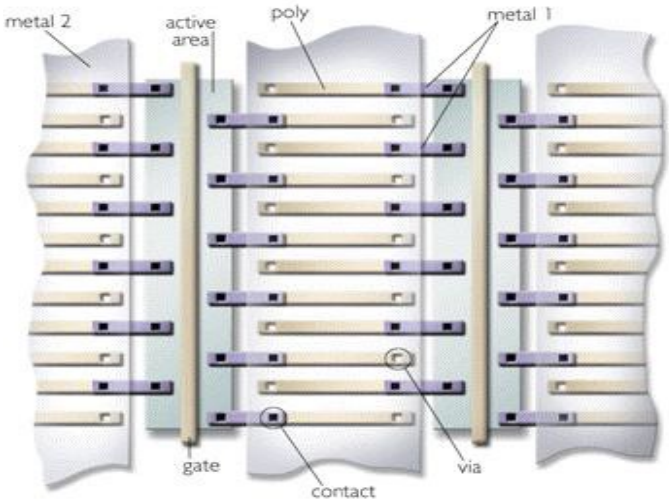

Figure 3