CUSTOMER CASE STUDY

Multi-project wafer service slashes design risk for novel wireless microcontroller

Based in Sheffield, UK, Jennic is at the forefront of the emerging market for chips for low-cost wireless sensors and actuators. According to analyst Frost & Sullivan, this market is set to explode over the next few years as home and industrial networking systems move to low-cost wireless technologies.

The main standards in this market are IEEE802.15.4 and Zigbee, which provides a standard software stack for sensor nodes to use. Thanks to the increased level of standardisation in what has been a highly fragmented market, Frost & Sullivan said the market for chipsets alone would grow from just $18.8m in 2004 to $700m in 2008. Realising the potential of IEEE802.15.4 and Zigbee, Jennic decided that market would prefer a high-integration solution to minimise costs in sensor nodes.

The company's response was the JN5121 wireless microcontroller, launched in September 2005. The JN5121 is unique in that it combines a 32bit RISC processor core with a radio transceiver that is fully compliant with the IEEE802.15.4 standard as well as 96Kb RAM and 64Kb ROM. In addition a comprehensive range of analogue peripherals is integrated including a 12-bit ADC, twin 11-bit DACs, two comparators and a temperature sensor.

Despite having all these functions, the chip itself fits into a package that is no bigger than 8x8mm - the size of less functional 16bit microcontrollers that lack radio functions but which are themselves aimed at small, low-cost systems such as sensor nodes. As a company, Jennic is no stranger to chip design although the JN5121 is the first to be sold by the company. Over the last nine years, the company has built up extensive experience in implementing designs in silicon, creating not just intellectual property cores for complex functions such as Serial RapidIO but entire chip designs for customers. "We have designed a number of chips for tier-one semiconductor suppliers," said Tony Lucido, vice-president of marketing at Jennic. "We decided to develop and sell our own solution this time. So it is the first chip that we have sold to customers directly but the people here have implemented many chips in the past."

However, combining digital cores such as microcontrollers with high-frequency analogue circuits brings significant risks, particularly when aiming at the relatively advanced processes needed to provide the necessary performance. The company wanted to use a 0.18µm process to produce the JN5121. For a process like this, non-recurrent engineering costs, including those needed to produce the masks for the design, are significant. A full mask set for this process can cost $250,000. If the design needed to be changed to improve RF performance or to solve problems, the cost could escalate easily to more than $500,000. "We knew there could be multiple iterations: we were designing complex structures," said Lucido.

Knowing that the radio portion of the design had the greatest design risk, the company looked for a way of minimising the cost of redesign and to test out its favoured architecture. The company alighted on the multi-project wafer (MPW) service offered by MOSIS. This allows different customers to share the cost of a mask set by placing multiple designs in the one reticule. For small designs, the cost savings are enormous.
Jennic's engineers had made use of MPW services in the past for customer projects.
A trial device incorporating both the RF transceiver and the RISC processor was built in order to verify both the RF performance and its interaction with the digital circuitry.
Jennic had selected IBM as its favoured foundry for the JN5121. "We wanted to work with a company that had good processes and where we would get a high level of support to get good time to market," said Lucido.

IBM has made many of its processes available to MOSIS. As a result, Jennic was able to use exactly the same 0.18µm process for the trial chip that was fabbed through MOSIS' MPW service as that used for the final chip. There was no need to change design file formats or adjust the design rules. This is one key advantage of the MOSIS service. By having arrangements with many leading foundries, customers can use the MPW service for risk reduction on key parts of a chip design. They can then run the final silicon through the same fab using their own mask set.

The availability of an MPW path for trial chips meant Jennic could afford to tune the design for better performance. Companies who decide to go to implementation using full mask sets may find that too expensive. "We got the chip working functionally first time," said Lucido. "But, since that first chip, we had one more iteration to get the RF performance to where we wanted it to be."

Since September, the company has been shipping products fabbed by IBM to customers and is looking at next-generation designs and variants. "The product today is positioned to be able to satisfy the demands of the whole sensor-network market. We are seeing such a diverse range of applications where customers are using the product. However, we are looking to introduce cost-optimised products for specific markets next year," said Lucido.
The initial variants will probably not use MPW prototypes as the changes will largely be to digital portions of the design. "But we may do derivative designs and use MPW to test parts of them out if we decide to make more fundamental changes to the architecture for next-generation products," explained Lucido.